EE-382M
VLSI-II
Early Design Planning for:
Physical Design (PD)

Spring 2017

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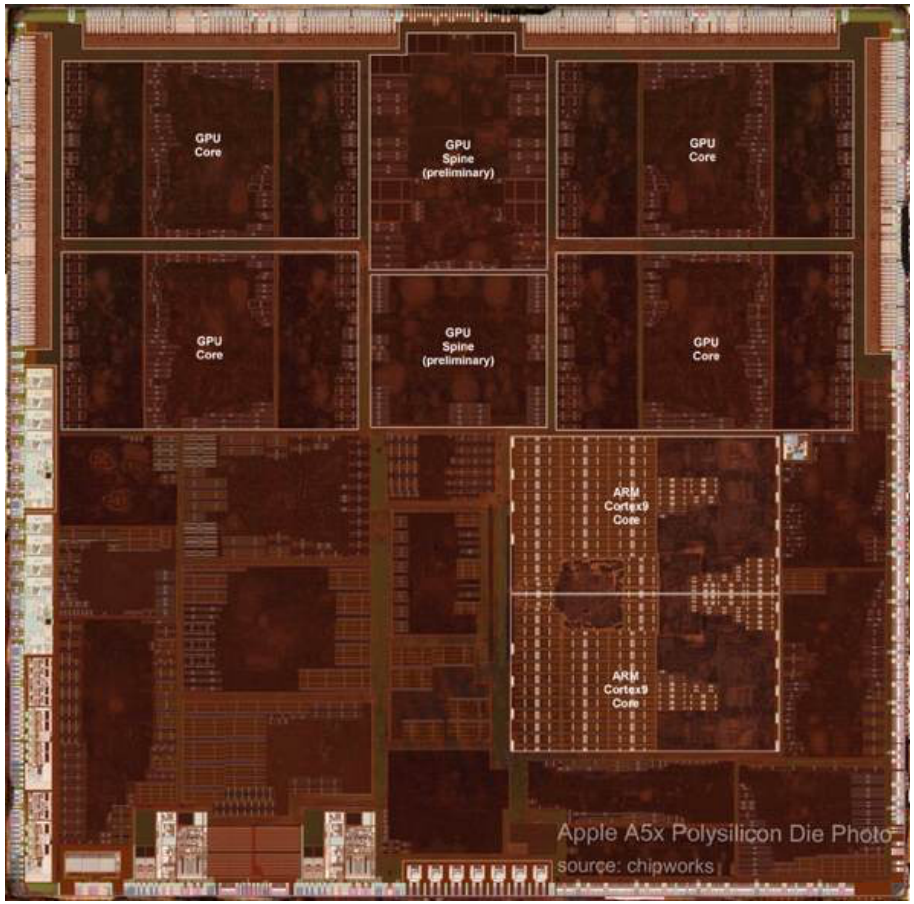


Apple A5X Die Photo

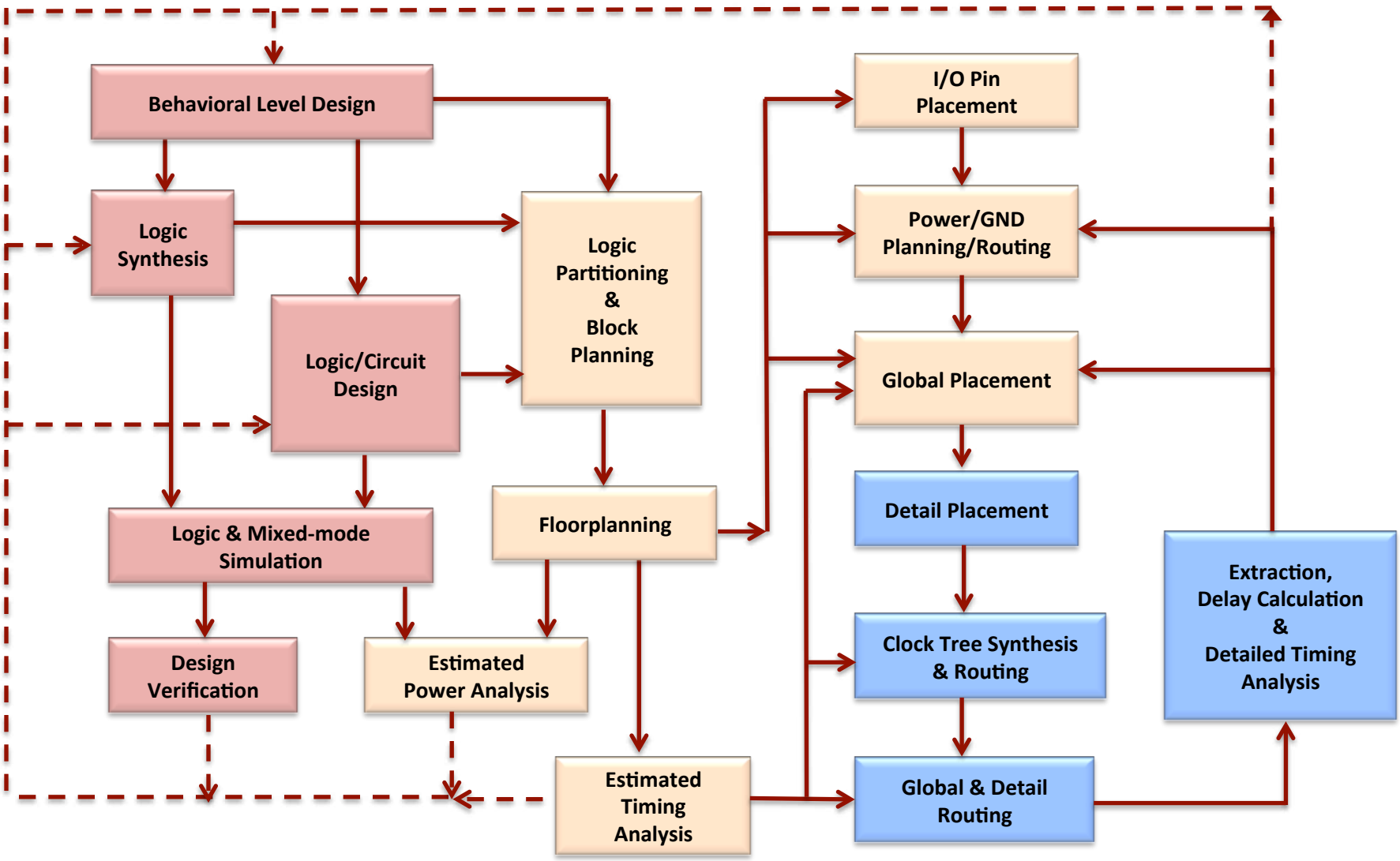
Agenda

- Design flow review
- Physical design
- Floorplanning
- Metal planning
  - Clocks
  - Power grid
- Memory array planning

TLAs

- EDP – Early Design Planning
- PD – Physical Design
- FE – Front End
- BE – Back End
- SOC – System-on-Chip
- SC – Standard Cell
- SDP – Structured Datapath
- STA – Static Timing Analysis
- .LIB – STA Library
- ABGEN – Abstract Generator
- APR – Auto Place & Route
- LEF – Library Exchange Format
- DEF – Design Exchange Format
- TTM – Time to Money

Design Flow Review



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- **Physical design**
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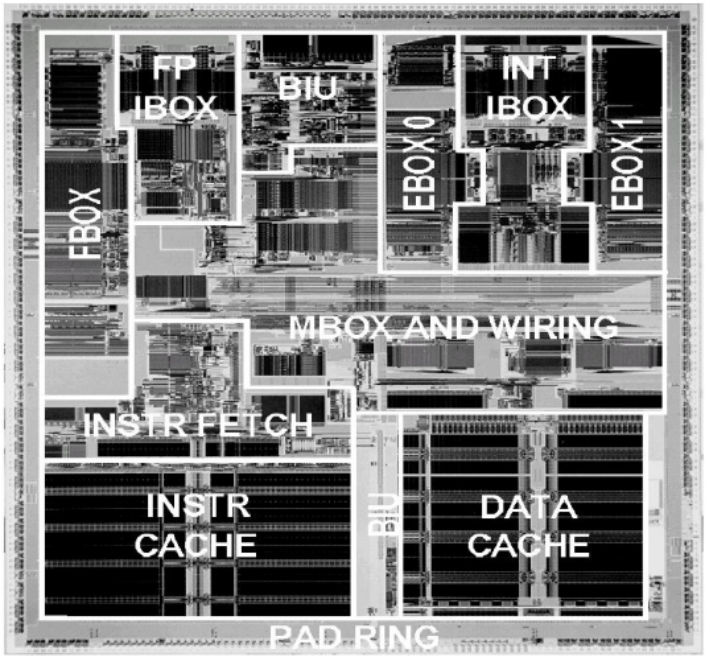
PD is handled by the Integration Team

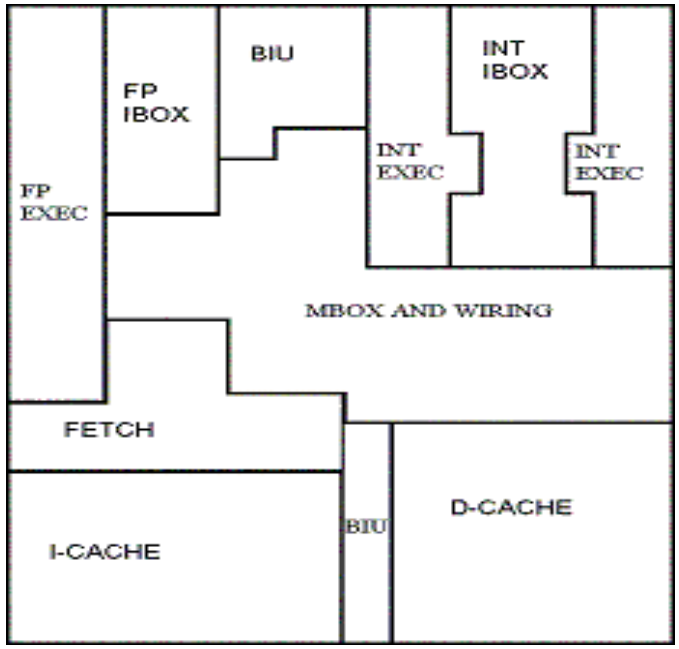
- **Integration teams are responsible for:**
  - Doing a floor plan of the top level of the chip
  - Characterizing the top-level routing delays and determining the assertions and constraints for each cluster.
    - They will be working with each cluster to optimize the constraints
  - Designing the clock routing structure
  - Determining the clock regeneration circuitry
  - Determining the reset logic
  - Designing the power grid
  - Determining global clock and signal route power estimation
  - Generating the power budget for each cluster
  - Generating the area budget for each cluster

NOTE: There are typically between 40 – 60 floorplans generated during the course of a chip design.

PD-EDP Activities

- **PD-EDP activities include:**
  - Detailed floorplan of the block level components.
  - A reasonably detailed top-level floorplan using the cluster abstracts followed by final block synthesis and AP&R using a 32/28nm std-cell library
  - Memory blocks built with Synopsys memory compiler (SAED-MC)
  - Approximate clock routing at the top-level
  - Approximate Power-GND routing at the top level





PD Prerequisites

- **The types of data that are required to start a physical design are:**
  - Technology and library files
  - Circuit description of the design in the form of netlist representation
  - Floorplan constraints
  - Timing and Design Rule Constraints
- **Technology and library files:**
  - Manufacturing grid
  - Routing layer definition & routing grid
  - Standard cell placement tile
  - Placement and routing blockage layer definition
  - Via definition
  - Conducting layer density rule
  - Metal layer slotting rule
  - Routing layer physical profile
  - Antenna definition
  - Required manufacturing cells such as fiducials, alignment markings, Intra-Die-Monitoring cells, Power rail monitoring cells, etc.
  - C4/wafer bump constraints and last-metal layout rules.

PD Prerequisites (cont.)

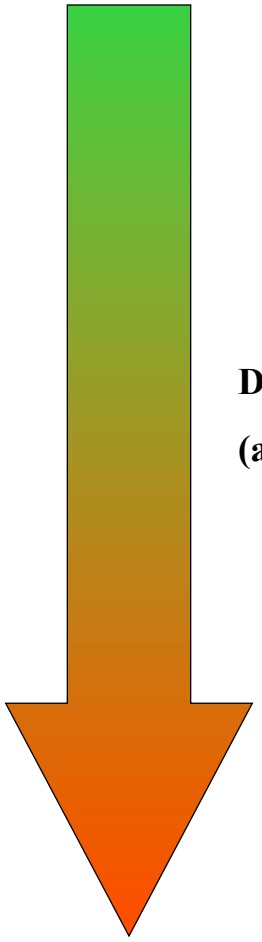
- **Circuit description of the design in the form of netlist representation:**
  - Gate level HDL Model
    - Schematic based
    - Synthesis generated
- **Floorplan constraints (Chip & Block Level):**
  - Power grid
  - Clocking
  - Signal Routing including pre-routes & shielding requirements
  - Structured Data-path area
  - Random logic area
  - White space
  - "Thru-block" routing
  - Identify power grid and clock-domain 'islands'
    - Synchronous and asynchronous regions
    - Determine signal level shifters and clock-domain-crossing checks
      - Synchronizers may be required, or special clock budgeting when crossing different clock frequencies.

PD Prerequisites (cont.)

- **Two basic types of design constraints:**
  - Timing constraints
  - Design rule constraints
- **Timing constraints utilized by physical design tools include:**
  - System clock definition and clock delays
  - Cycle time and clock budgets (based on actual variability circuit simulations of sequential elements) for MIN and MAX DELAY
  - Multiple cycle paths
  - Input and output delays
  - Minimum and maximum path delays
  - Input transition and output load capacitance
  - False paths
- **Design rule constraints include:**
  - Maximum number of fan-outs
  - Maximum transitions
  - Maximum capacitance
  - Max wire length

PD Implementation Options

- **Synthesis – Standard Cell (SC)**
  - Cell layout comes from a shared cell library
  - Automated cell selection and placement
  - Automated placement and routing (APR) between cells
- **Structured Datapath(SDP)**
  - Cell layout comes from a shared cell library
  - Manual cell selection and relative placement
  - Automated routing between cells
- **Custom Design (CD)**
  - Cell layout is unique for each application
  - Manual cell selection and placement
  - Manual routing between cells



Increasing Design Effort (and Density)

PD Implementation Options (cont)

	CD	SDP	SC
RTL Coding	M	M	M
Logic Minimization	M	M	A
Cell Placement	M	M	A
Device Sizing	M	A	A
Layout	M	A	A

A = Automatic

M = Manual

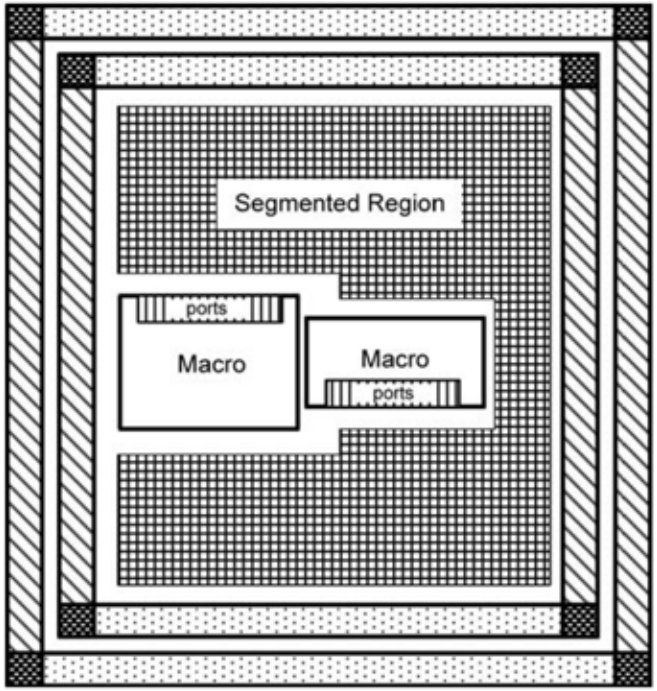
	CD	SDP	SC
Timing	Best	Better	Worst
Density	Best	Better	Worst
Design Time	Worst	Better	Best
Revisions	Terrible	Tolerable	Best

Agenda

- Design flow review
- Physical design
- **Floorplanning**
- Metal planning
  - Clocks
  - Power grid
- Memory array planning

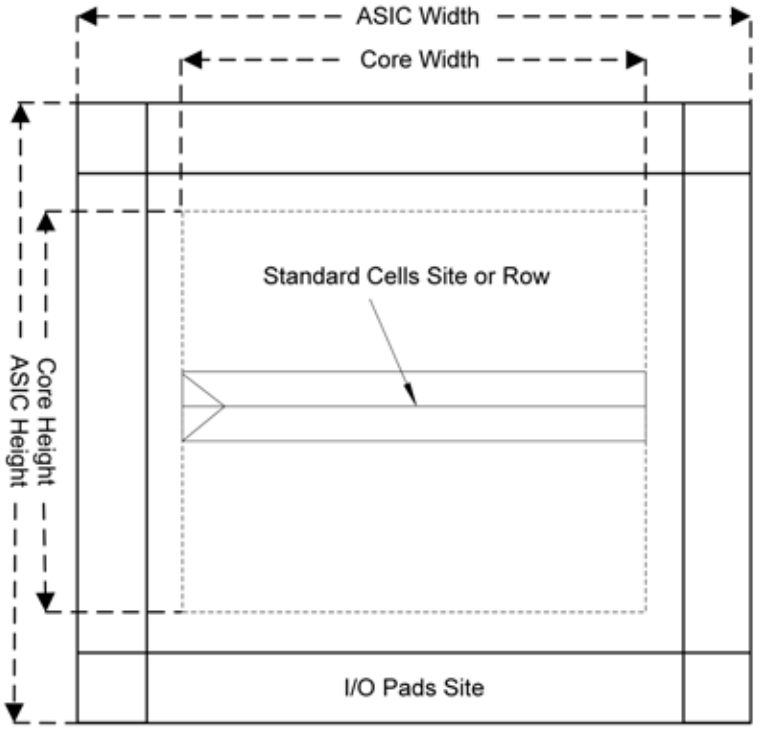
Floorplanning 101

- **Determine block sizes**
  - Function of SC pitch, Cell Placement, RLM, SC/SDP, Custom/ Memory Block Sizing and Block Routing Overhead (Signals, Clocking, Power)



Floorplanning 101

- **Determine block sizes**
  - Function of SC pitch, Cell Placement, RLM, SC/SDP, Custom/ Memory Block Sizing and Block Routing Overhead (Signals, Clocking, Power)
- **Determine core size**
  - Function of #Blocks, Block sizes, Block Aspect Ratios, Global Routing Overhead (Signals, Clocking, Power)
- **Determine I/O ring size**
  - Function of the number of I/O, Number of Power Pins and Placement



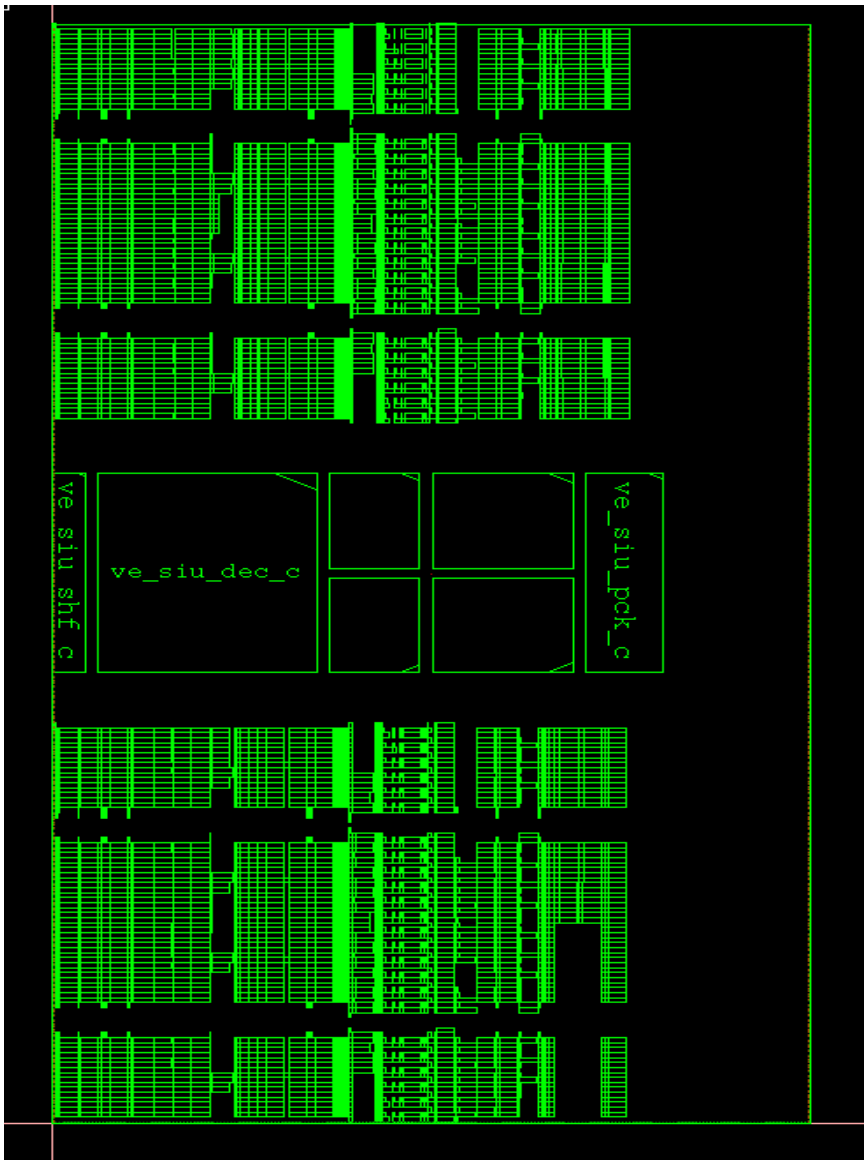
Macro/Cell Placement & Routing

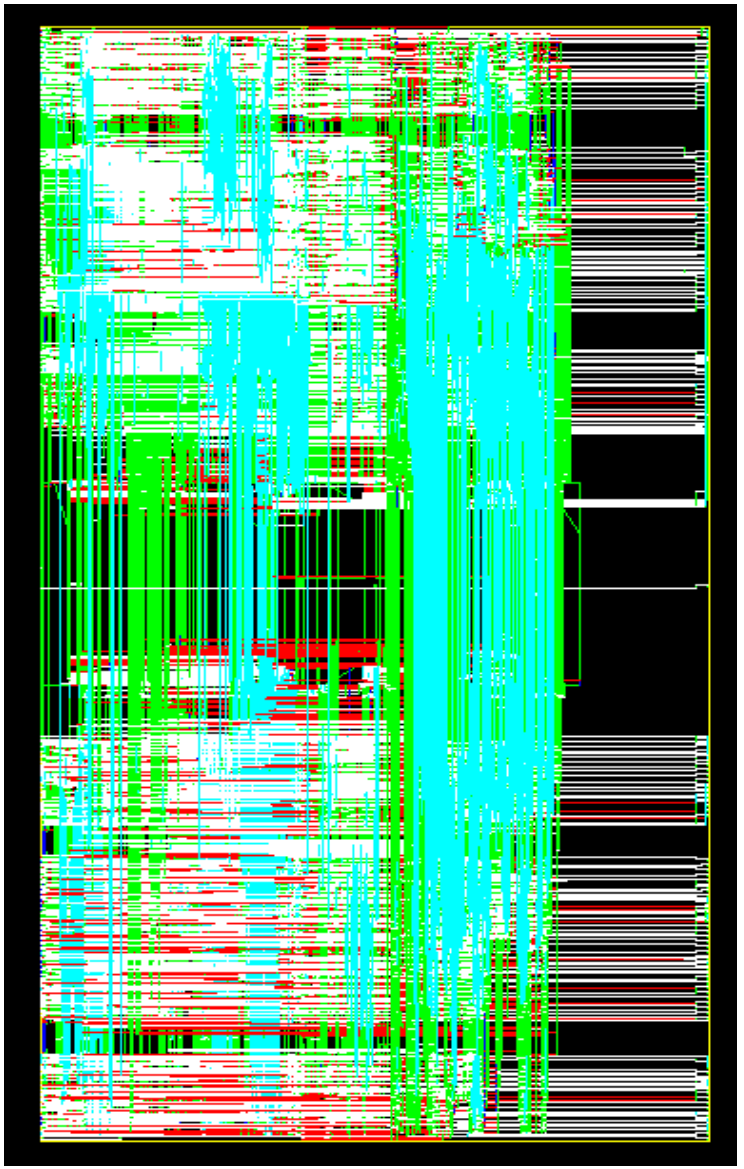
- **Start with the critical path!**
  - Use "regions" to place cells to limit the wire load on the critical path
    - Move less critical blocks out of the way
  - Pre-route critical paths

- **Pre-place critical macro cells to "guide" placement tool**
  - Can set the one of the dimensions of the chip

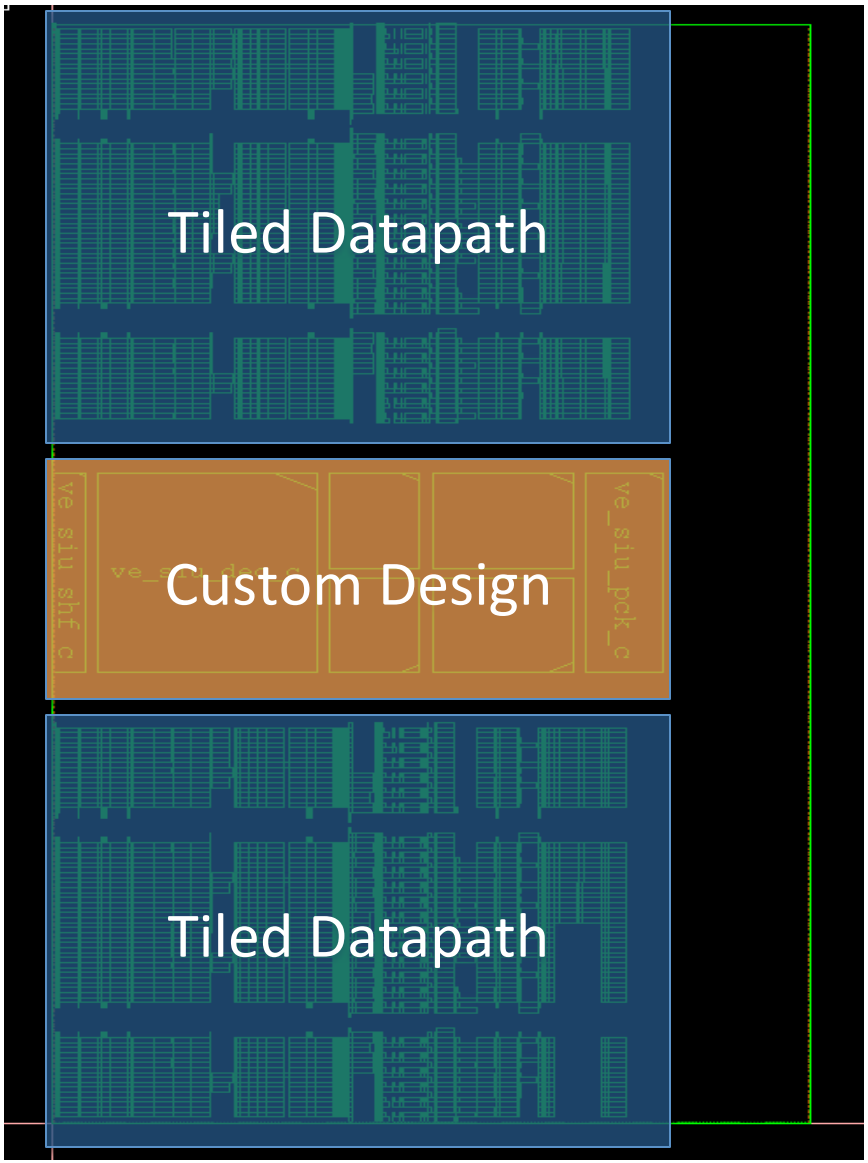
- **Pre-place clock generators to limit clock wire load**
  - Again, place most critical local clock buffers (LCB) first if area is tight
  - Ideally there should be minimal side loads

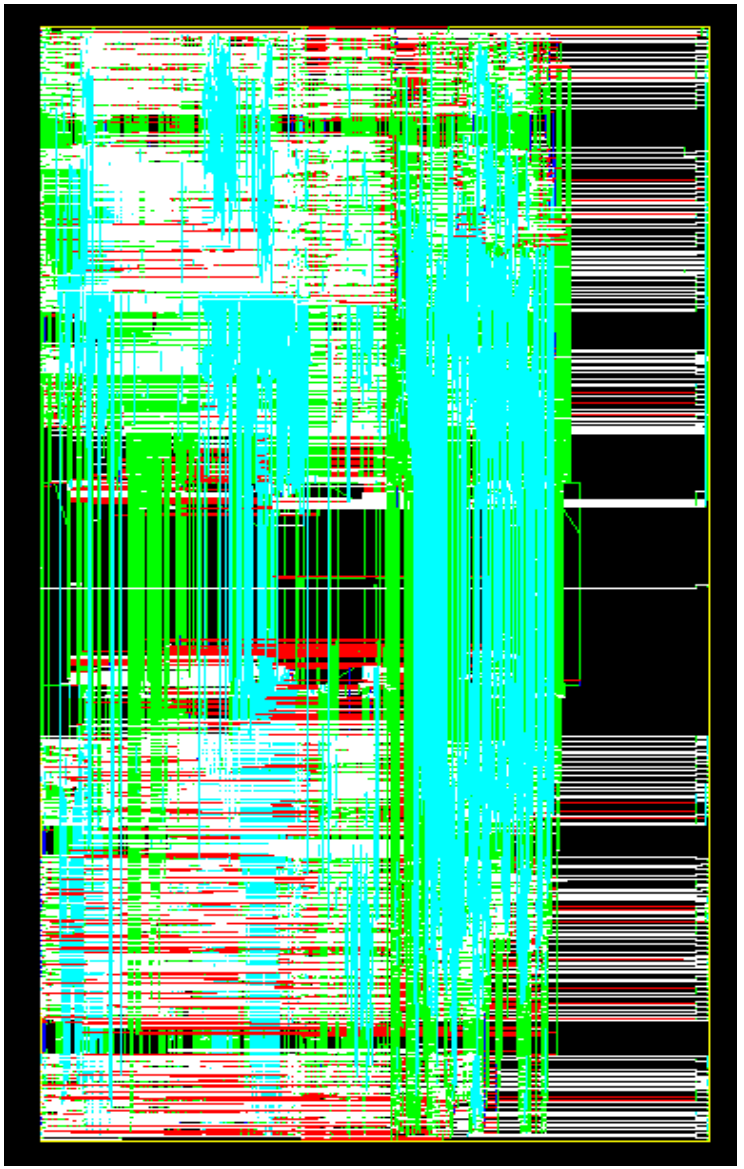
Cell Placement & Routing (example)



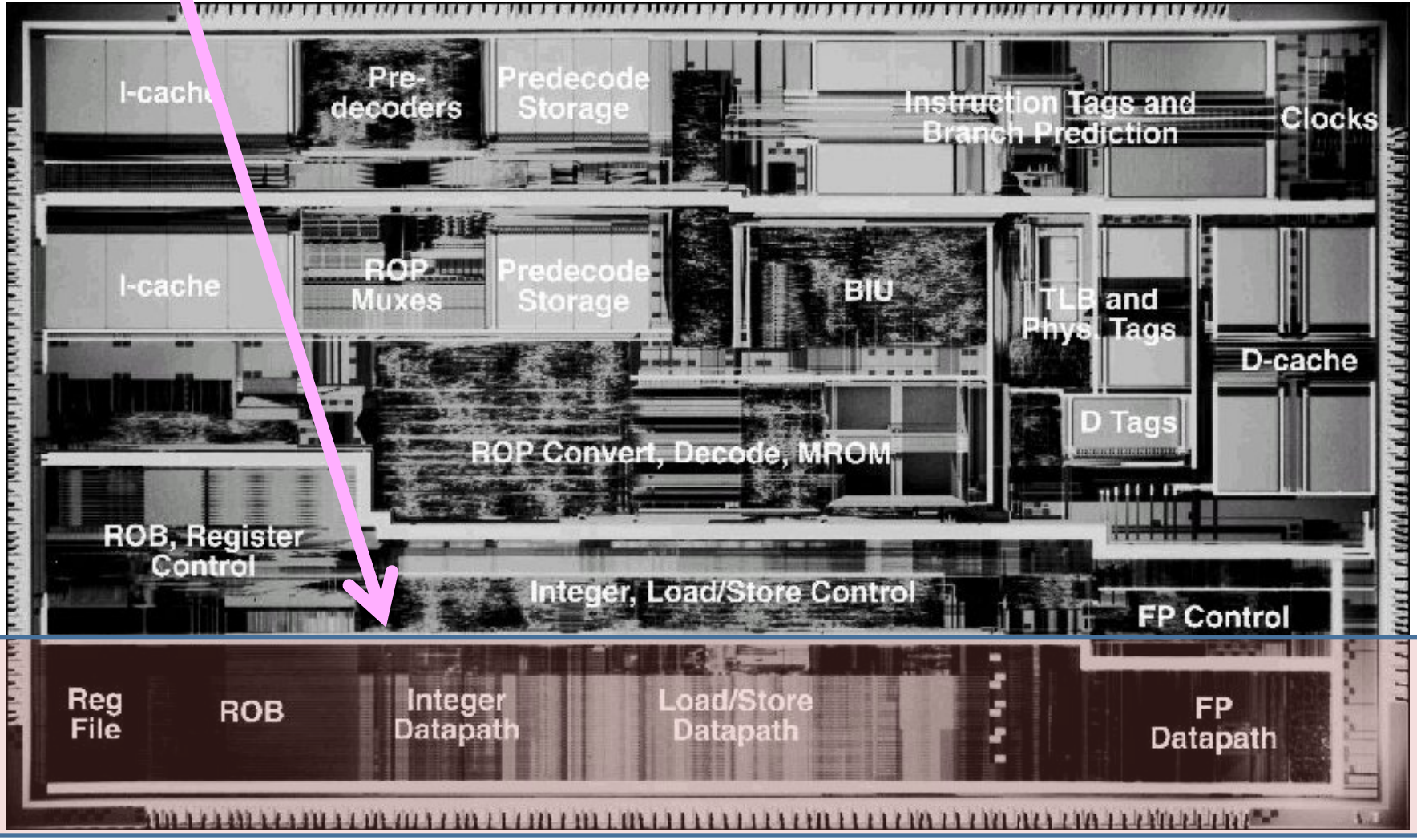


Cell Placement & Routing (example)





Hard Macros Defining Width of Chip



AMD K5 Datapath

Agenda

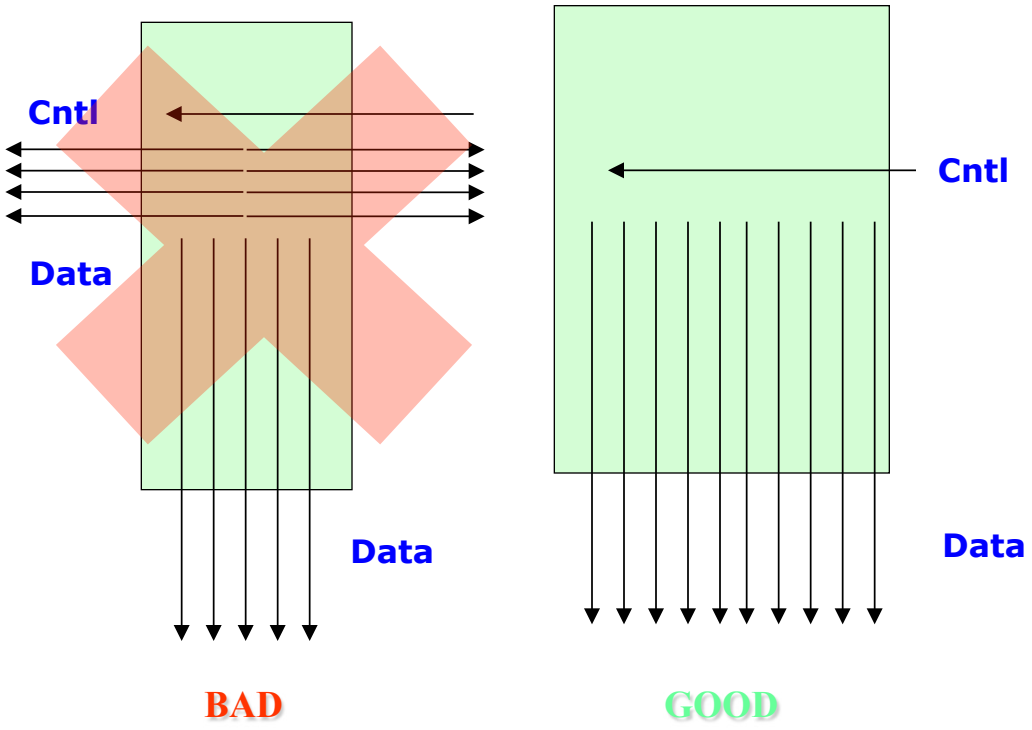
- Design flow review
- Physical design
- Floorplanning
- **Metal planning**
  - **Clocks**
  - **Power grid**
- Memory array planning

Metal Planning

- **Metal layer, width, spacing and shielding are negotiable**
  - "Negotiable" means you have to plead your case to the integration leader
  - All of these impose a physical constraint for layout
- **Typical 8 layer metal layer allocation**
  - M1,M2 : Local routing (standard cell)
  - M3,M4, M5, M6 : Data and control
  - M7,M8 : Power, Ground, Clock, Reset, etc
  - Assume HVH routing:
    - Metal-1: Horizontal
    - Metal-2: Vertical
    - Metal-3: Horizontal
    - Metal-4: Vertical
    - …..
- **Use standard 'HALO' cells to make the resulting 'floor-plannable' objects 'snap' to the desired power and routing grids.**
  - Added to the boundary of all custom layouts (as well as synthesized blocks).

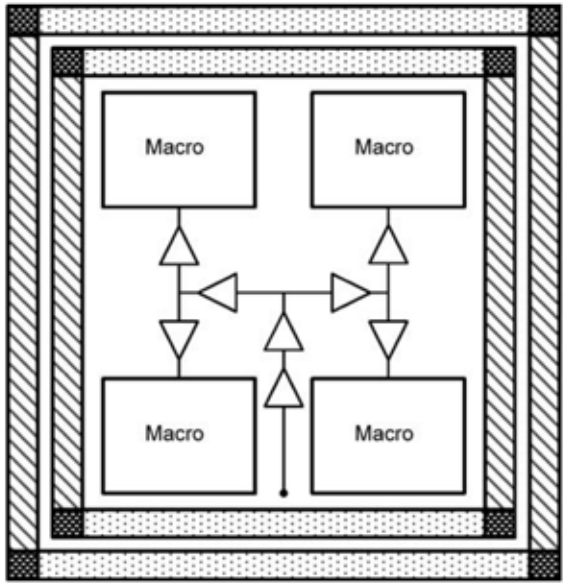
Metal Flow Planning

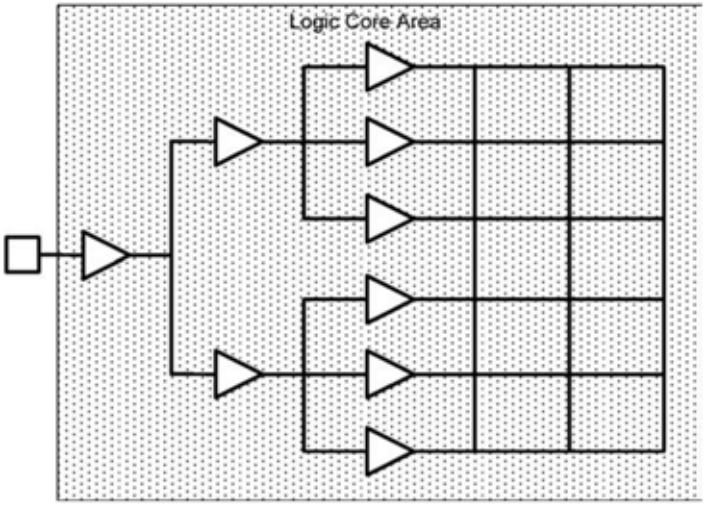
Avoid bi-directional dataflow



Chip & Block Level Clock Routing

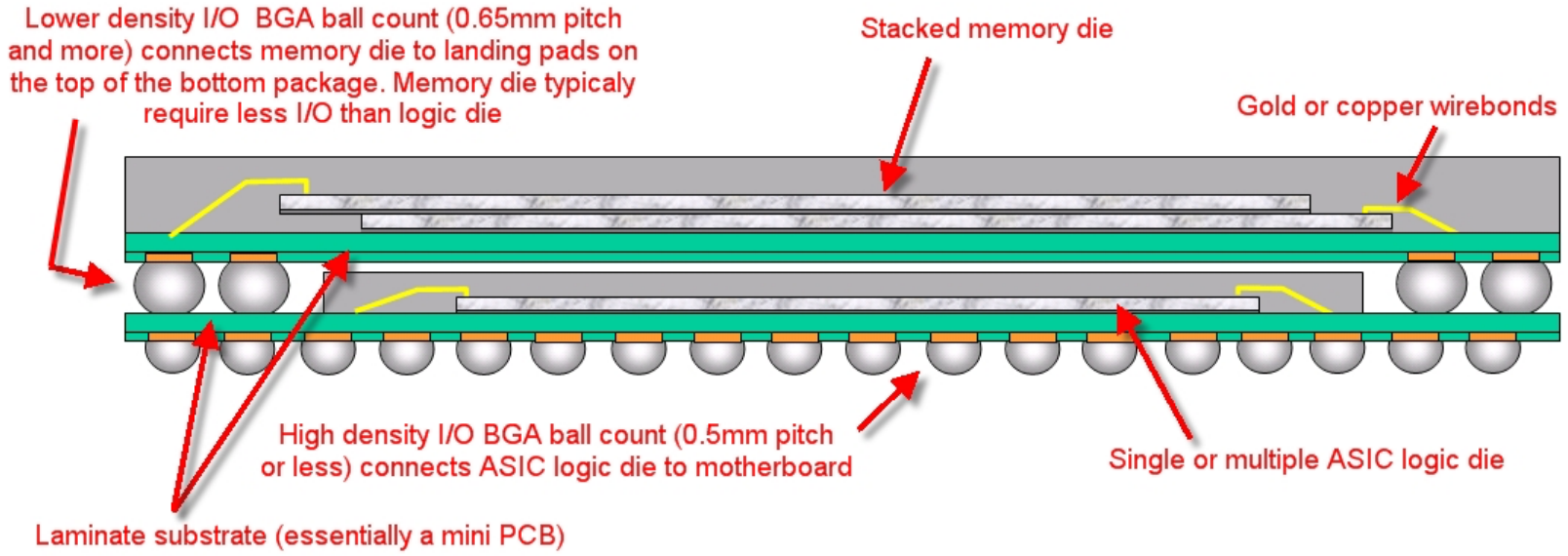
- Watch out for the clock, it's your most critical net
- Make sure the physical design treats it accordingly
- Help reduce clock power by eliminating unnecessary load
- Make sure the clock net has enough via coverage
- Use a combination of Global (Chip) and Block Level Clock distribution





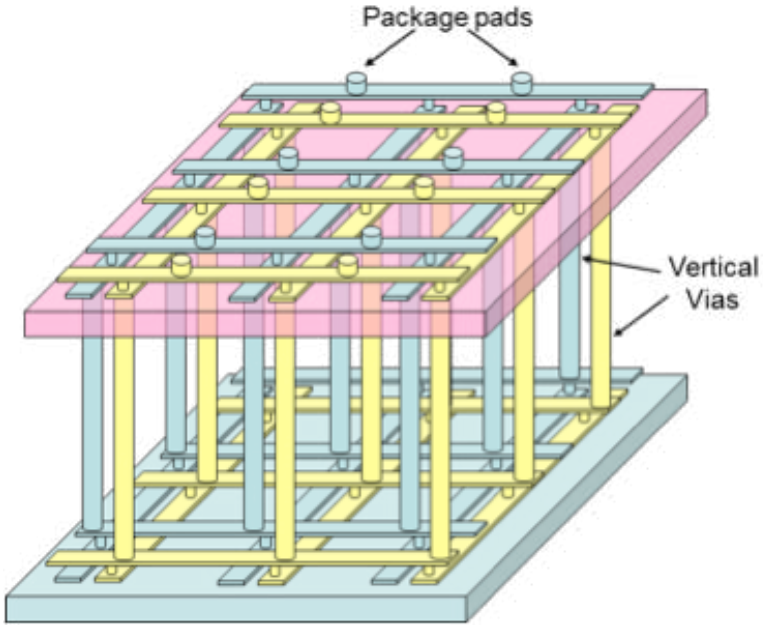
Power Grid

- Delivers current from the package and C4 bumps to the transistors
- Designed to deliver "typical" current density to the devices
- Increasing current density by arraying large devices can cause you to exceed the power grid's nominal design



Power Grid Considerations

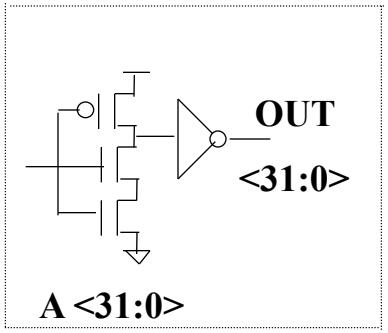
- Be very careful arraying large drivers
- Follow the % power guidelines for the power grid
- Try to keep temporal relationships between arrayed drivers
- Consider the physical impact on the grid by your design
- Be prepared to make the grid more robust to compensate for marginal grids



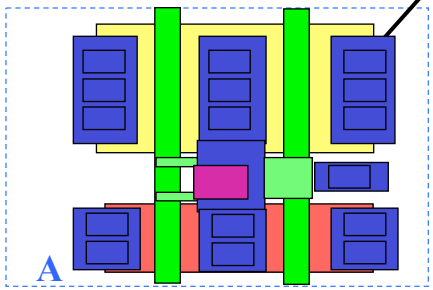
Think of the grid as a straw between the C4 and the devices.

Too many devices drawing current through the same via or too narrow a via can cause devices to starve and the supply to dip or crater!

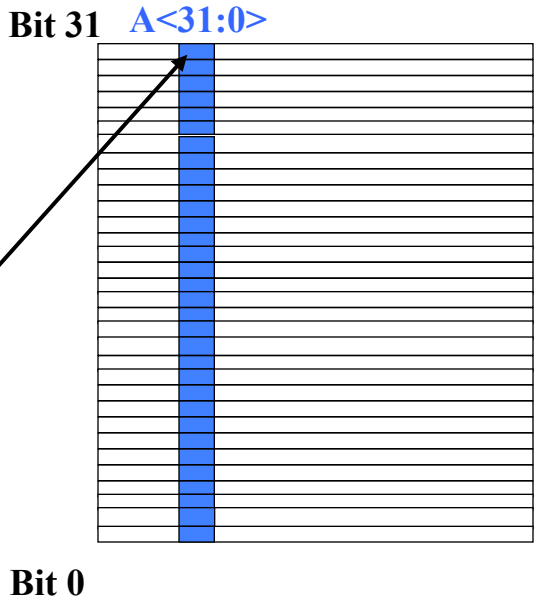
Power Grid Considerations (cont)



SCHEMATIC VIEW

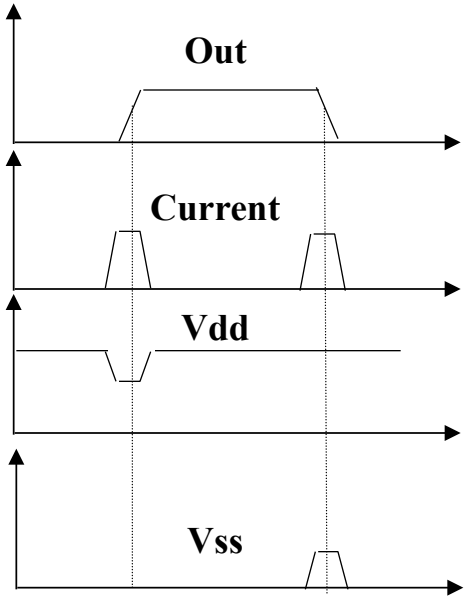


CELL LAYOUT VIEW



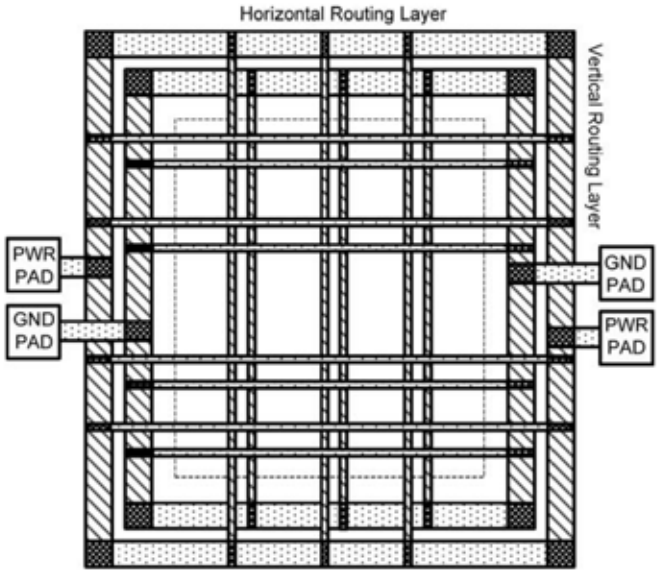
RELATIVE CELL PLACEMENT

When large, arrayed drivers pull on the same rail, supply bounce can occur degrading performance and causing supply offset noise

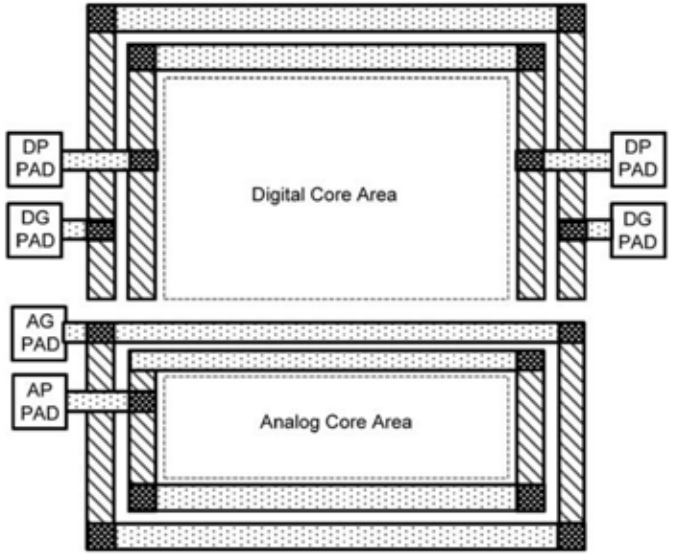


Chip level power routing

- **Power busses are a combination of rings and/or grids.**
  - Rings are generally in the I/O ring.
  - Grids are used at the chip and block level
  - Grid pitch is set by horizontal and vertical routing resource requirements

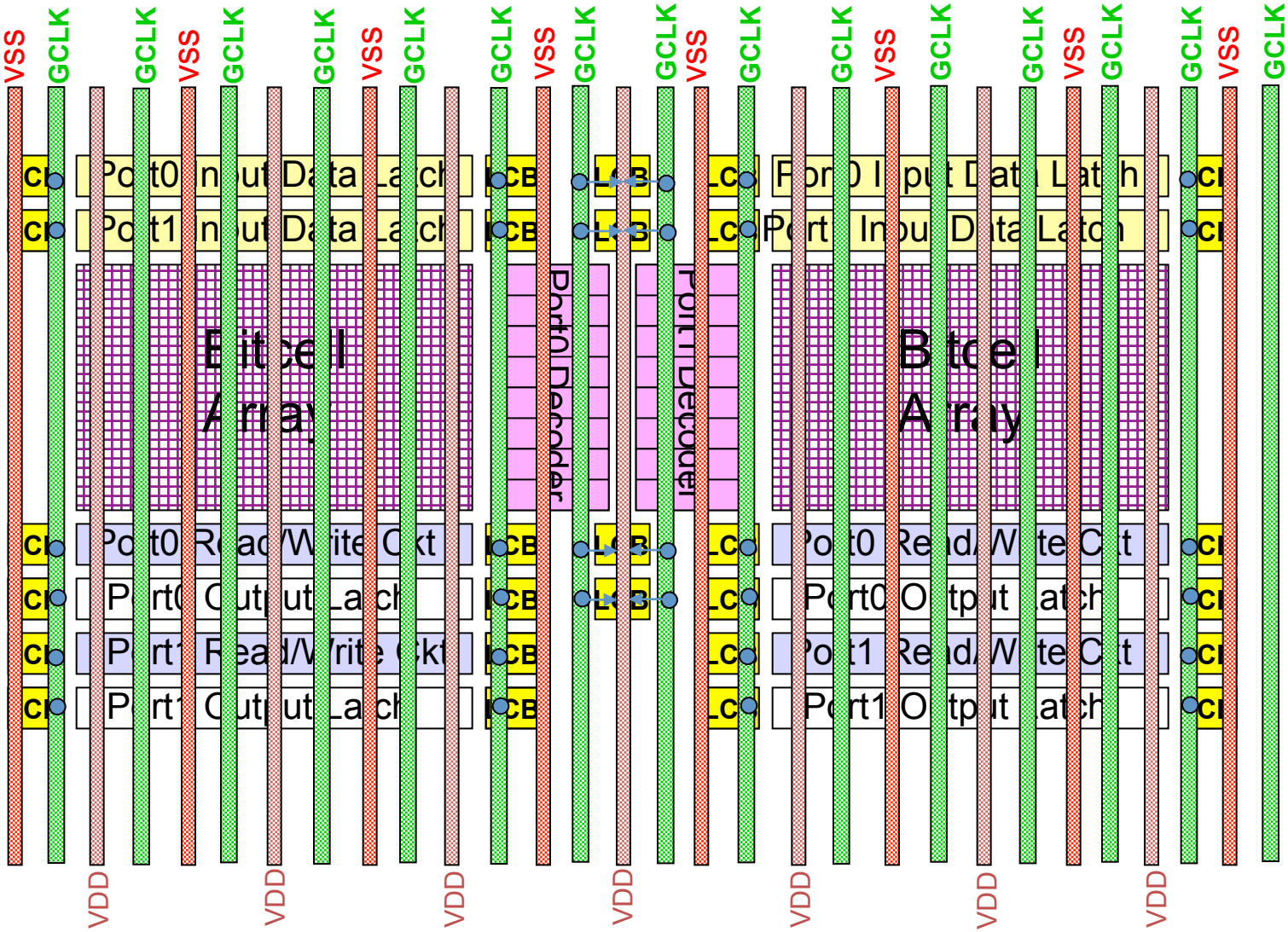


- **Special consideration needs to be taken for multiple power domains.**
  - There can be any number of power domains depending on the system architecture
  - Analog blocks require isolation rings
  - Interfaces between blocks require level shifters



Power/Clock Grid Example

- Clock grid is interleaved between VDD and VSS on metal6



Shielding

- Intentionally routing signals to control the effective line-to-line capacitance seen during switching.

- Requires designers to constrain the physical assembly done by routing tools or physical design specialists (PDSs).

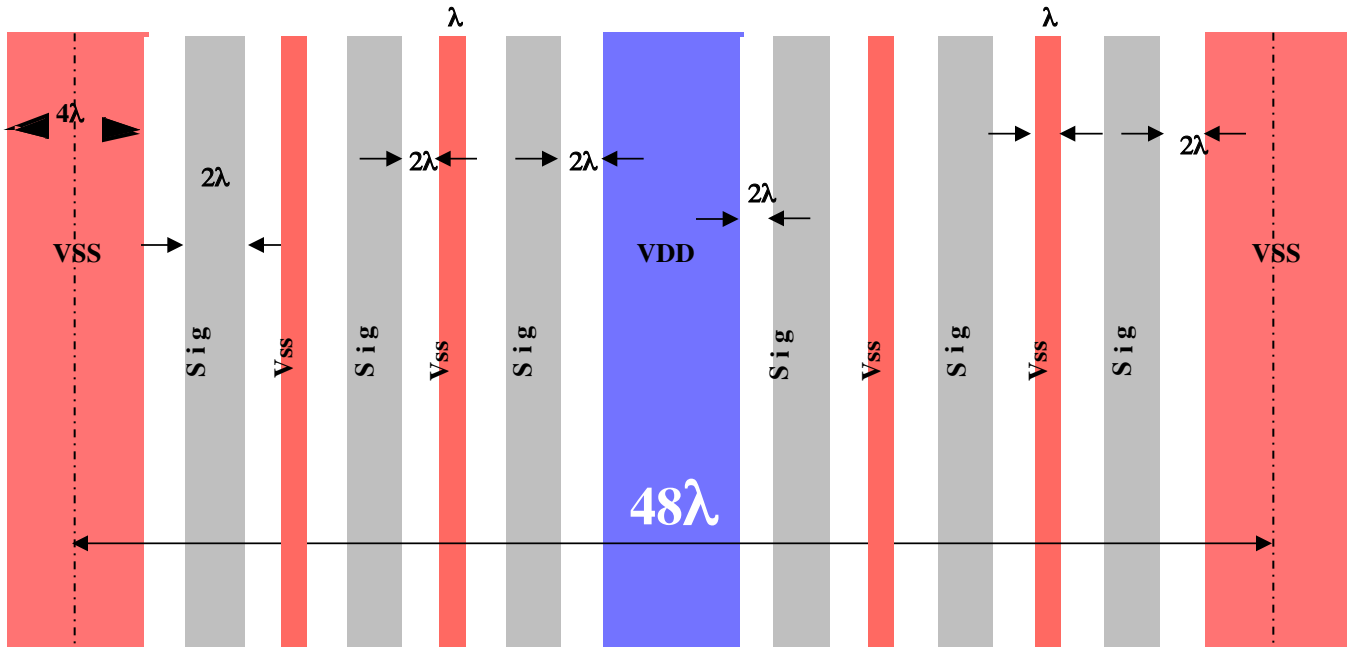
- Falls into one of three categories:
  - Physical shielding - signals are routed next to a power rail
  - Logical shielding - signals are routed by logically related signals
  - Temporal shielding - signals are routed by temporally distinct signals

Power/Ground/Signal Shielding Example

- Shielding takes up significant routing resources.

- Global M6 routes over the array should have minimal coupling noise to array bitlines.

(Full Shielding, MCF = 1.0)



* Where λ is minimum critical dimension for width/space

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- **Memory array planning**

Array Area Estimation

- **Cell Area**
  - 6T bitcell dimensions strongly dependent on technology
    - Manufacturing/FAB provides this
  - Multiported cells are wire limited and can be easily caculated
    - Cell Height is a function of {MH_Pitch*(Wordlines + Shields)}
    - Cell Width is a function of {MV_Pitch*(Bitlines + Datalines + Shields)}

- **Local Bitline Receivers and Dataline drivers**
  - Height of array is increased by local bitline receivers
    - NumReadPorts*NumEntries/CellPerLBL

Array Area Estimation

- **Decoder & Wordline Repeaters**
  - Width of array is increased by the decoder
    - Decoder width is a function of number of ports
    - 20% of total array width is a reasonable estimate
  - Width of array is increased by wordline repeaters
    - Typically no more than 32 to 64 bitcells on a single wordline (limits rise/fall time of selected row)

Array Area Estimation

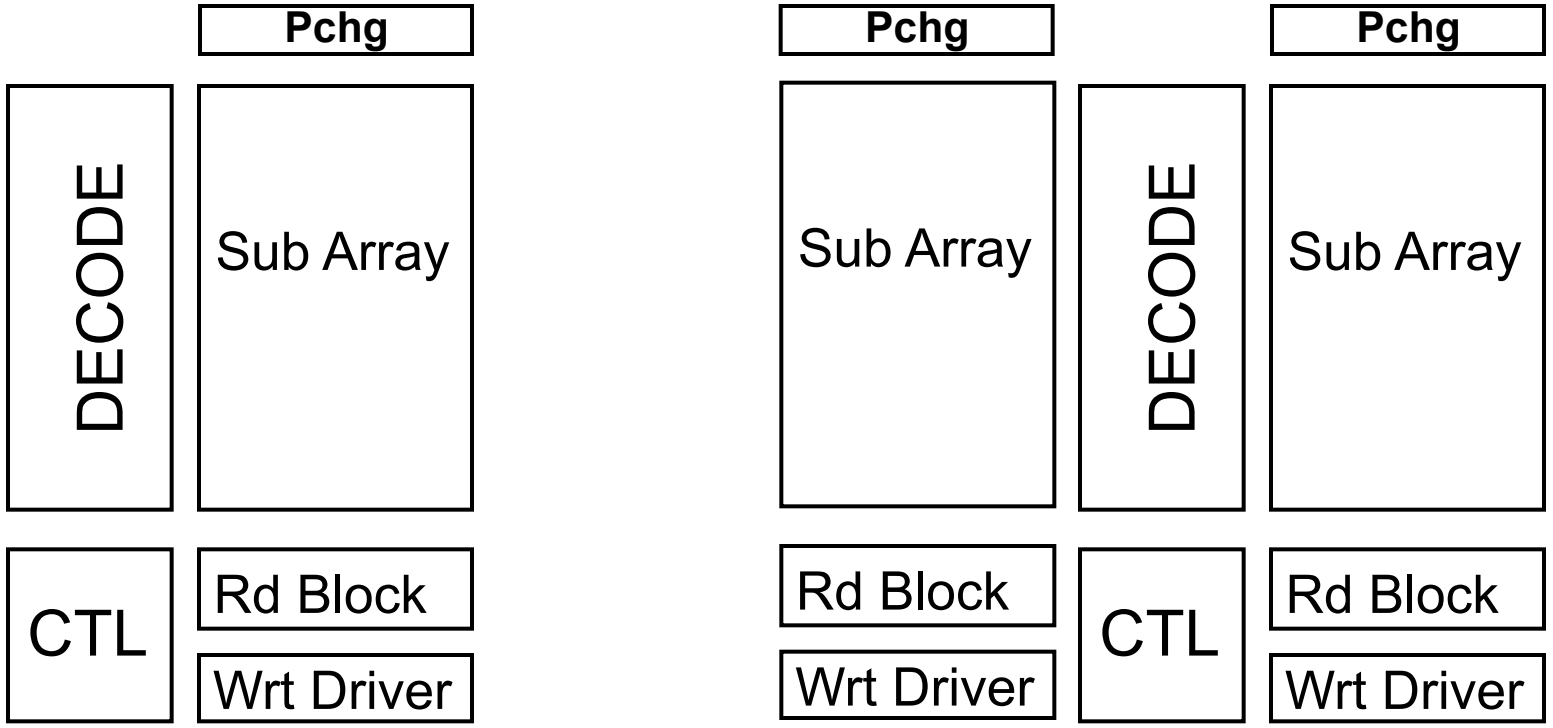
- **Cell Height & Width Calculation**
  - Cell Height = {MH_Pitch*(Wordlines + Shields)}
  - MH_Pitch*[(#R + #W) + WL_shield*(#R + #W + 1)]
  - Cell Width = {MV_Pitch*(Bitlines + Datalines + Shields)}
  - MV_Pitch*[(#R + Rd_shield*#R + 1) + (#W + Wr_shield*#W + 1)]

  - Where
    - #R Number of Read Ports
    - #W Number of Write Ports
    - WL_shield Read wordline shield factor
    - Rd_shield Read bitline shield factor
    - Wr_shield Write dataline shield factor
    - MH_Pitch Wordline Pitch
    - MV_Pitch Bitline Pitch

SRAM Array Area Estimation

- **Estimate sub-array first:**
  - # 6T bitcells * bitcell area + wordline & column decoders + sense-amp + read/write sequentials.
  - The decoders + sense-amps + sequentials are typically 15% of the subarray bitcell area.
  - Use an 'array efficiency' factor to calculate the total SRAM array area; this includes clock buffers, address decoders, control logic, repeaters, routing, etc.; typical numbers are in the range of ~60%.
- **EXAMPLE:**
  - A 16KB L1 cache with four 4KB subarrays; each subarray is comprised of 128 bitcells/column and 256 bitcells/wordline; the 6T bitcell area in this 45 nm CMOS technology is 0.38 mm2.
    - Bitcell subarray = 0.38 mm2 * 128 * 256 = 12,452 mm2
    - Subarray = 1.15 * 12,452 = 14,320 mm2
    - 4 subarrays = 4 * 14,320 = ~57,280 mm2
    - 16KB L1 cache = 57,280 / 0.60 = 95,467 mm2

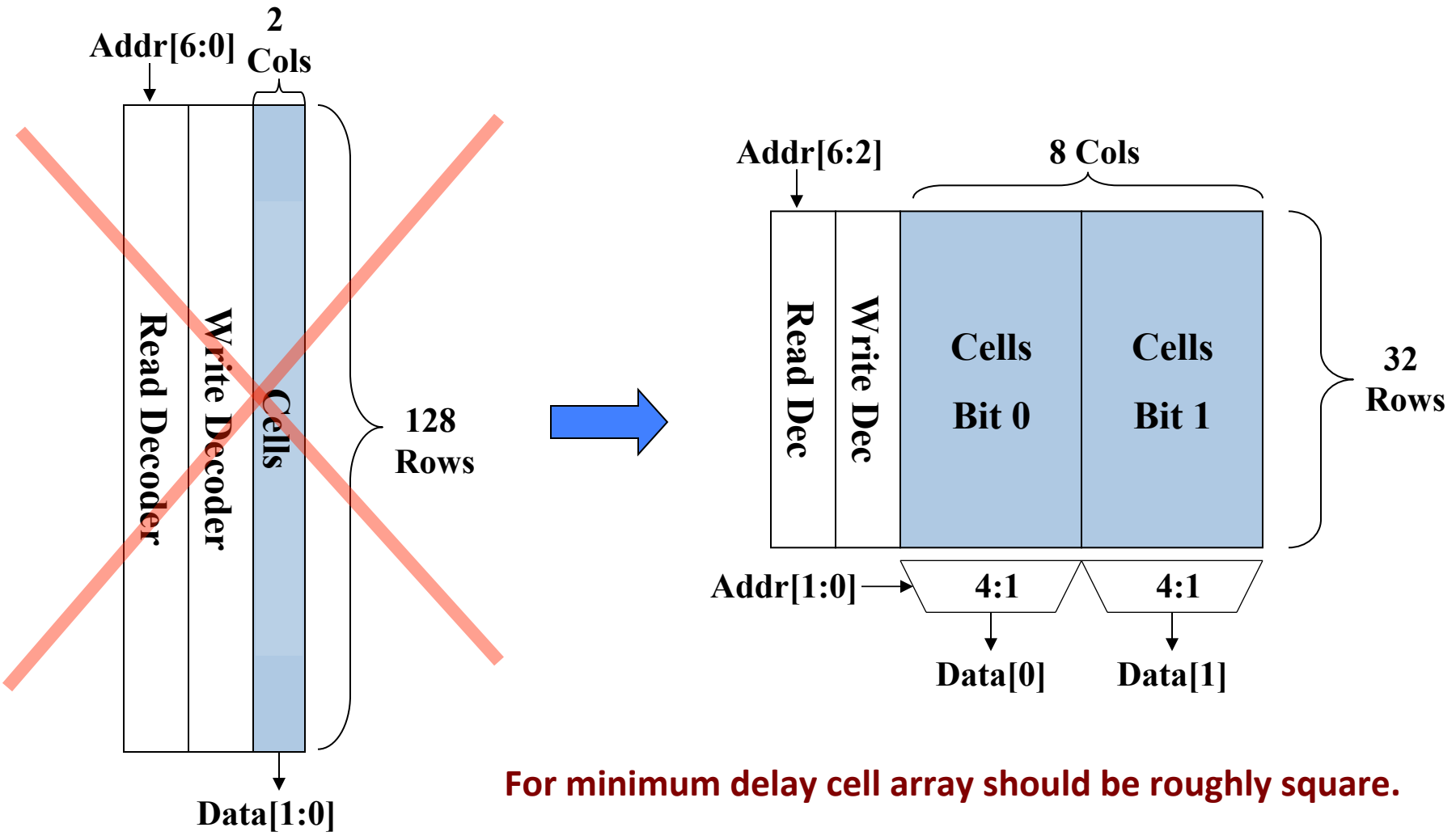
Floorplan Options



Possible Large-Signal Array Floorplans

Array Area Calculator provides dimensions for these blocks

Dual-Ended Cell Column Muxing



For minimum delay cell array should be roughly square.

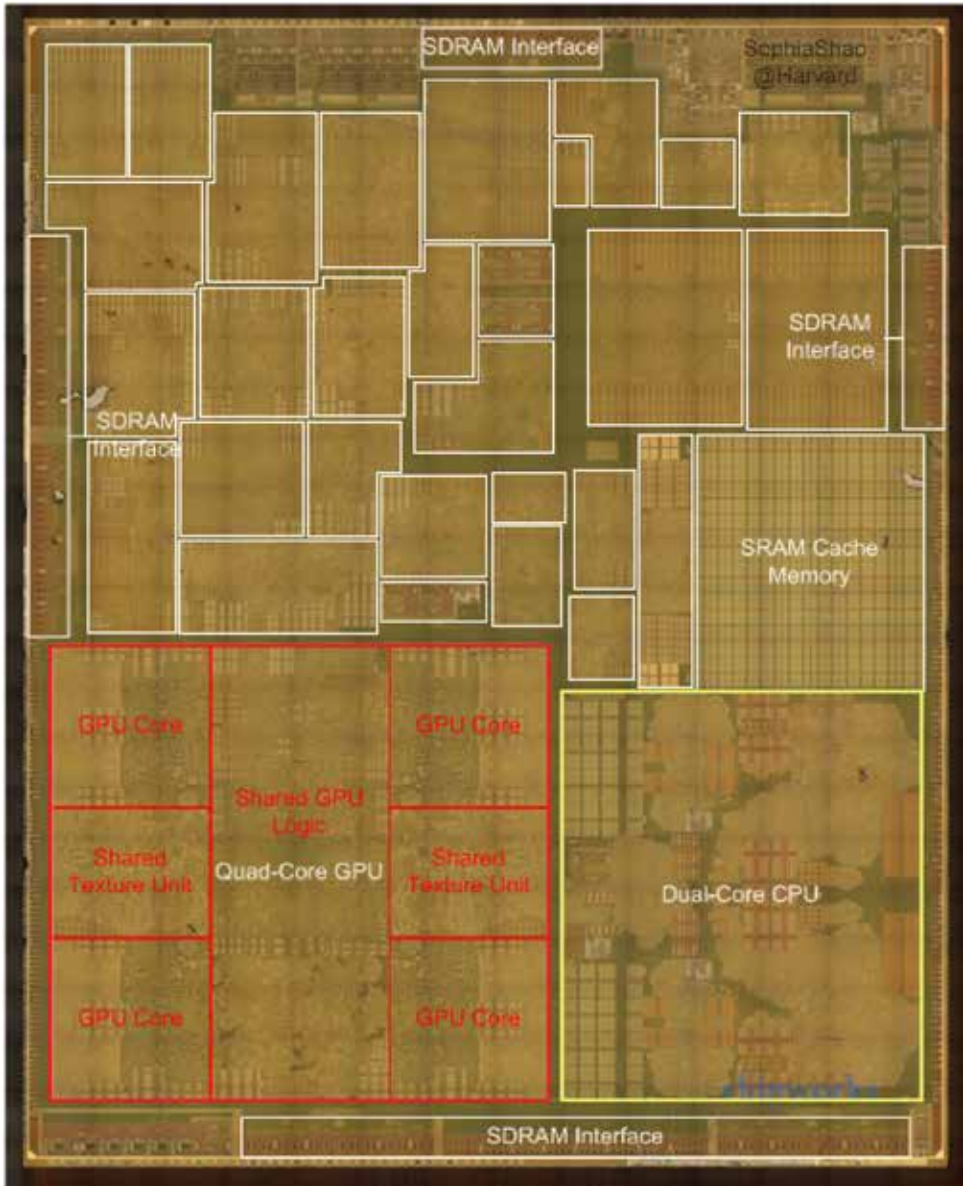
Summary

- **Early design planning and and improved layout density can have a significant impact**
  - Die size, profit & power are impacted by layout density
  - Schedule is impacted by implementation decisions

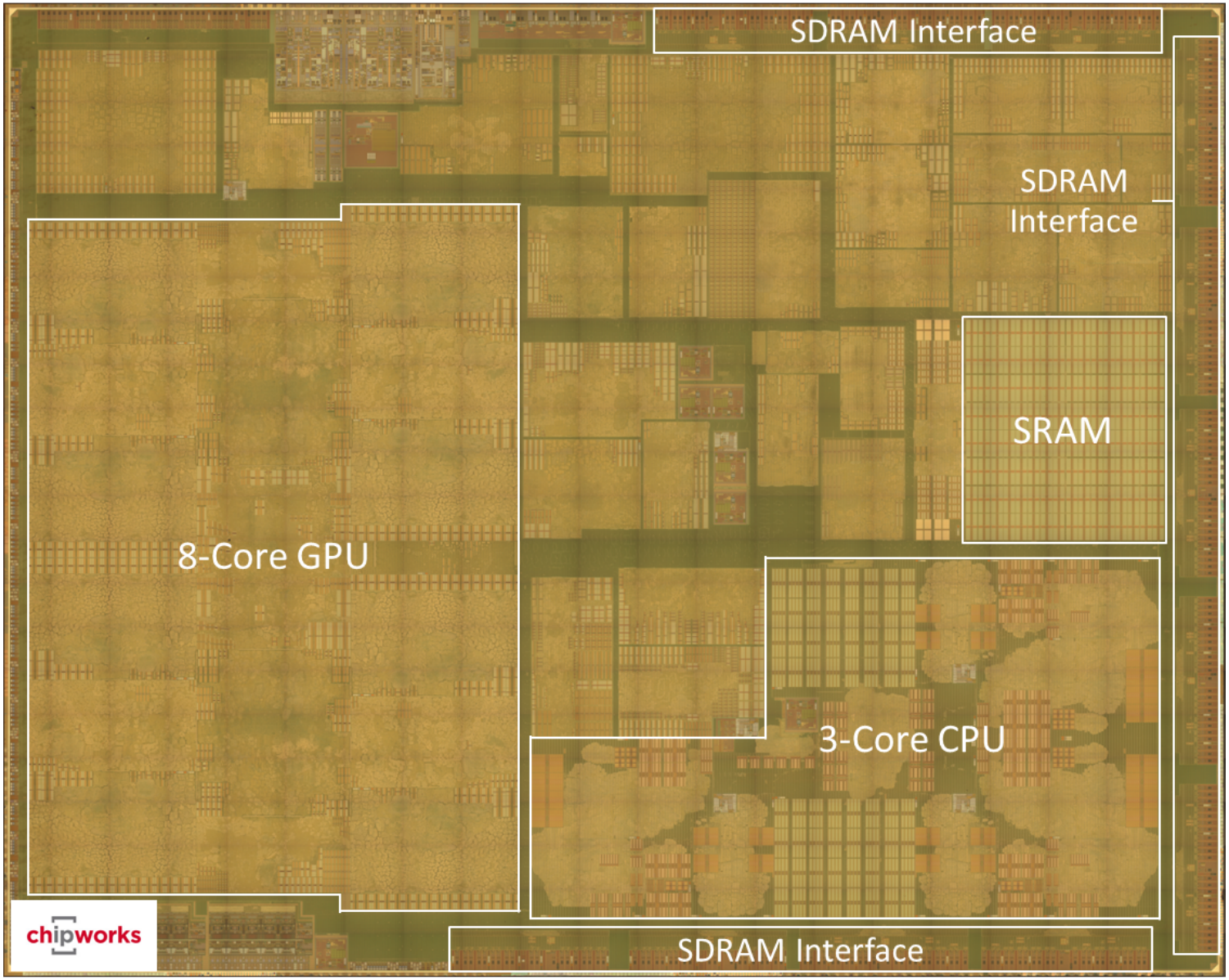
- **Floorplanning can significantly impact chip performance**
  - Shielding can help timing and noise sensitive circuits
  - Carefully floorplanning critical paths can help reduce wire loads
  - Reducing clock routing can reduce clock skew and clock power

Eye candy: Floorplan examples

Apple A8 SOC (for iPhone)

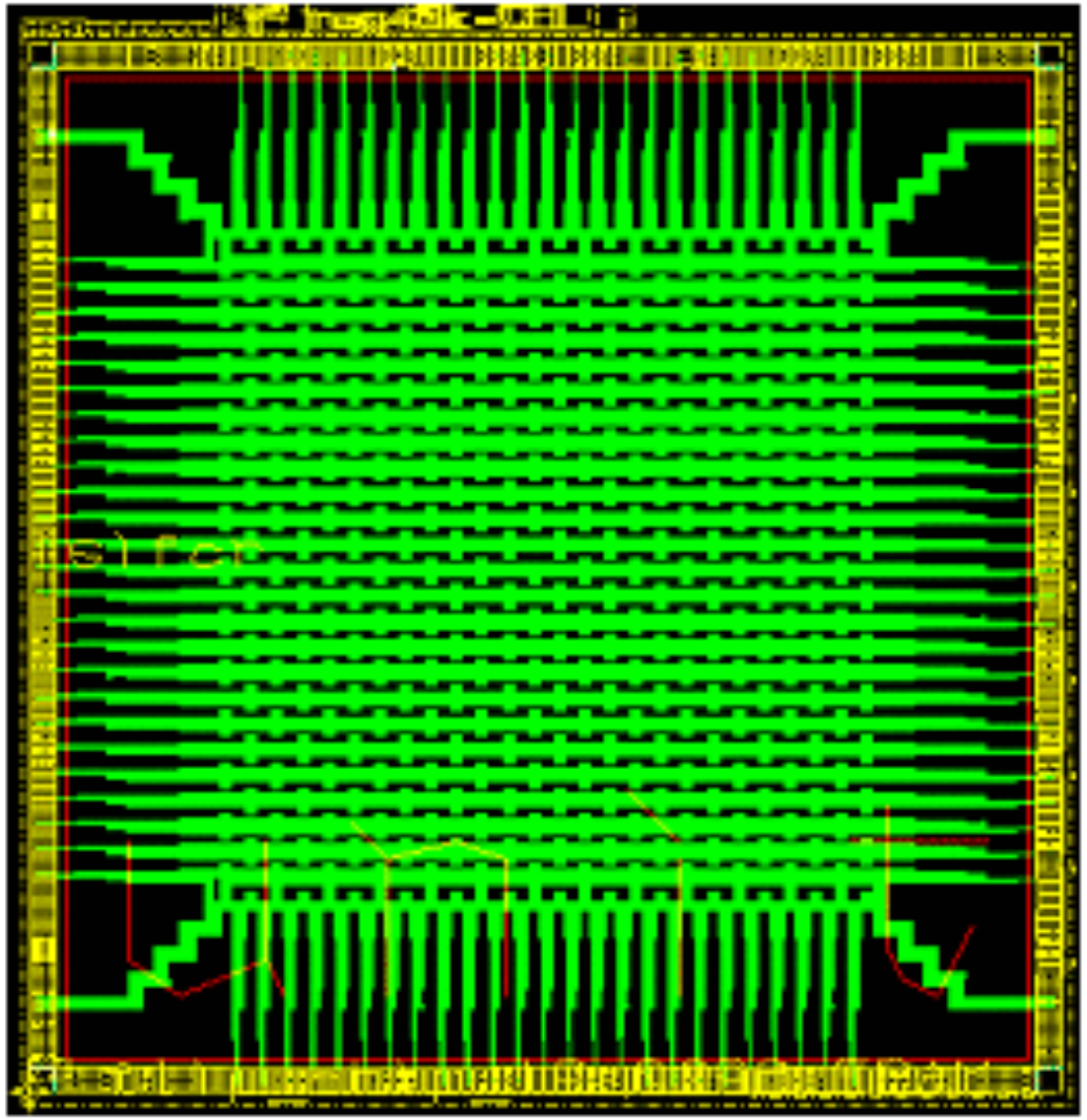


Apple A8X SOC (for iPAD)



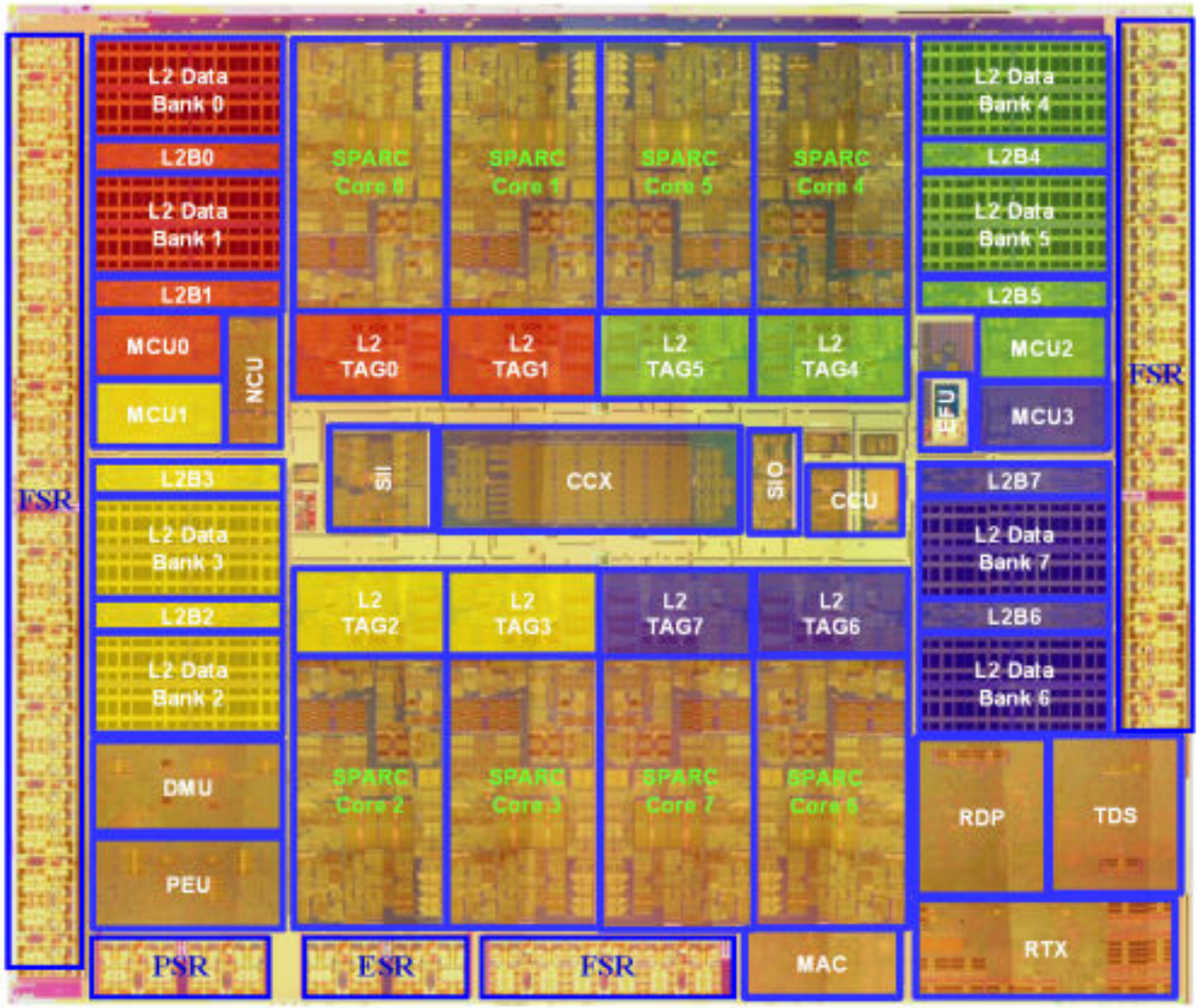
AMD Jaguar Floorplan

Flip chip power mesh for AMD Jaguar

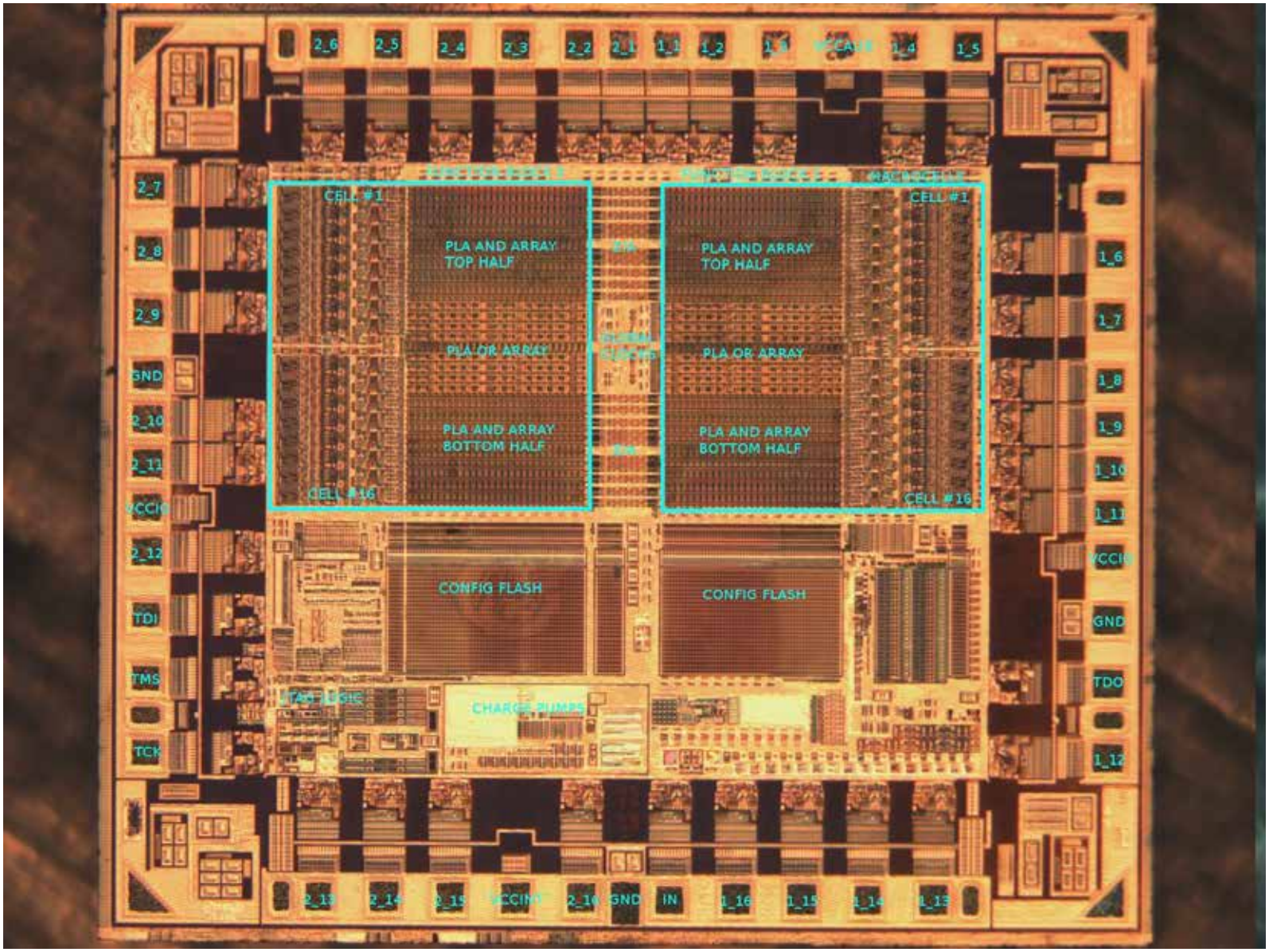


Flip-Chip
Power Mesh
(Top Layer)

SPARC Multicore Processor



Xilinx XC2C32A CPLD



Analog Devices LNA