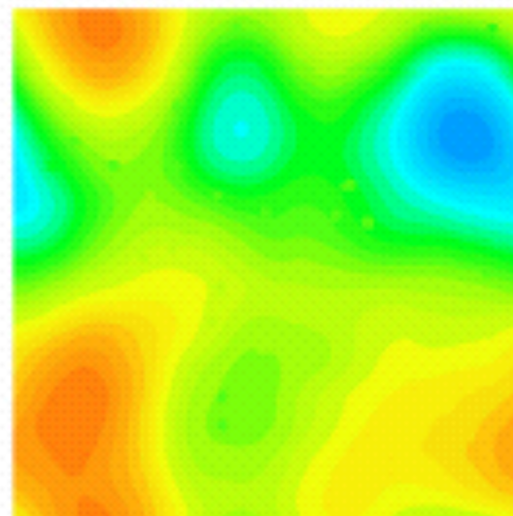
# EE-382M
# VLSI-II

## Variability Aware Design

## Spring 2017

Mark McDermott



**Statistical thinking will one day be as necessary for efficient (*chip-design*) citizenship as the ability to read and write.**

-- H. G. Wells

**There are three kinds of lies: lies, damned lies and statistics.**

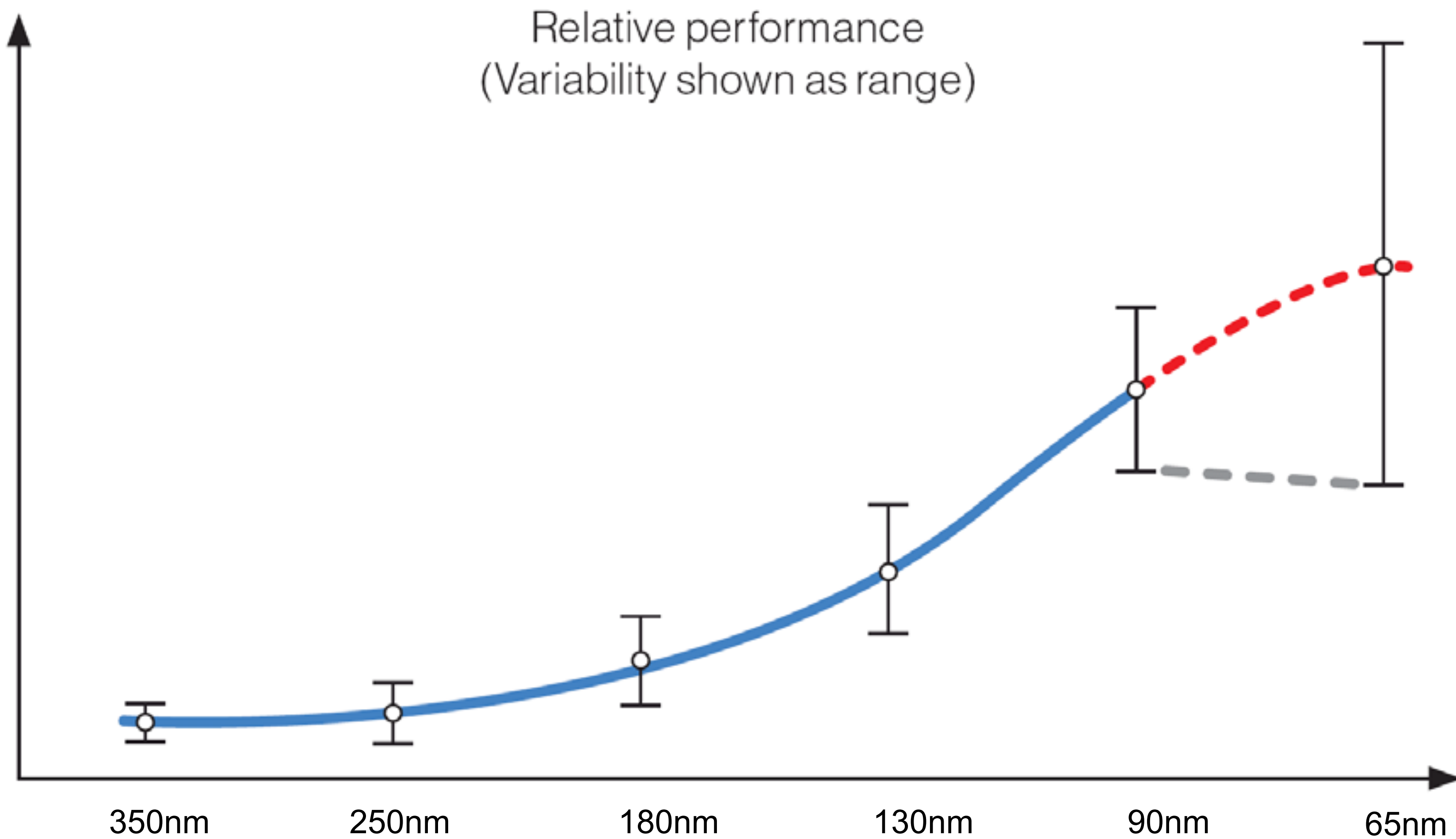
-- Disraeli

*From "How to Lie with Statistics," by Darrell Huff, Norton, 1954

**Statistics is like a bikini, what they reveal is suggestive, what they conceal is vital…**

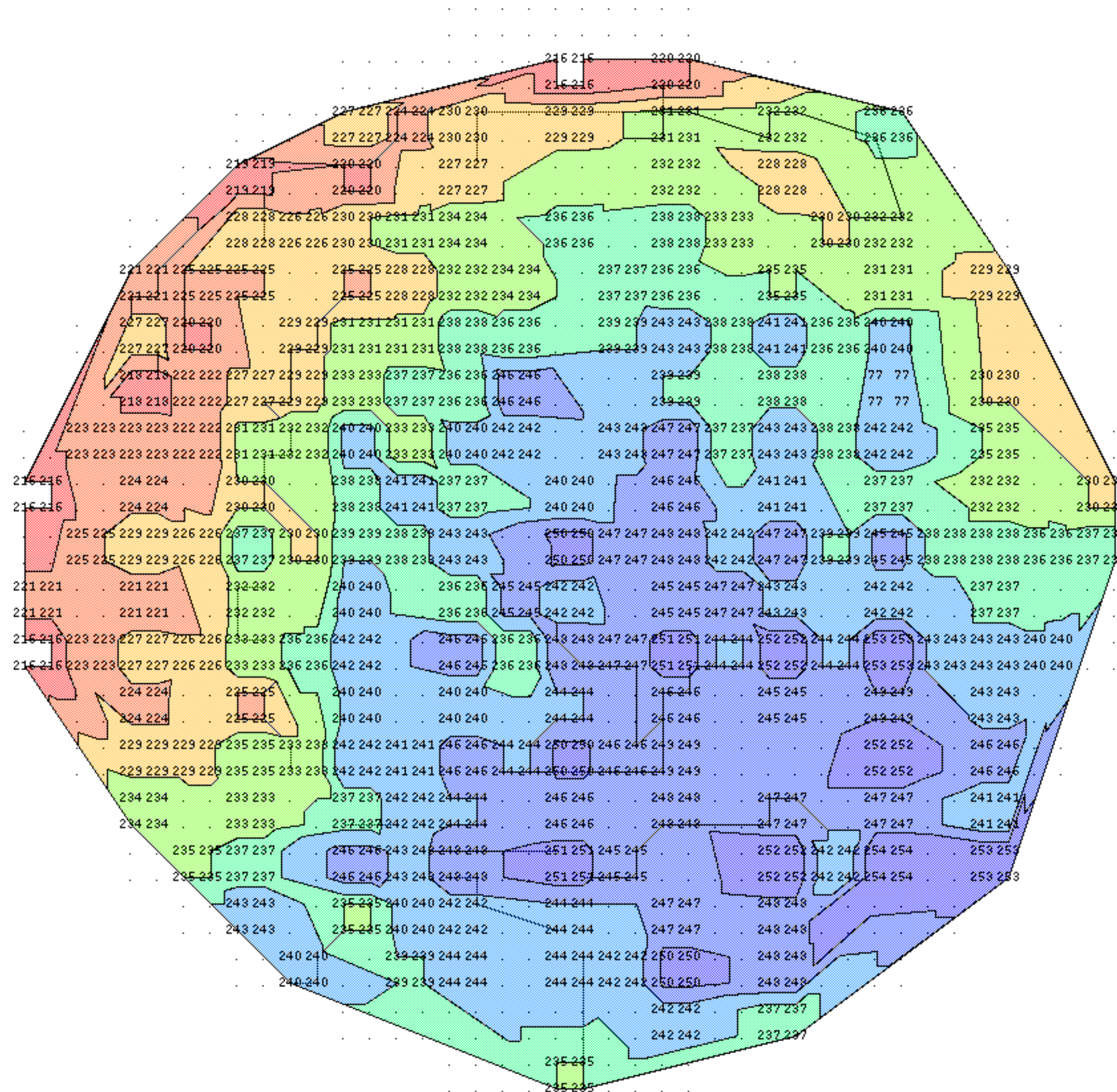
-- Aaron Levenstein

# Variability per technology node




Chandu Visweswariah, *IBM Thomas J. Watson Research Center*

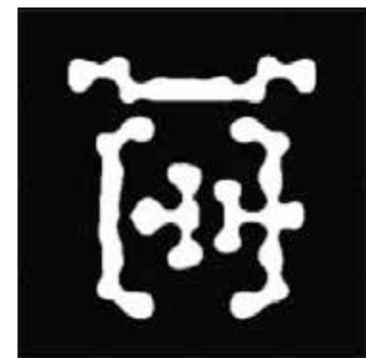
# Variation: Across-Wafer Critical Path Analysis



# Sources of variation

- **Process variations**
  - Ion implantation, photolithography, gate etch, thermal processing, tolerance in the size of the mask image, mask alignment, angle of the etched poly-silicon, temperature, polishing, planarization

- **Subtle layout dependencies**
  - Transistor orientation
  - Post OPC effects



- **Tool errors**
  - Gate delay model, waveform model, etc.
- **Human errors**
  - Designer overwriting the tool results

F. Dartu: Variation Impact on High Performance Circuits

# Types of variability

- **Global within a die/reticle**
  - metal dimensions
  - device family strength mistracking
  - ambient temperature and power supply
- **Spatial/local correlation across a die/reticle**
  - Leff
  - Junction temperature
  - VDD => voltage droop, voltage islands
- **Independently random**
  - Tox
  - Doping effects
  - Fatigue

Chandu Visweswariah, *IBM Thomas J. Watson Research Center*

# Motivation to worry about it…

- **Yield optimization**
  - Are enough parts in the profitable area?
- **Design functionality**
  - Will the design be DOA (races, etc.)?
- **Nominal performance**
  - Is our design/optimization well guided?
- **Design turn around**
  - Are we needlessly complicating the design?

F. Dartu: Variation Impact on High Performance Circuits

# Tool error vs. process variation

- **Both model uncertainties regarding the performance of the final product the final product**
  - **The process variation should be the only cause for yield spread**

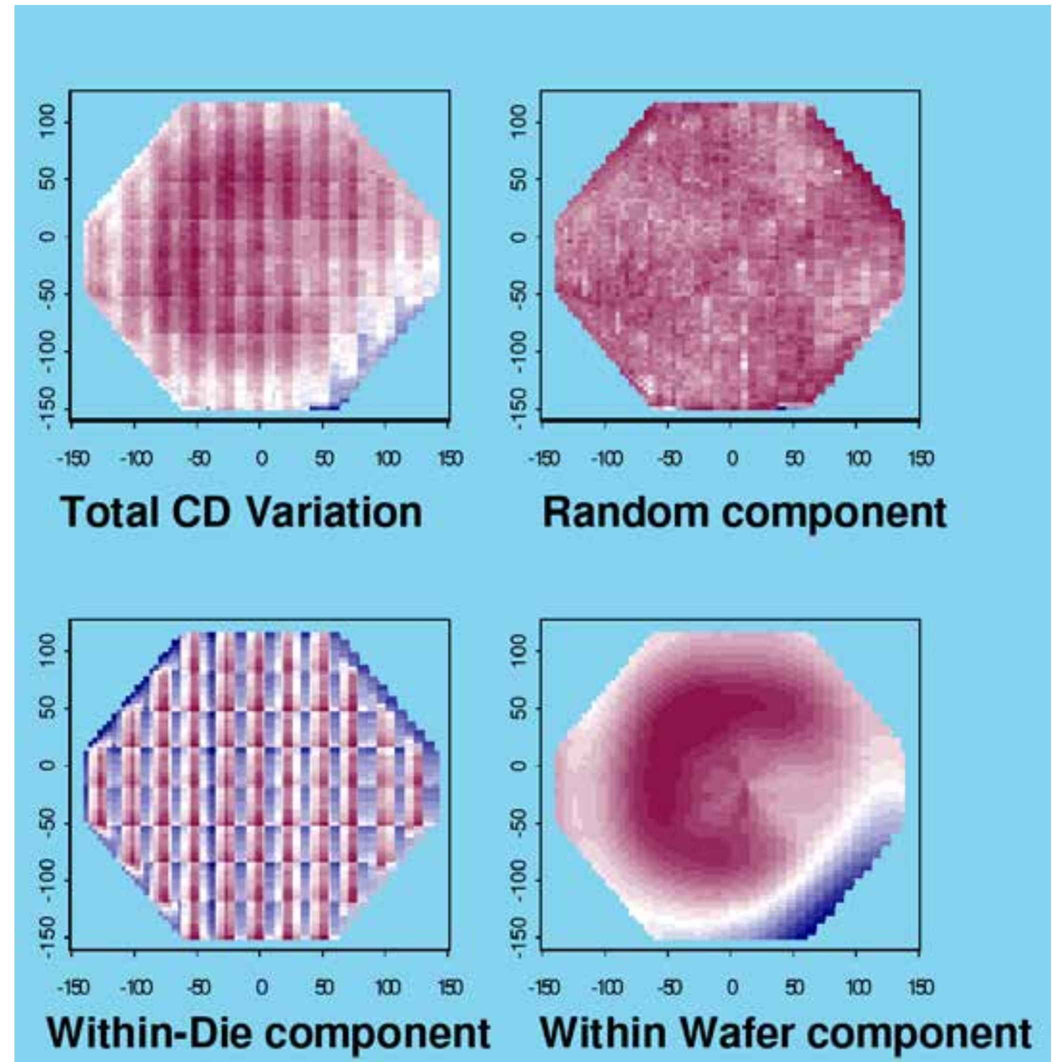
- **In reality there is a grey area**
  - **Layout dependant behavior:**
    - **Nested vs. isolated poly**
    - **Interconnect density**
  - **Environment dependant behavior:**
    - **Temperature**
    - **Power supply**

- **During the design, uncertainty influences the decision process, changing the average final performance**

F. Dartu: Variation Impact on High Performance Circuits

# Classification

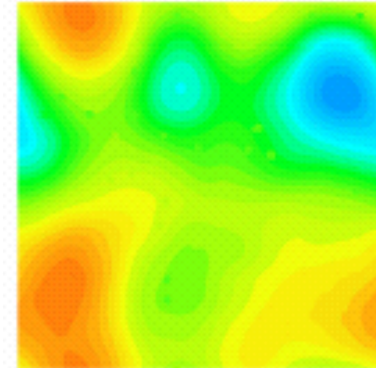
- **Electrical behavior**
  - Le
  - VT
  - Width
  - Interconnect
- **Spatial behavior**
  - Wafer to wafer
  - Die to die
  - Within die



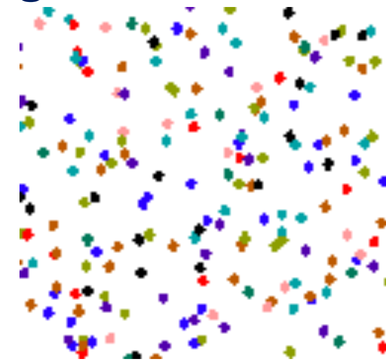

Source: Nagib Hakim, Intel Corp.

# Classification

- **Correlated**
  - Smooth and distance dependant
  - Examples: CD, COV, Metal R & C, Vdd, T
  - Known rate of change with distance

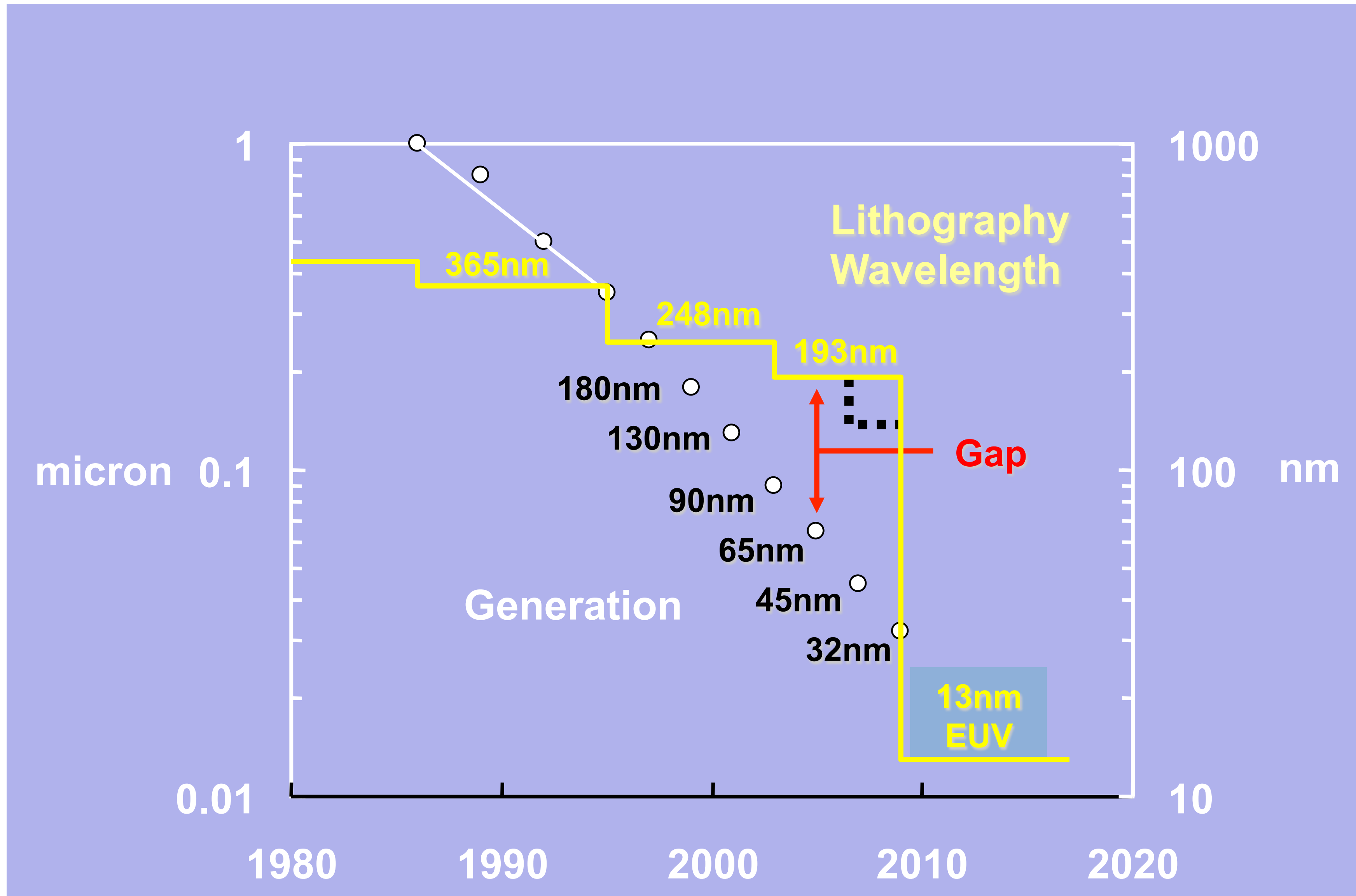


- **Random**
  - Looks like regular "white" noise
  - Distance independent
  - RDF (Vt), CD (LER), COV, NES / ISO poly.
  - During design: Tool inaccuracies, node coupling, designer error.

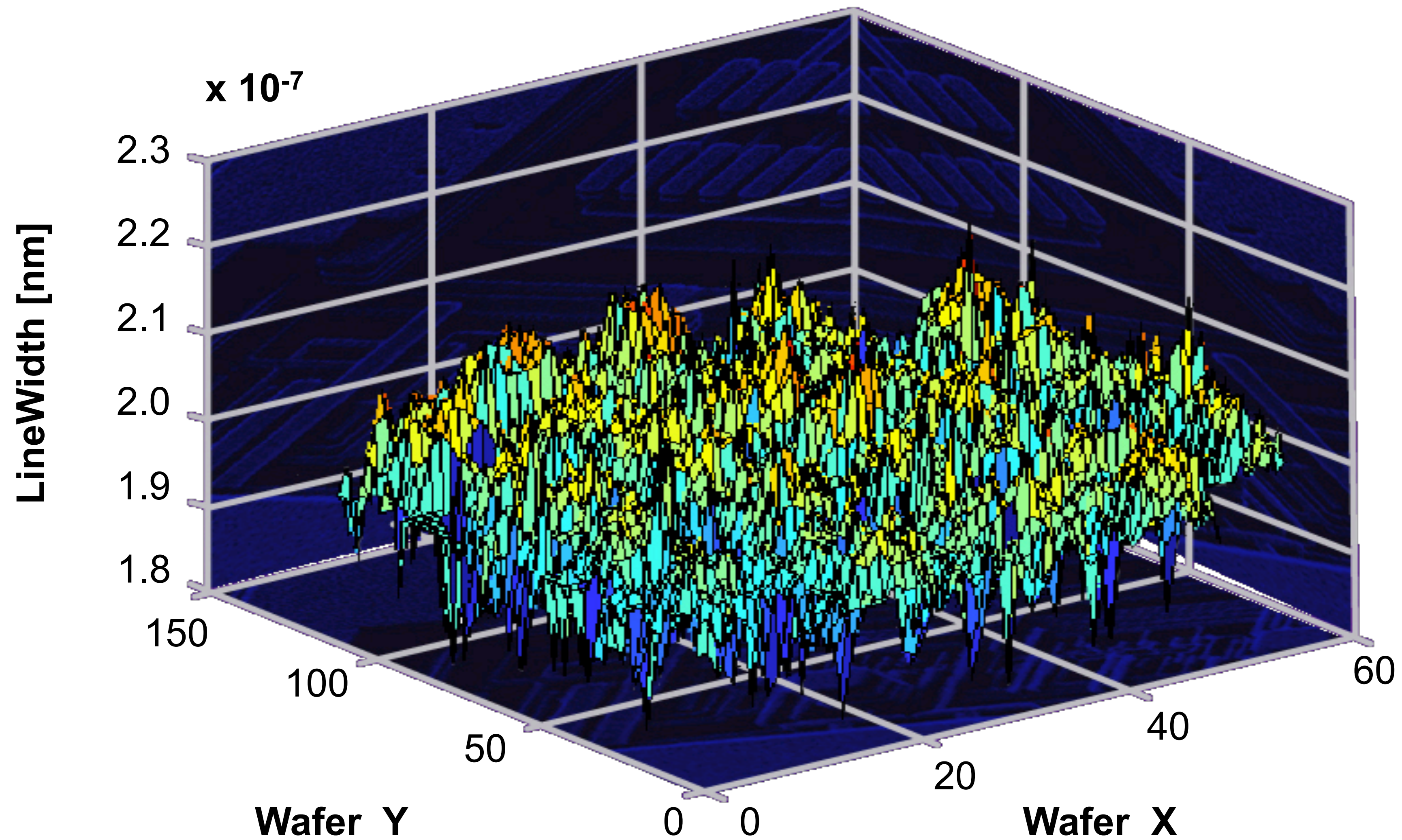


Source: Samie Samaan, Intel Co.

# Sub-wavelength Lithography Adds Variations



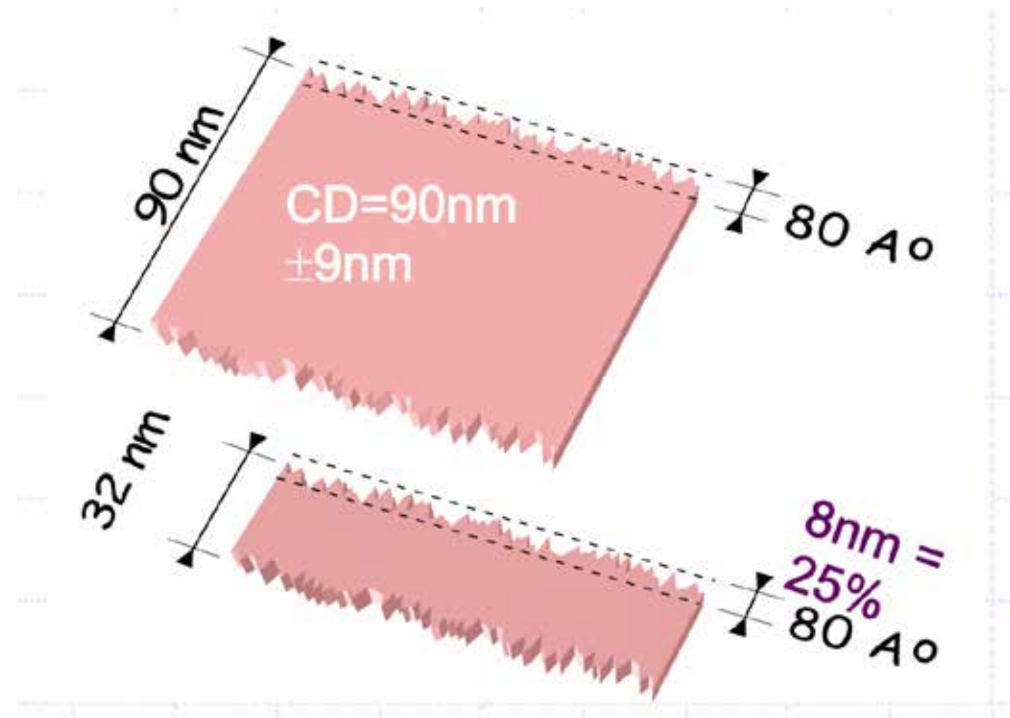
# CD Variation Across a Wafer




Source: Spanos, UCB

# Line Edge Roughness

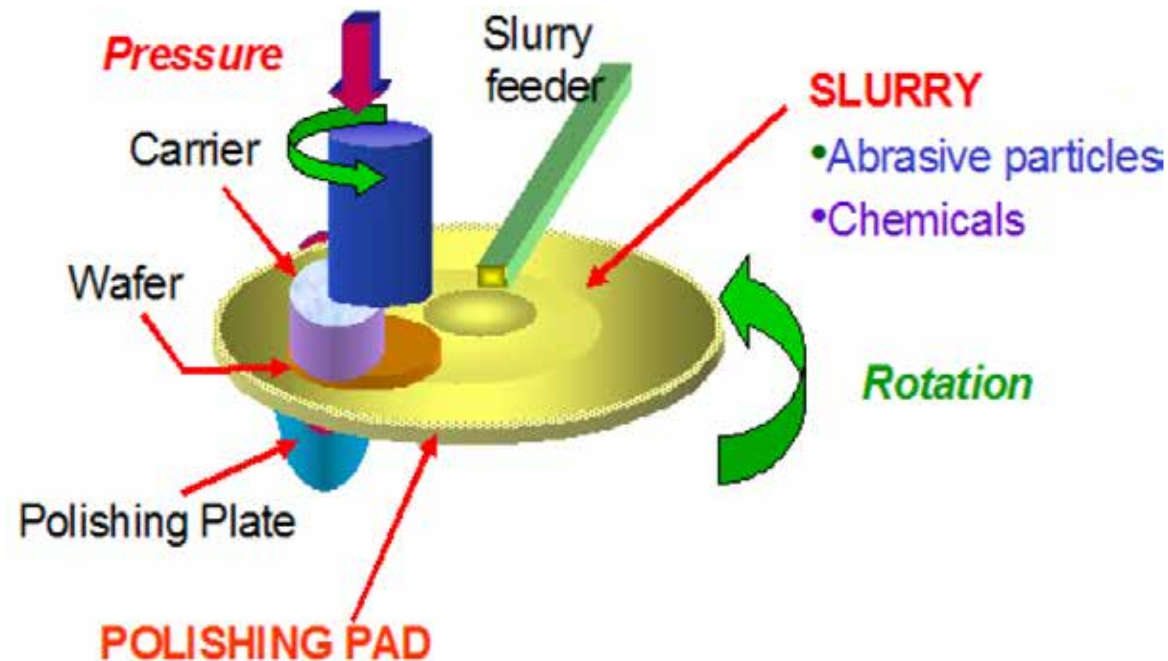
- Sources of line-edge variation
  - Fluctuations in the total dose due to finite number of quanta
    - Shot noise
- Fluctuations in the photon absorption positions
  - Nanoscale nonuniformities in the resist composition
- With decreasing feature size, a larger percentage of Lpoly has LER randomness
  - Impact delay and leakage power




Source: D. Frank, VLSI Tech 99

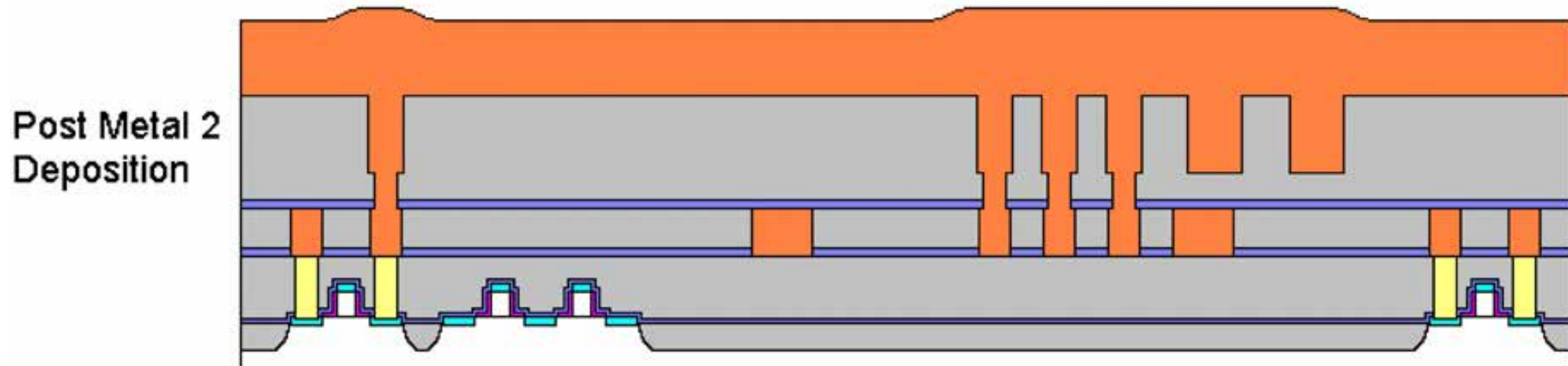
# Back End Variability - CMP

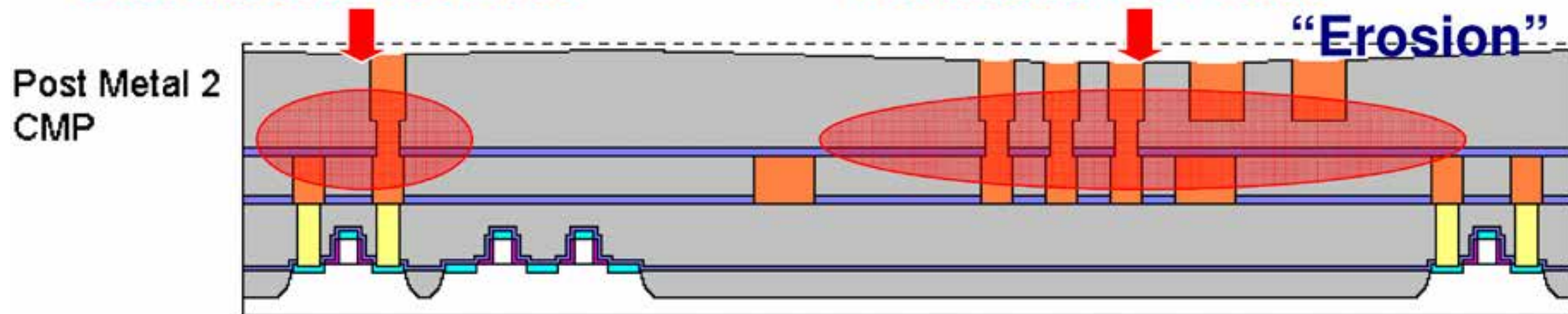
- Chemical-Mechanical Polishing (CMP)
  - Introduces large systematic intra-layer interconnect thickness
  - Additional inter-layer interconnect thickness effects as well




Source: Kevin Nowka, IBM Corporation

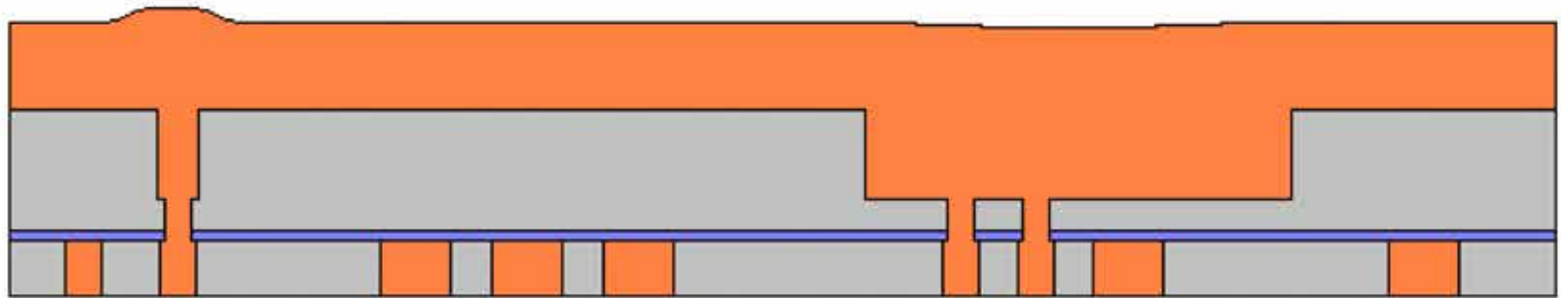
# Cu CMP and Metal Density



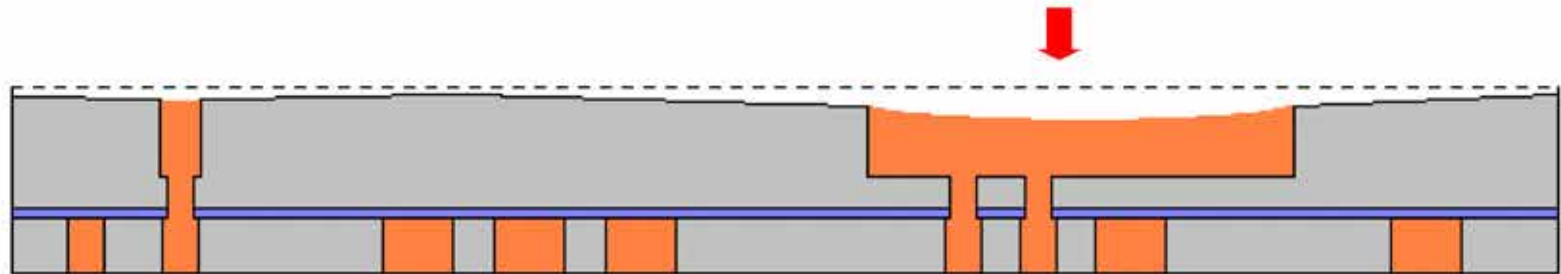




Source: Berni Landau, Intel Corporation

# Cu CMP and Metal Density




“Dishing” affects wider metal lines
-metal line cross-section is not rectangular

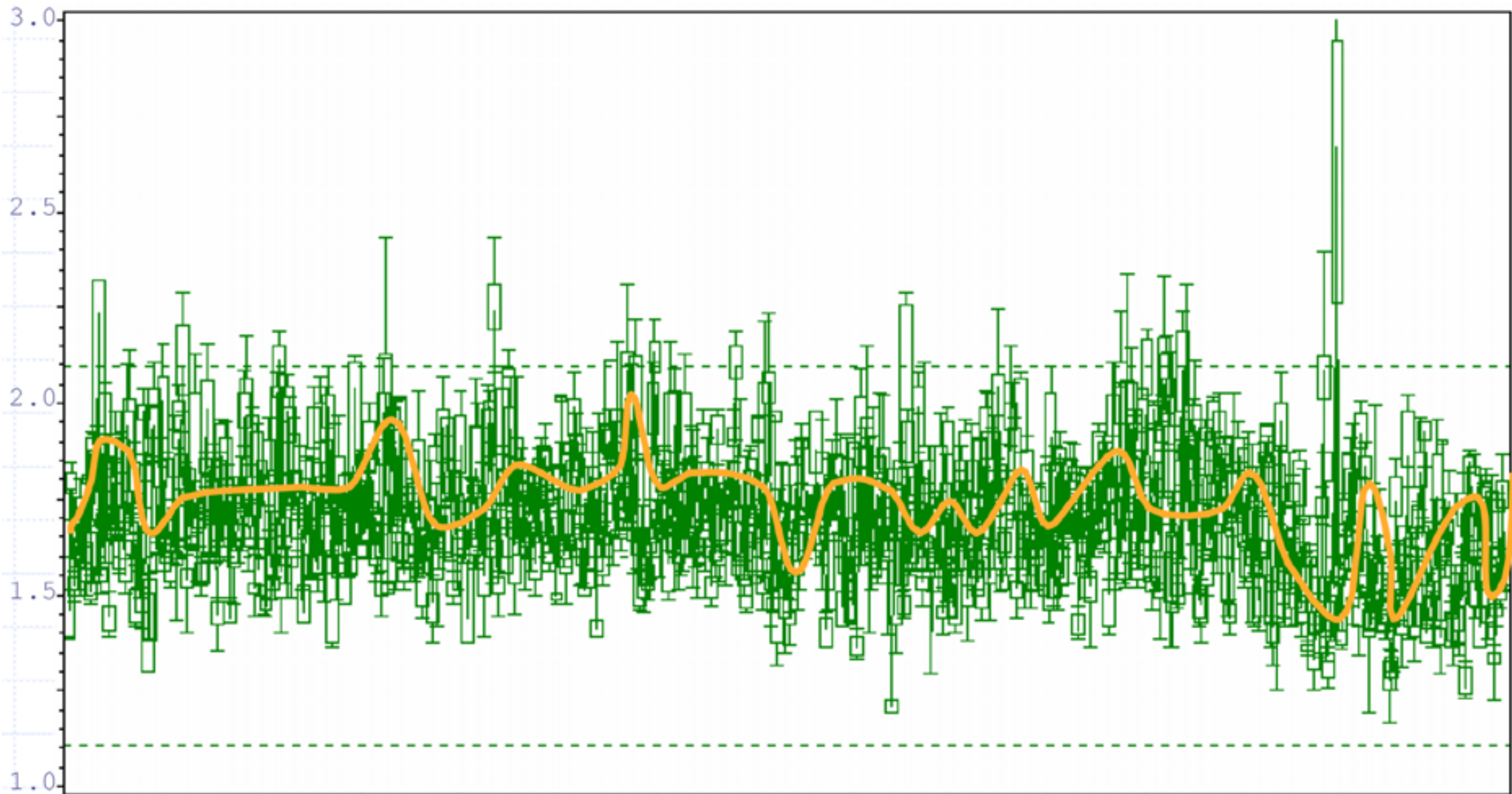



Source: Berni Landau, Intel Corporation

# Metal Fill

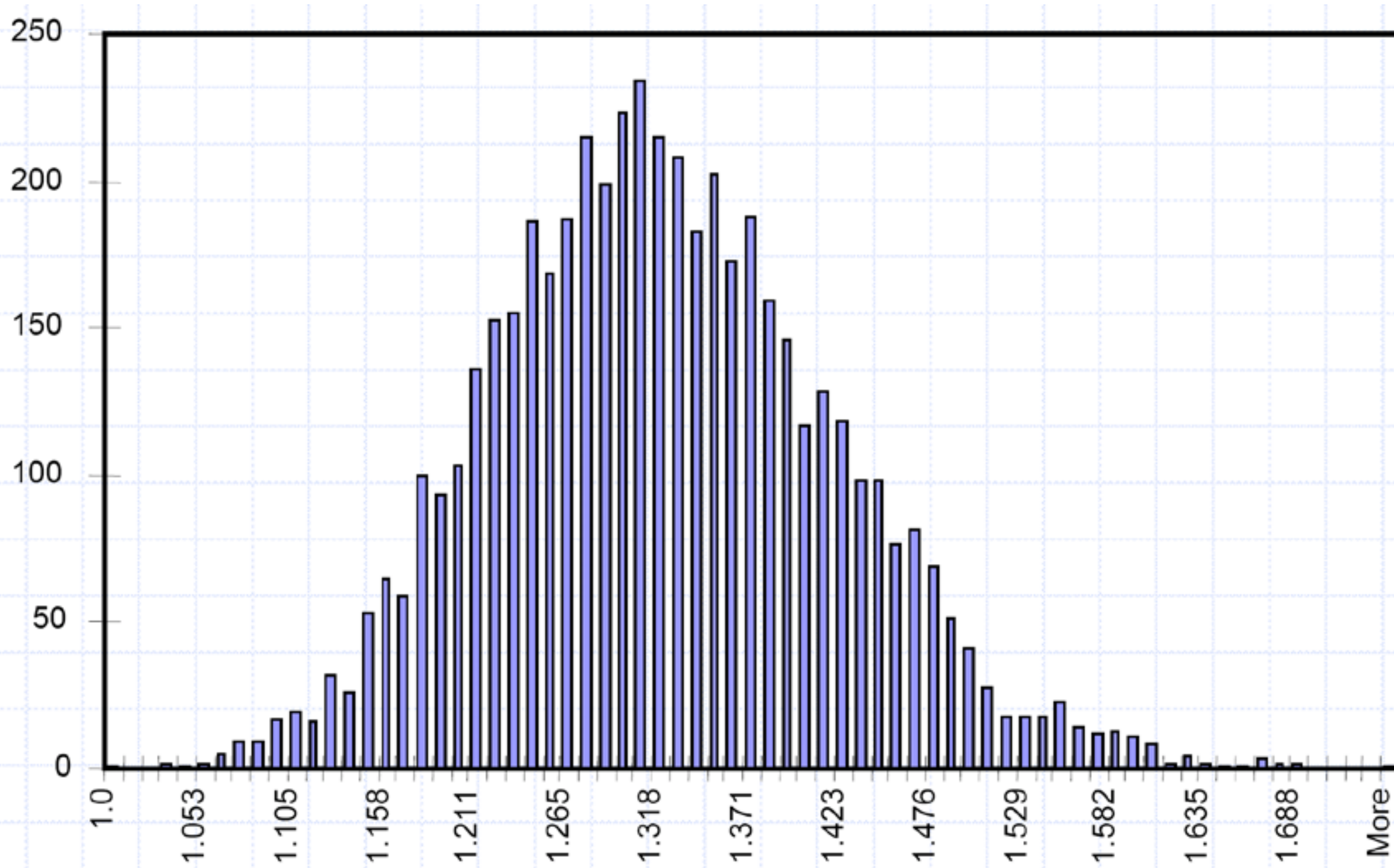
# Measured Variation: interconnect resistance

## Measured over three months.



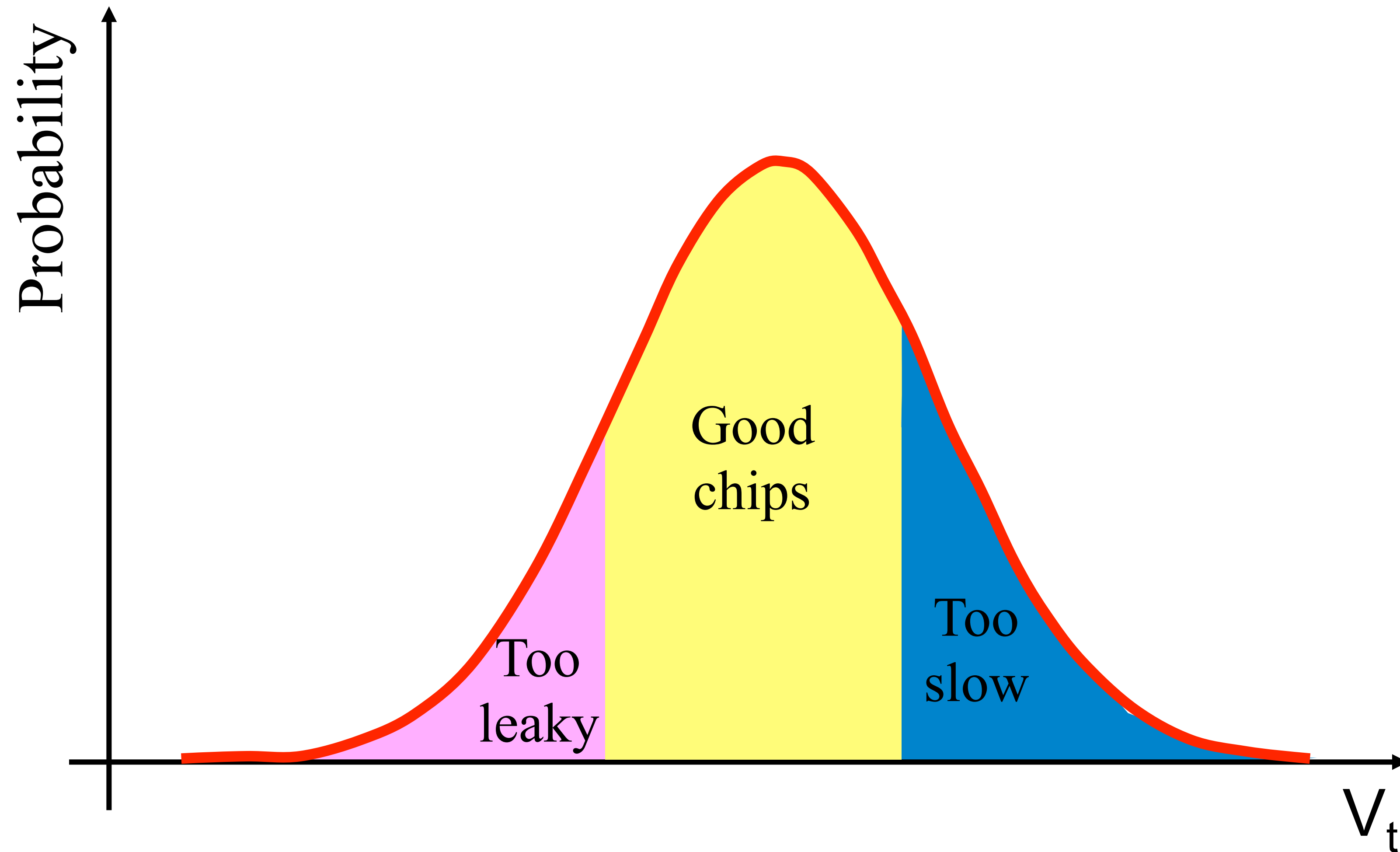

Source: Chandu Visweswariah, Kevin Nowka IBM

# Normalized single-level capacitance distribution



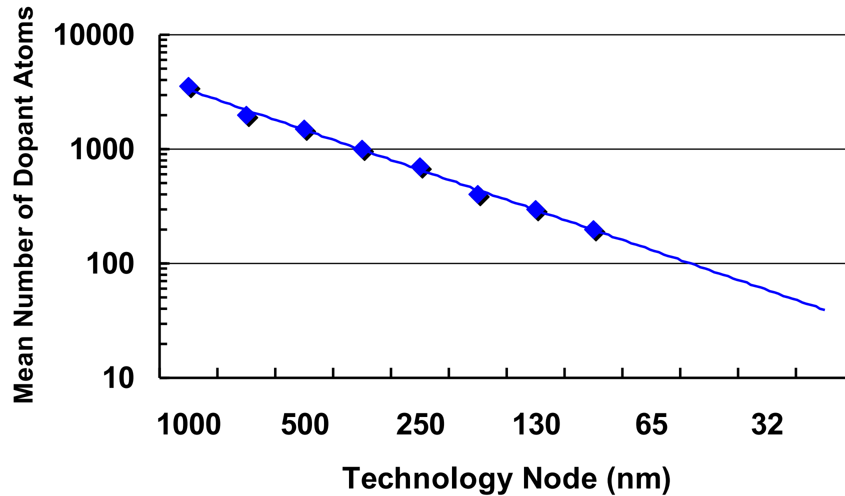

Source: Chandu Visweswariah, Kevin Nowka IBM

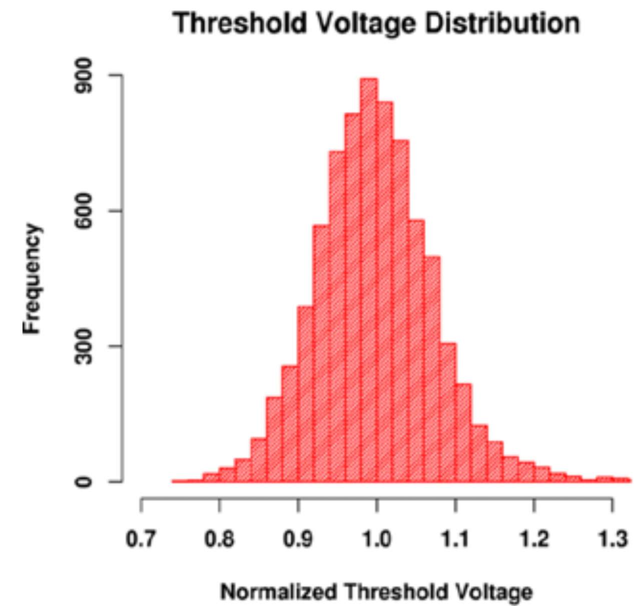
# Vt Variations

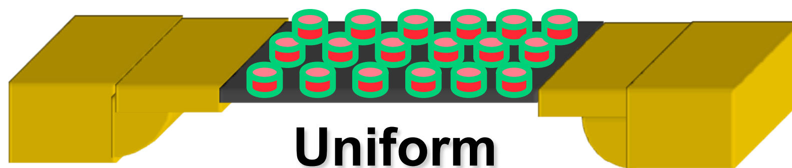



Chandu Visweswariah, *IBM Thomas J. Watson Research Center*

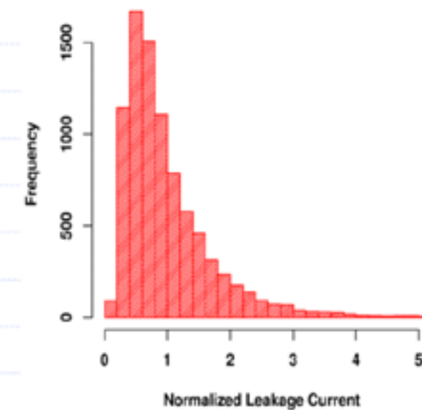
# Random Dopant Fluctuations

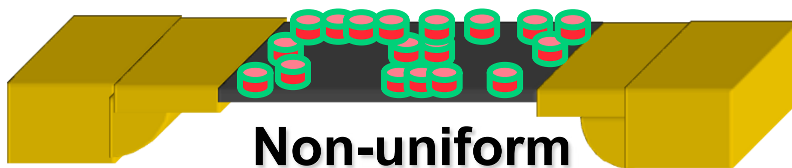



>200mV Vt Shift: ~100x leakage

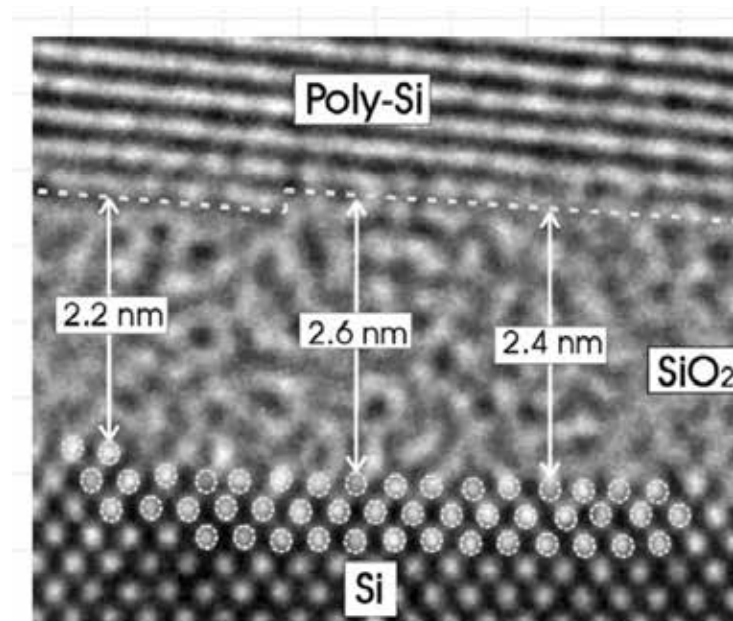



Source: K. Agarwal, VLSI 2006

# Gate Oxide Thickness Fluctuation

- **Gate oxide variation**
  - Exponential effect on gate tunneling currents
  - Affects device threshold, but significantly less important Vt variation factor than random-dopant fluctuation




Source: Kevin Nowka, IBM Corporation

# NBTI and Hot-carrier-induced Variation

UT ECE

- **Negative Bias Temperature Instability**
  - At high negative bias and elevated temperature the pFET Vt gradually shifts more and more negative (reducing the pFET current).
    - The mechanism is thought to be the breaking of hydrogen-silicon bonds at the Si/SiO2 interface, creating surface traps and injecting positive hydrogen-related species into the oxide.
    - Associated with the average NBTI shift, there are also random shifts, which even for identical use conditions and devices, will cause mismatch shifts due to random variations in the number and spatial distribution of the charges/interface states formed.
- **There are also other charge trapping and hot-carrier defect generation mechanisms that cause long-term Vt shifts in both nFETs and pFETs.**
- **Long-term Vt shifts are parameter variations that must be accounted for in the design of circuits.**

Source: N. Rohrer, ISSCC 2006

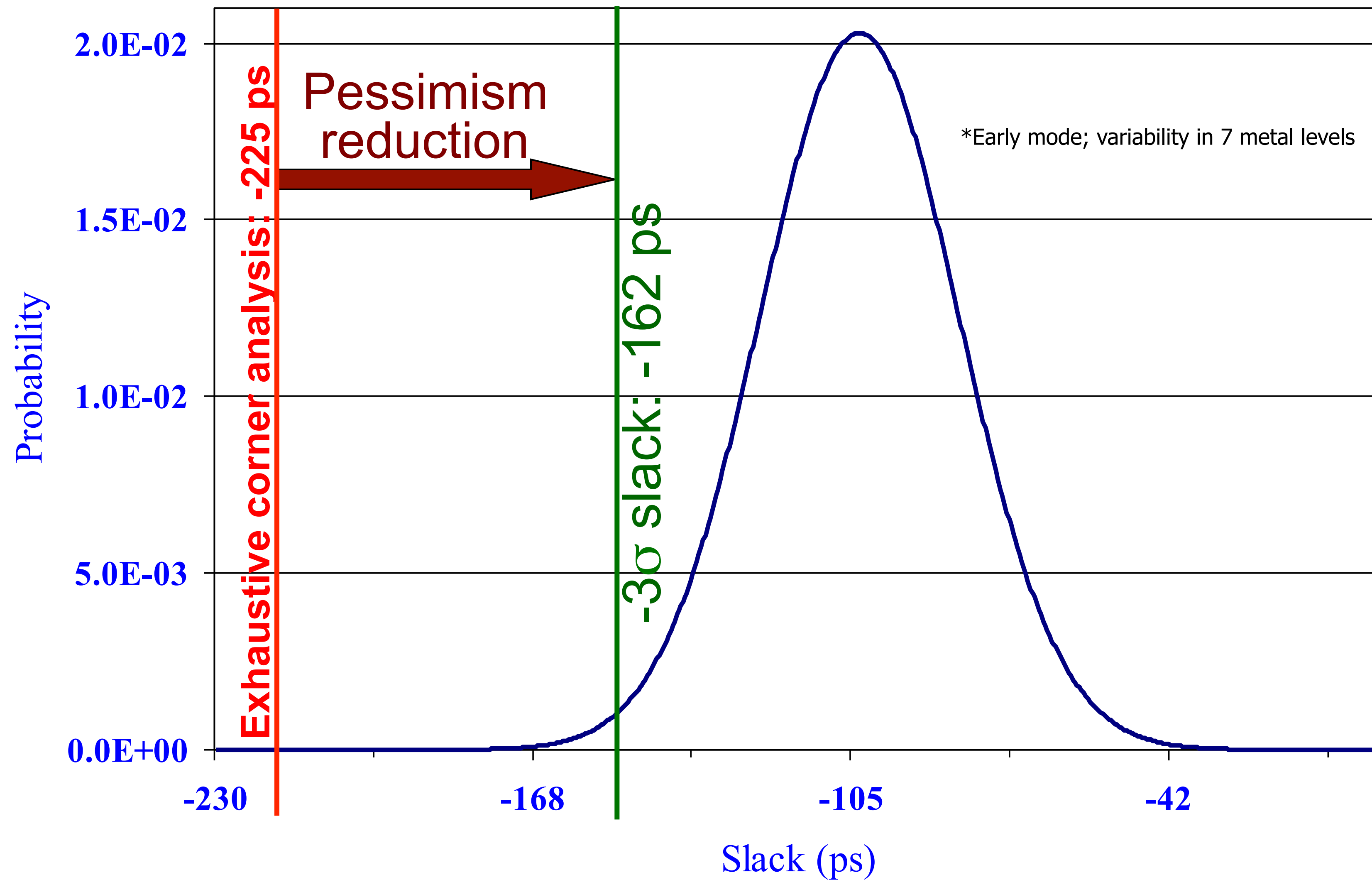
# Delay impact of variations

| ***Parameter*** | ***Delay Impact*** |
|---|---|
| **BEOL metal**<br>**(Metal mistrack, thin/thick wires)** | **-10% → +25%** |
| **Environmental**<br>**(Voltage islands, IR drop, temperature)** | **±15 %** |
| **Device fatigue (NBTI, hot electron effects)** | **±10%** |
| **$V_t$ and $T_{ox}$ device family tracking**<br>**(Can have multiple $V_t$ and $T_{ox}$ device families)** | **± 5%** |
| **Model/hardware uncertainty**<br>**(Per cell type)** | **± 5%** |
| **N/P mistrack**<br>**(Fast rise/slow fall, fast fall/slow rise)** | **±10%** |
| **Clocking: PLL & DLL,**<br>**(Jitter, duty cycle, phase error)** | **±10%** |

Source: Kerim Kalafala IBM

**Requires $2^{20}$ timing runs**

# BEOL early-mode variability



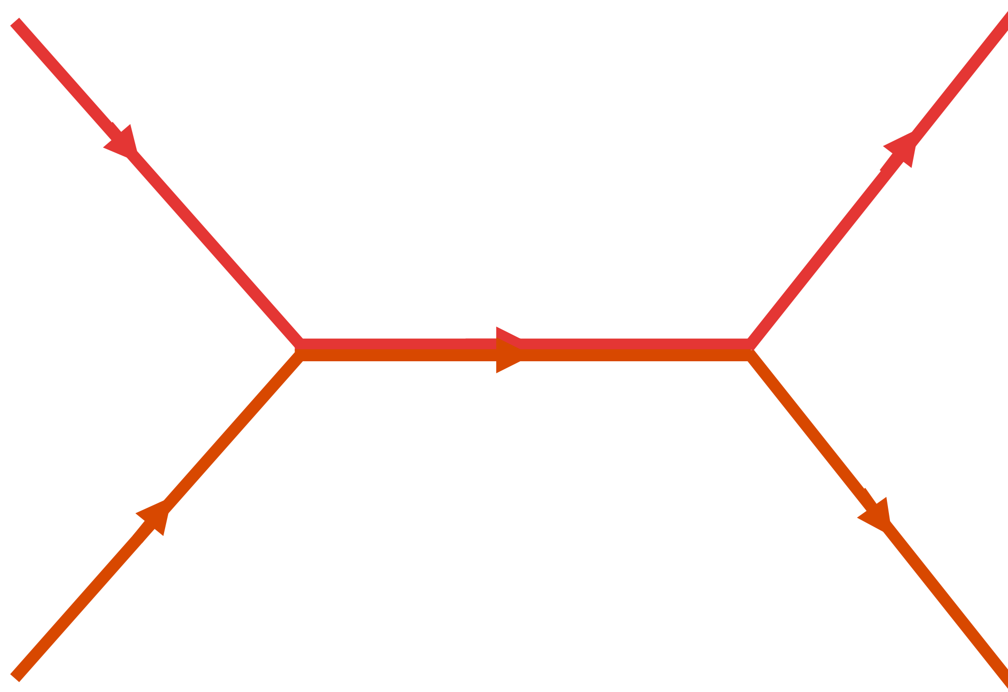

Chandu Visweswariah, *IBM Thomas J. Watson Research Center*

# Importance of correlation

- **Consider a circuit with 50K latches, each with a setup and hold test, each of which has a 99.99% probability of being met**
  - If all tests are perfectly correlated,
    yield = 99.99%
  - If all tests are perfectly independent,
    yield = 0.005%
  - The truth is closer to the perfectly correlated case!
- **Delay variation:**
  - Correlated: gates, wires, and paths become slower or faster simultaneously
  - Un-correlated: some gates or wires are faster, others on the same chip slower
- **Correlated delay variation happens if**
  - Only inter-chip variation is present, *and*
  - Sensitivities of gate / wire delays to process variation are the same

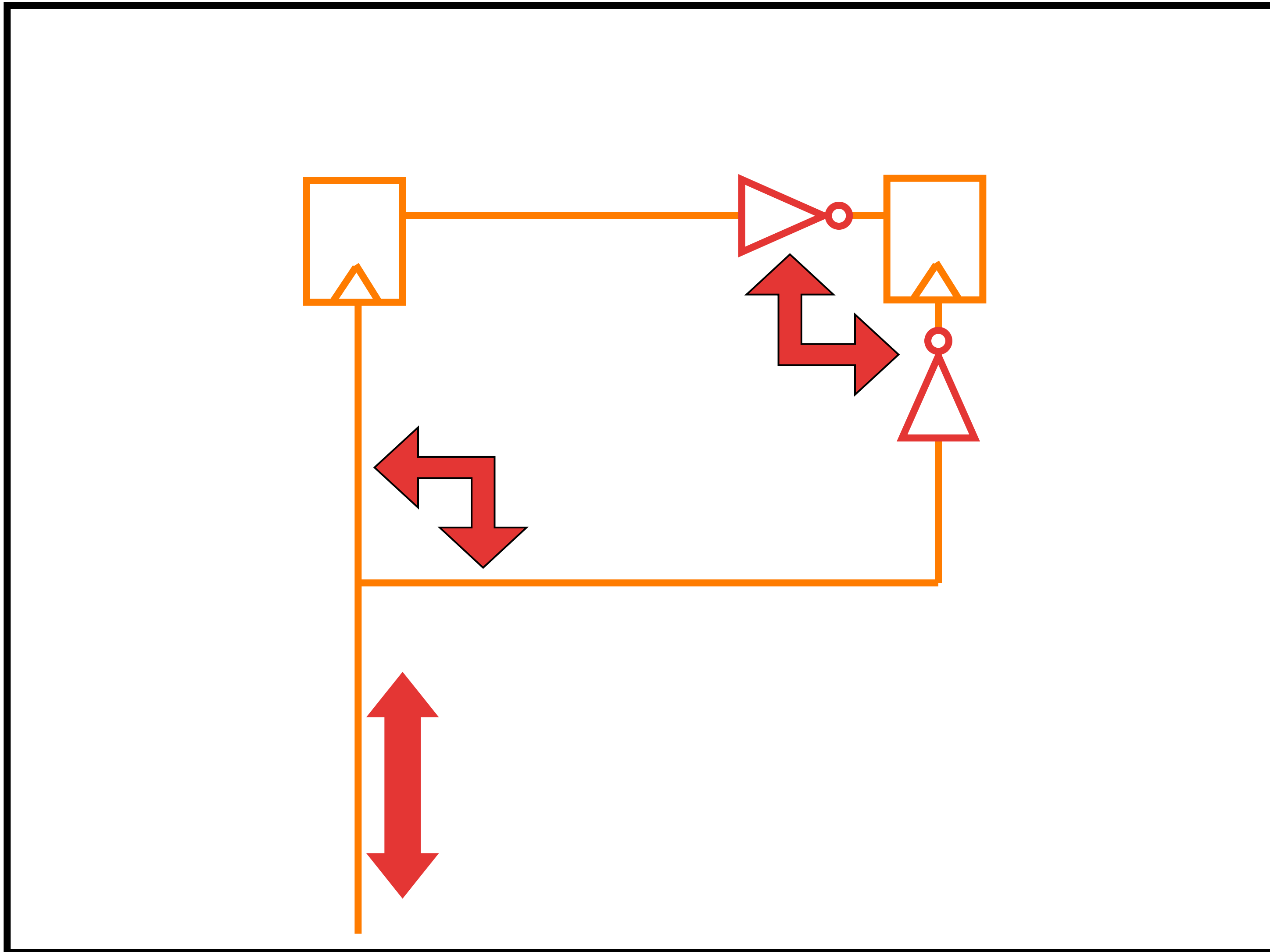
Chandu Visweswariah, *IBM Thomas J. Watson Research Center*

# Correlation due to path sharing



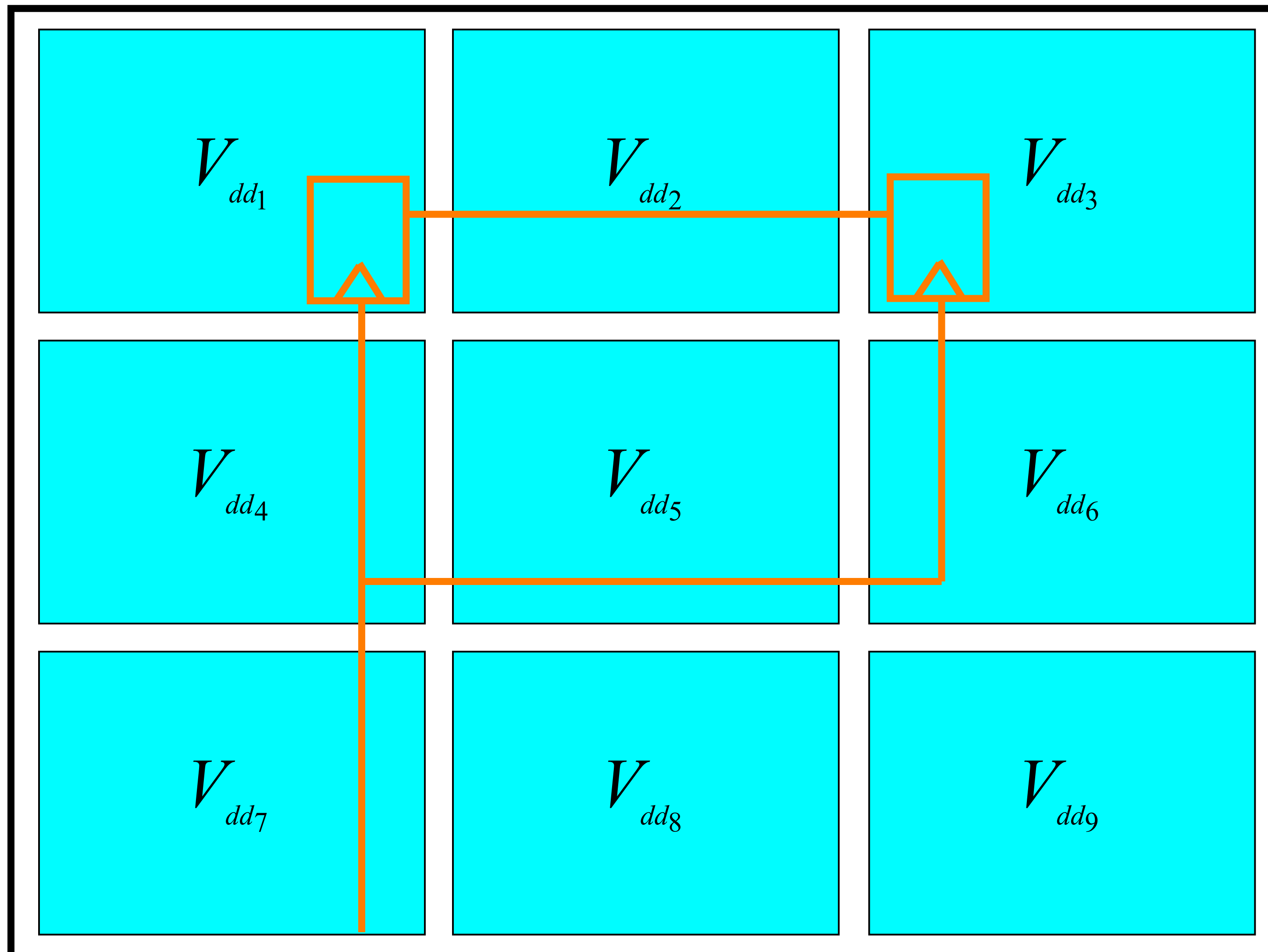
Chandu Visweswariah, *IBM Thomas J. Watson Research Center*

# Clock and cell-type correlation



Chandu Visweswariah, *IBM Thomas J. Watson Research Center*

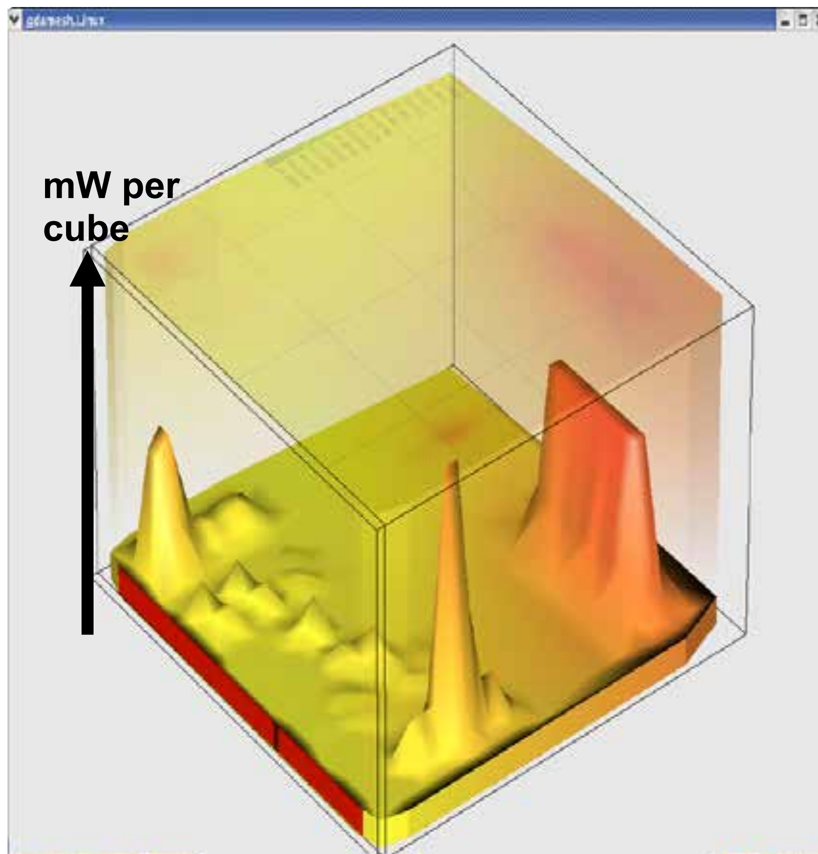
# Voltage correlation



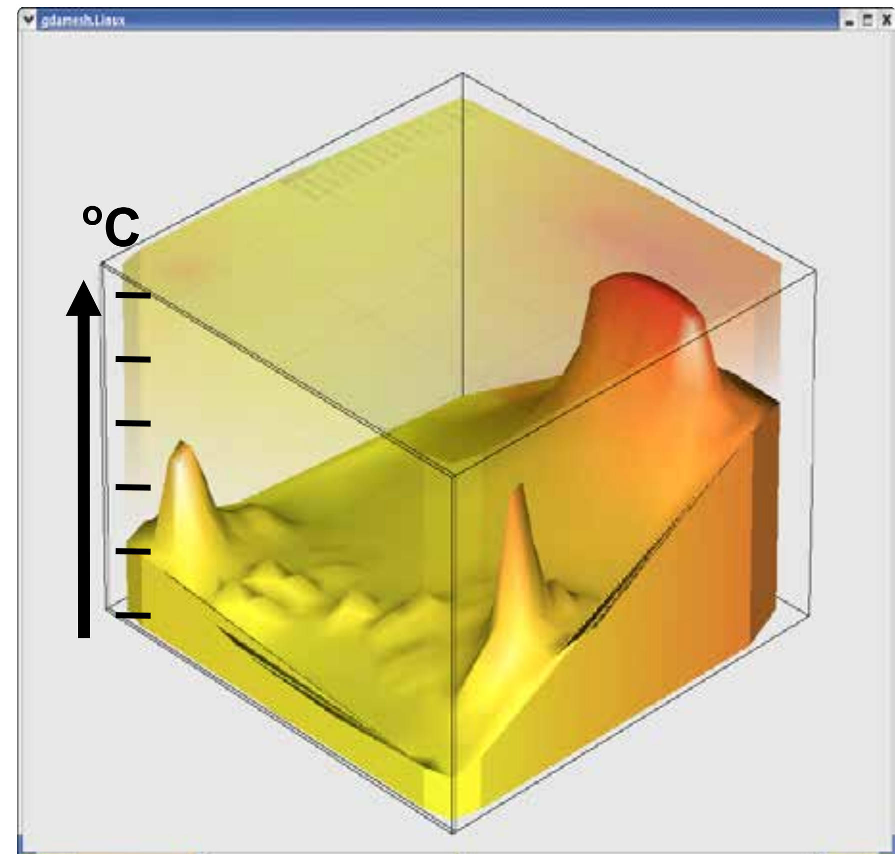

Chandu Visweswariah, *IBM Thomas J. Watson Research Center*

# Temperature/Power/$V_{dd}$ correlation

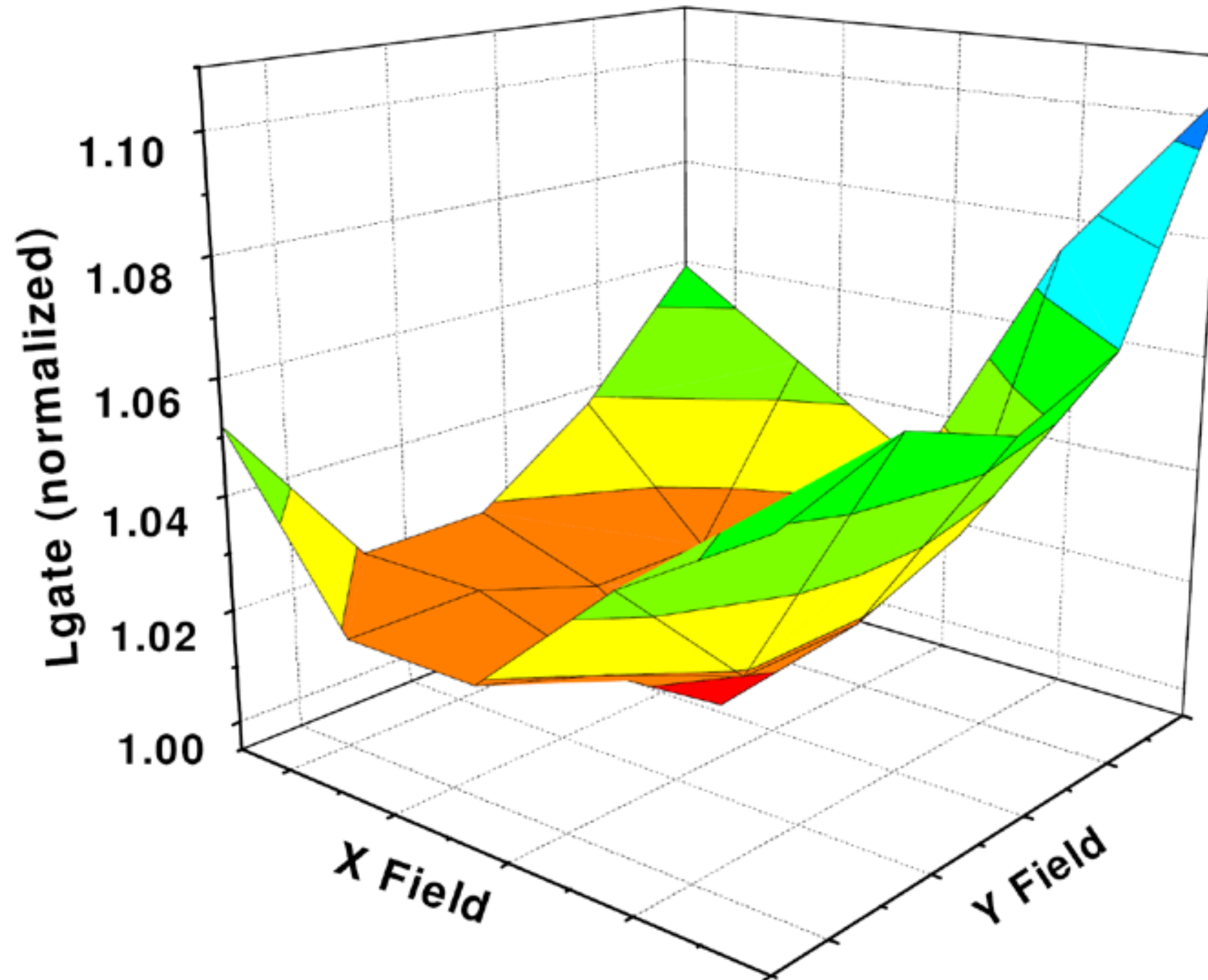
## Power




## Temperature



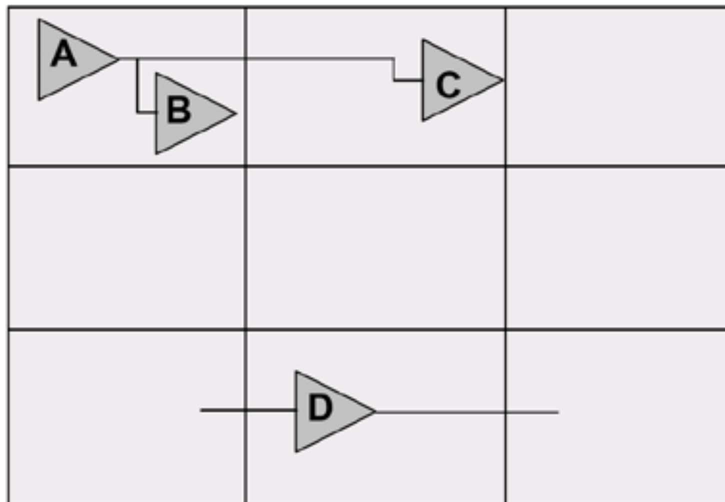
# Geographical (Spatial) correlation




[From M. Orshansky, L. Milor, P. Chen, K. Keutzer, C. Hu, ICCAD 2000]

# Spatial Correlation Modeling

- **A hierarchical grid-based approach is used to divide the chip area into n grid regions**

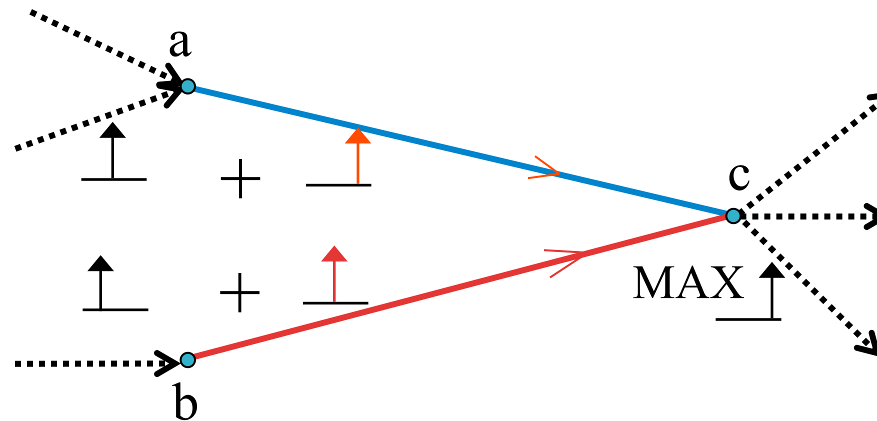



$$\mathrm{corr}(L_A, L_B) = 1$$
$$\mathrm{corr}(L_A, L_C) < 1$$
$$\mathrm{corr}(L_A, L_D) = 0$$

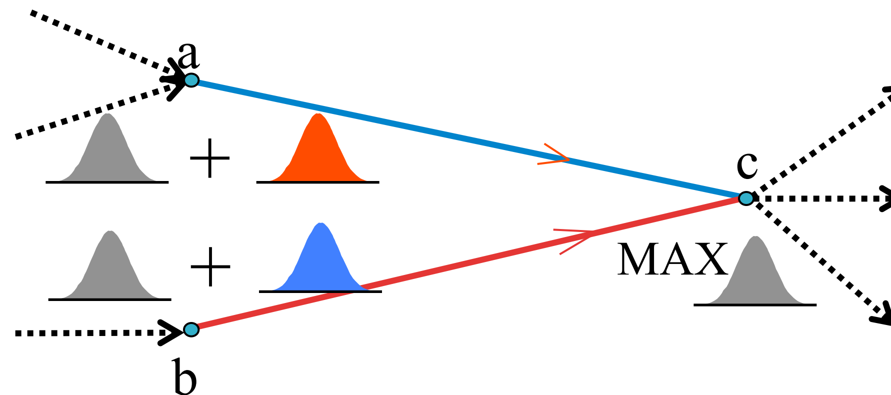
Source: Mustafa Celik, *Extreme-DA*

# STA vs. SSTA

- **Deterministic**




- **Statistical**




Chandu Visweswariah, *IBM Thomas J. Watson Research Center*

# Design for Correlation (DFC)

- **Two sources of information for statistical models:**
  - Process control & component testing
- **A lot of important correlation factors are design dependent.**
  - How do you extract these factors from a design?
- **Maybe we should call it Instrumentation for Correlation…**
- **Who drives DFC?**

# Summary

- Variability is proportionately increasing (getting worse)
  - Variation sensitivities matter
  - More design rules, more 2nd order effects, more systematic variations, more correction steps
  - Current techniques are insufficient
    - Abstractions no longer good enough
    - Predictability is poor
    - Ability to confidently bound performance is degrading.
    - Frequent model/hardware mismatch.
- Correlation is extremely important
  - global/systematic
  - spatial
  - independently random
- Robustness & resiliency are the key metrics for designs at 65nm and below

# BACKUP

# Variation-Aware Library Models

- **Each capacitance or delay value replaced by (μ,σ) pair**
- **Variation aware .lib**