EE-382M
VLSI–II
FLIP-FLOPS
Spring 2017

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OUTLINE

- Motivation to work on Sequentials
- LATCH Operation
- FLOP Timing Diagrams & Characterization
- Transfer-Gate Master-Slave FLIP-FLOP
- Merged Functions
- Clock Skew
- Other Topologies
- SCAN
- Simple Clock Division Using FLOPs
- References

MOTIVATION

- **Trends in high-performance systems**
  - Higher clock frequency leads to …..
  - Deeper pipelines or more ***parallelism*** leads to ….
  - More transistors which leads to ….
  - More sequentials (FLOP or LATCH) which leads to ….
- **Consequences**
  - Increased flip-flop overhead
    - Cycle time in 12 to 15 stage pipeline micro-Architectures is about ~22 FO4 delays
    - FLOP overhead ~3 FO4 delay (D-Q delay) ~12% (3/25)
  - Clock uncertainty (jitter & skew) also affects cycle time
  - Clock power

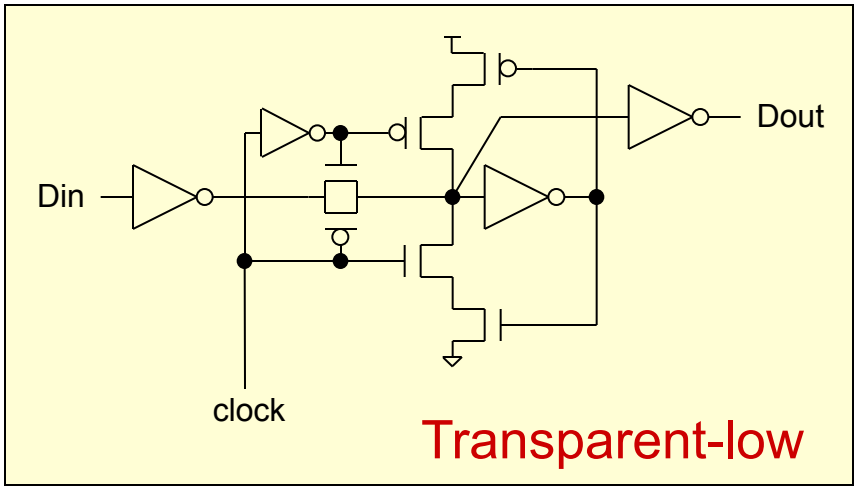
Why work on Sequentials ?

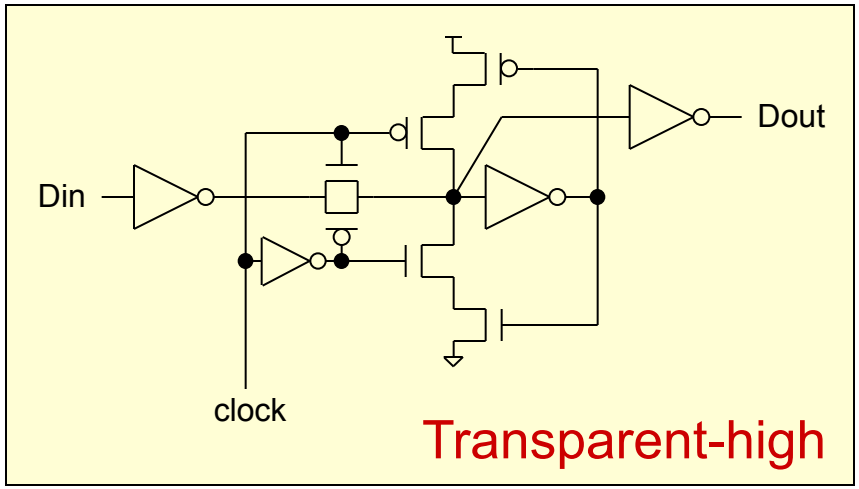
In a 2.5 GHz processor (32nm CMOS) cycle=400pS

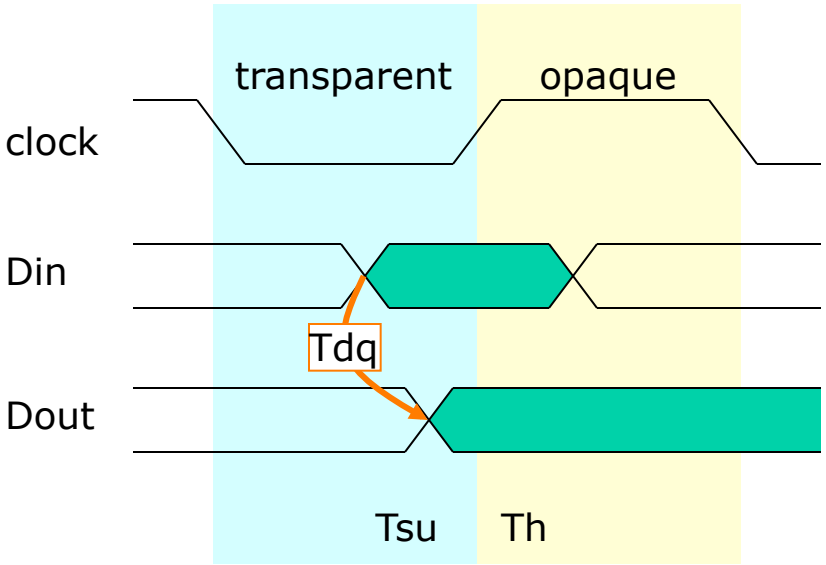
- Typical D-Q delay (FO4) is ~50ps.
- If one can design a faster sequential, say D-Q delay of ~25pS, this can be used to increase *processor* performance by ~6.8% (cycle can be reduced to 375ps or 2.67GHz).
- If in ***addition*** one can absorb 20ps of clock uncertainties and/or embed one level of logic, this will lead to an overall 12.8% *processor* performance improvement (CPU cycle can be reduced to 355ps or 2.82GHz).

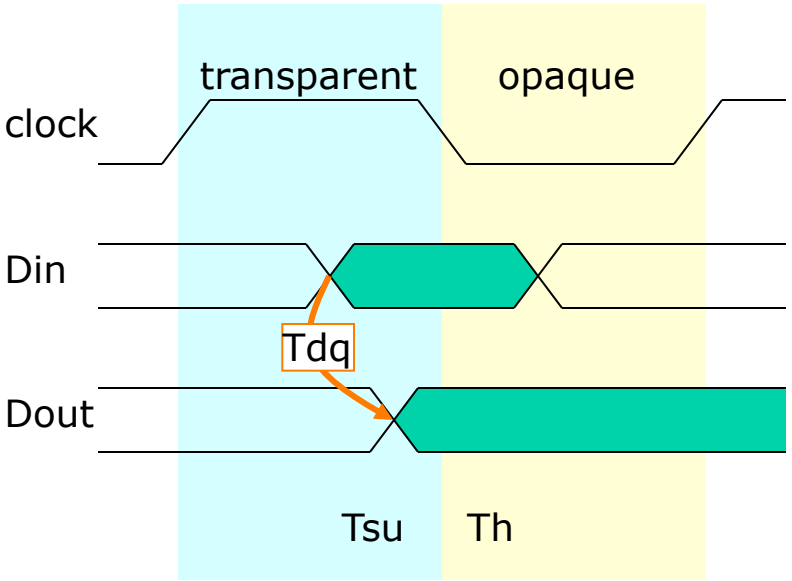
- *Attaining ~13% performance improvement via architecture enhancements is very expensive (area, power, complexity)!*

Basic LATCH Operation

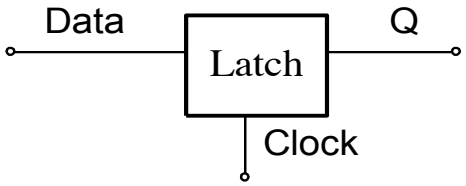




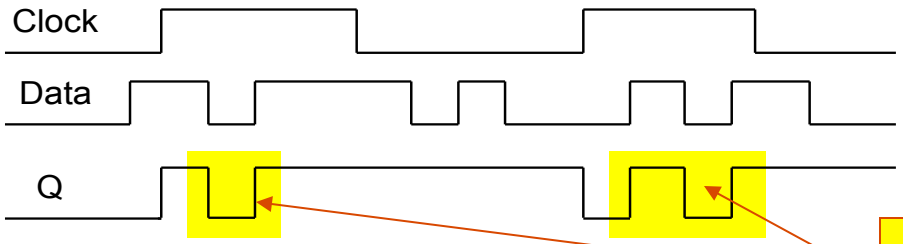




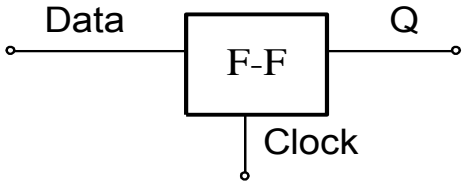
Difference between a LATCH and a FLOP



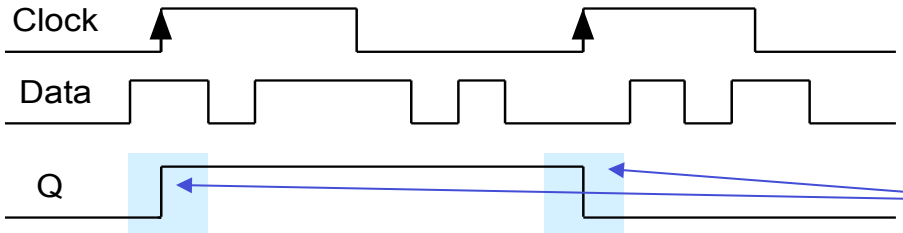
Transparent / Opaque



Q 'follow's the input DATA

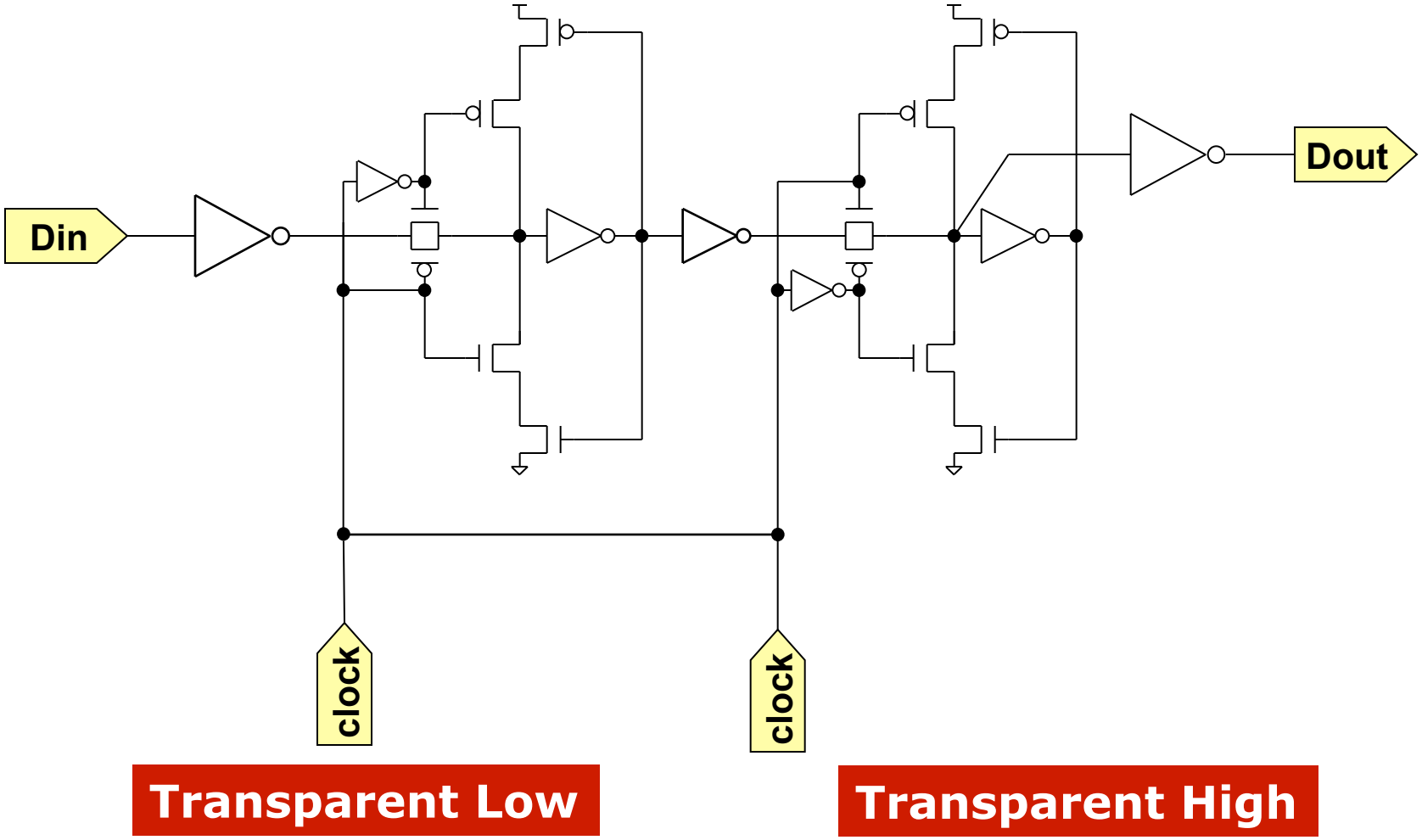


Edge triggered



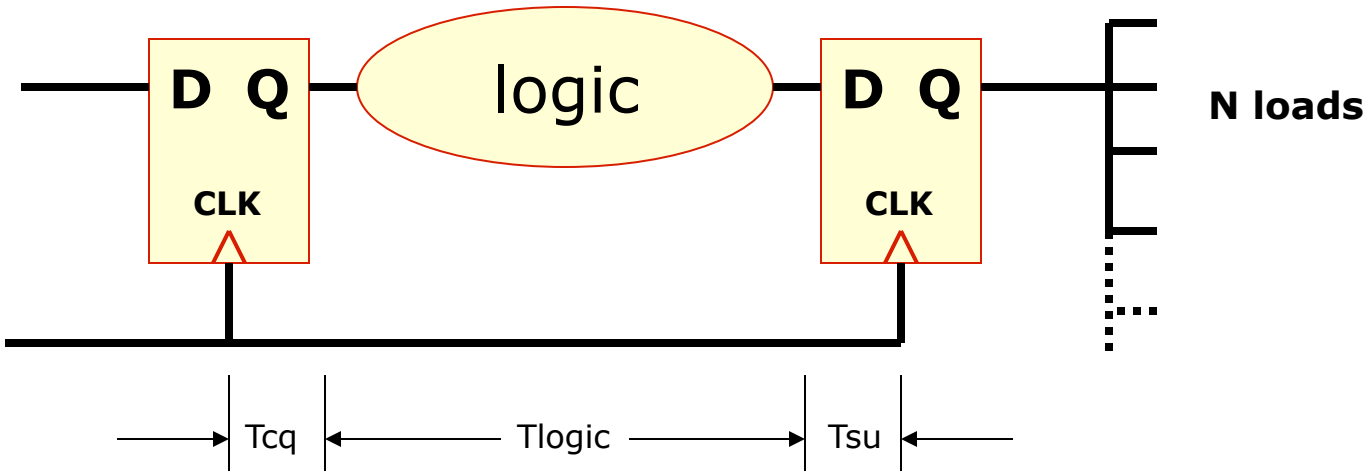
Q only changes at the rising edge of the clock

Building a FLOP with Two Latches

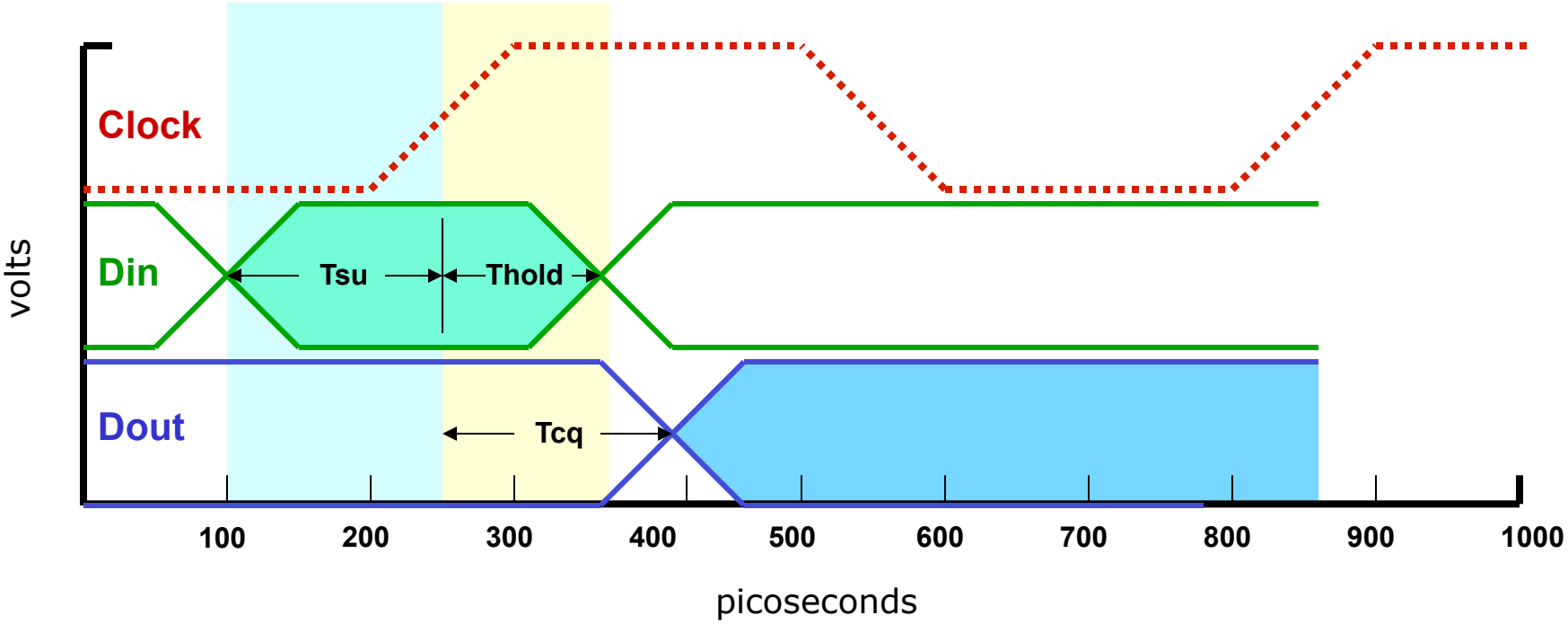


FLOP Delay

- **Sum of setup time and Clk-output delay is the only true measure of the performance with respect to the system speed (MAXDELAY)**
- ***Tcycle = Tcq + Tlogic + Tsu + Tskew***
- ***Tlogic* contains interconnect delay**



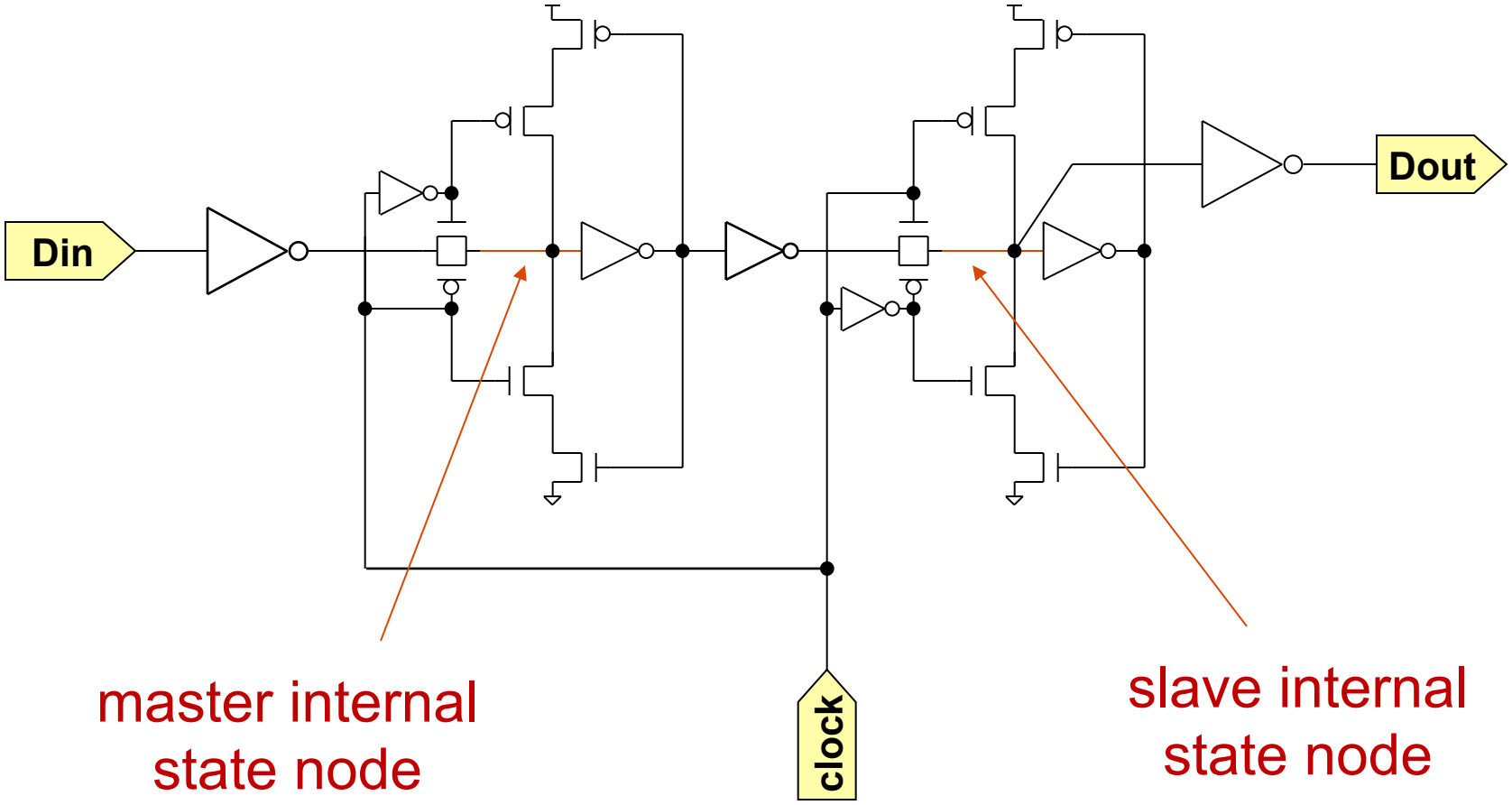
FLOP Timing Diagrams



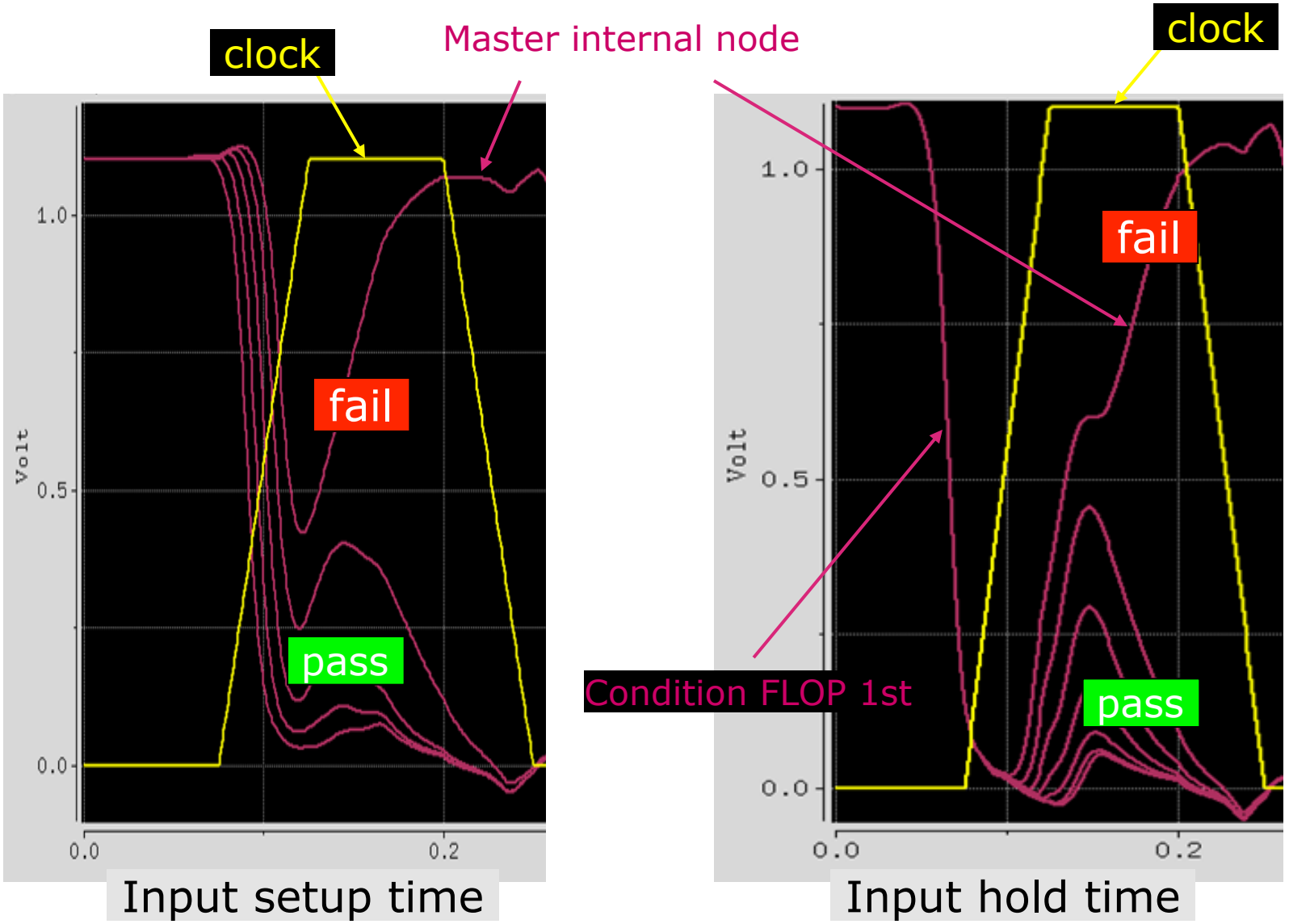
Tsu : input setup time
Thold : input hold time
Tcq : clock to out

Tdata to out = Tsu + Tcq

Edge-Triggered FLIP-FLOP



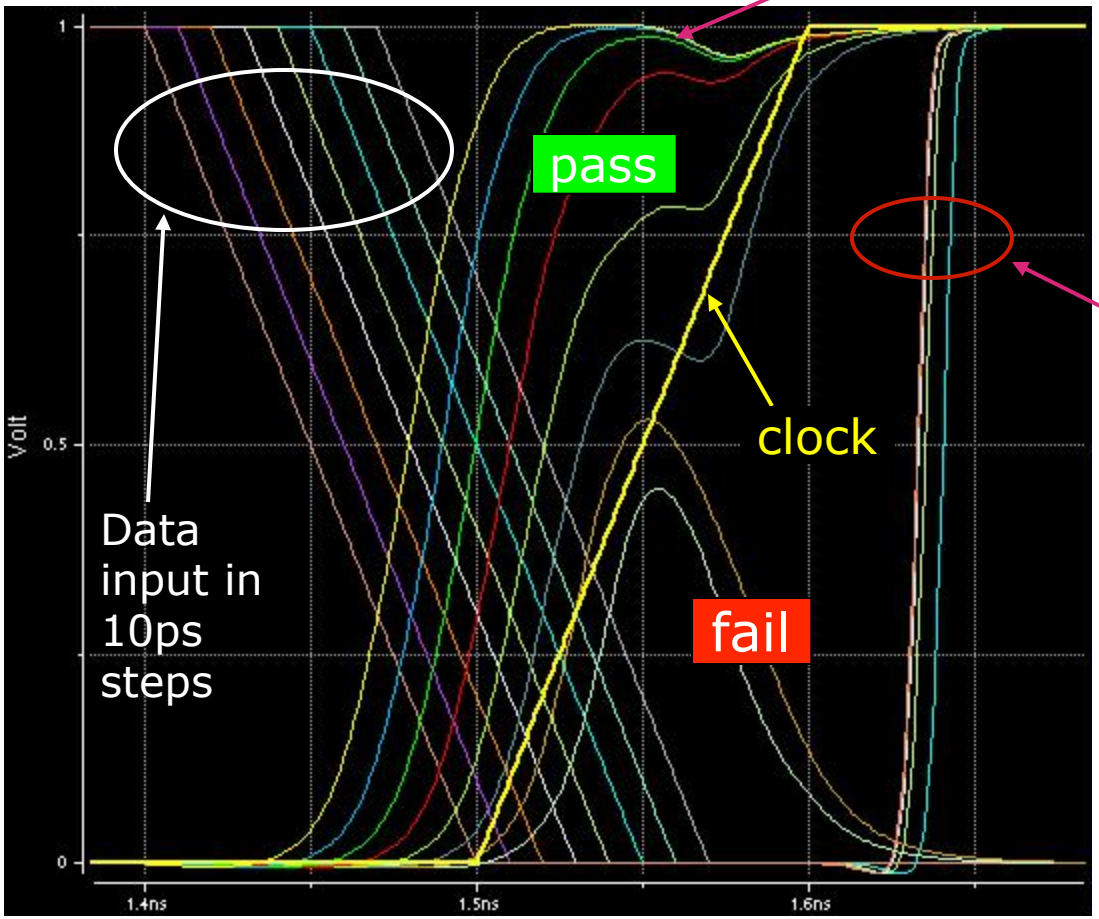
Functional Pass/Failure vs. Tsu and Th



Input setup time

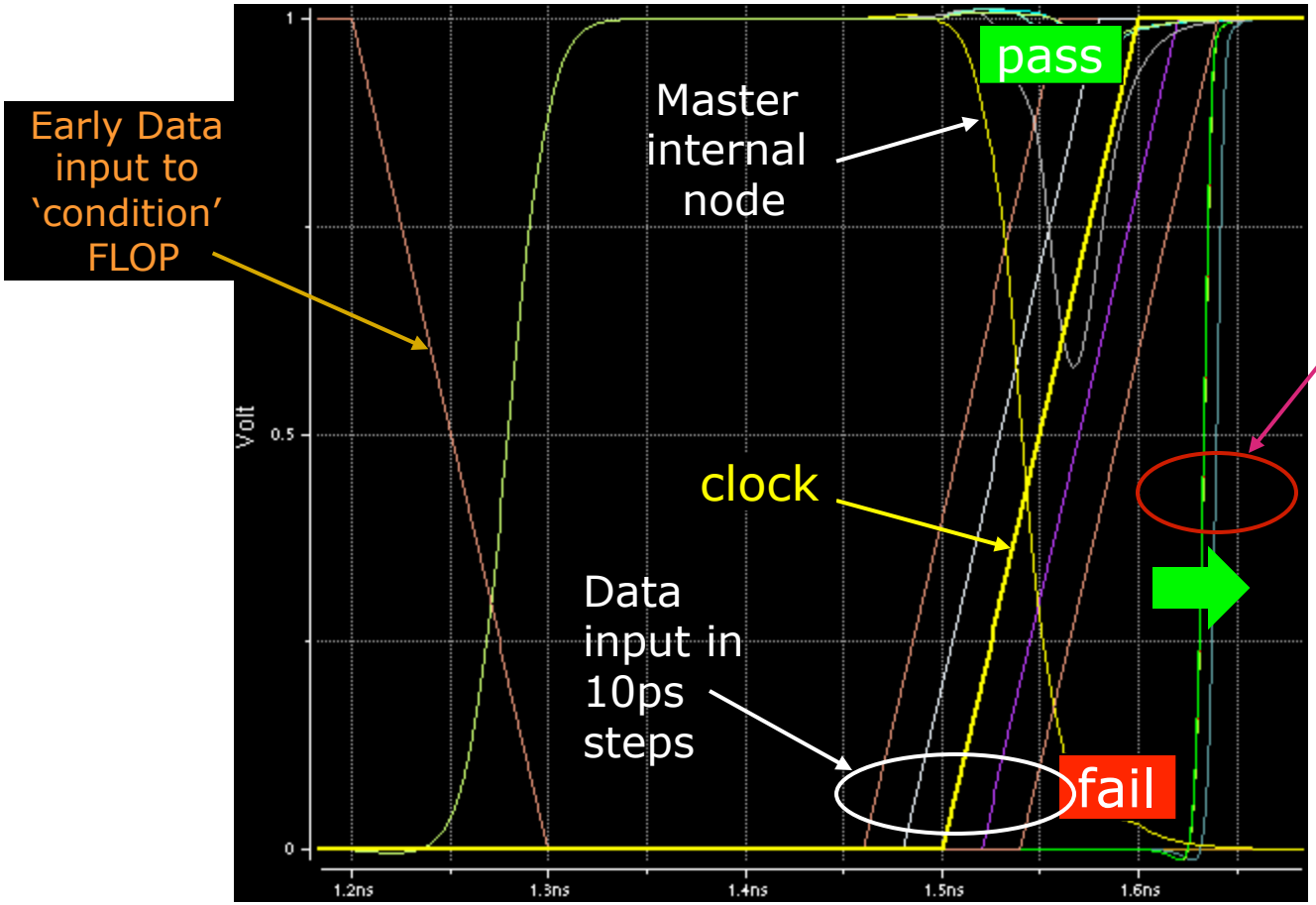
Input hold time

Tcq PUSH-OUT due to Tsu



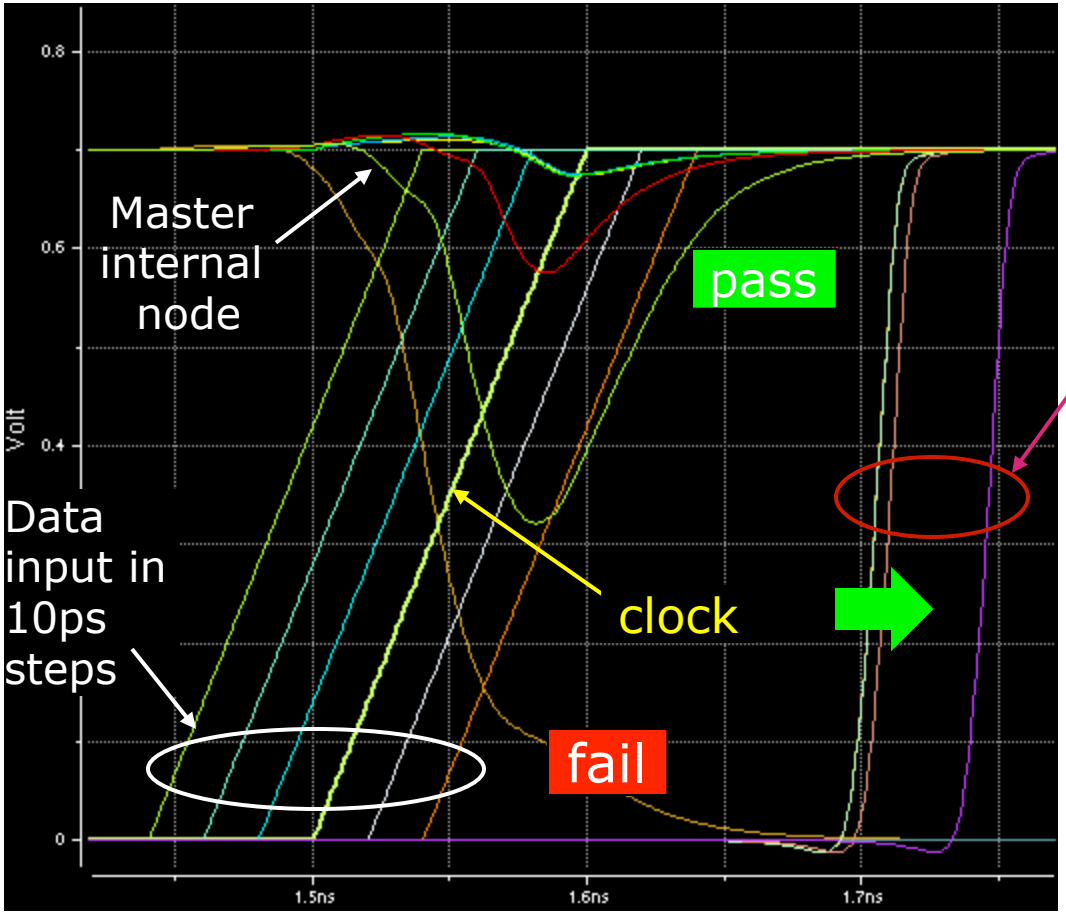
notice the ~10ps 'push-out' in Tcq on the last 'passing' step; there is no output transition on the 2 'failing' steps.

Tcq PUSH-OUT due to Th



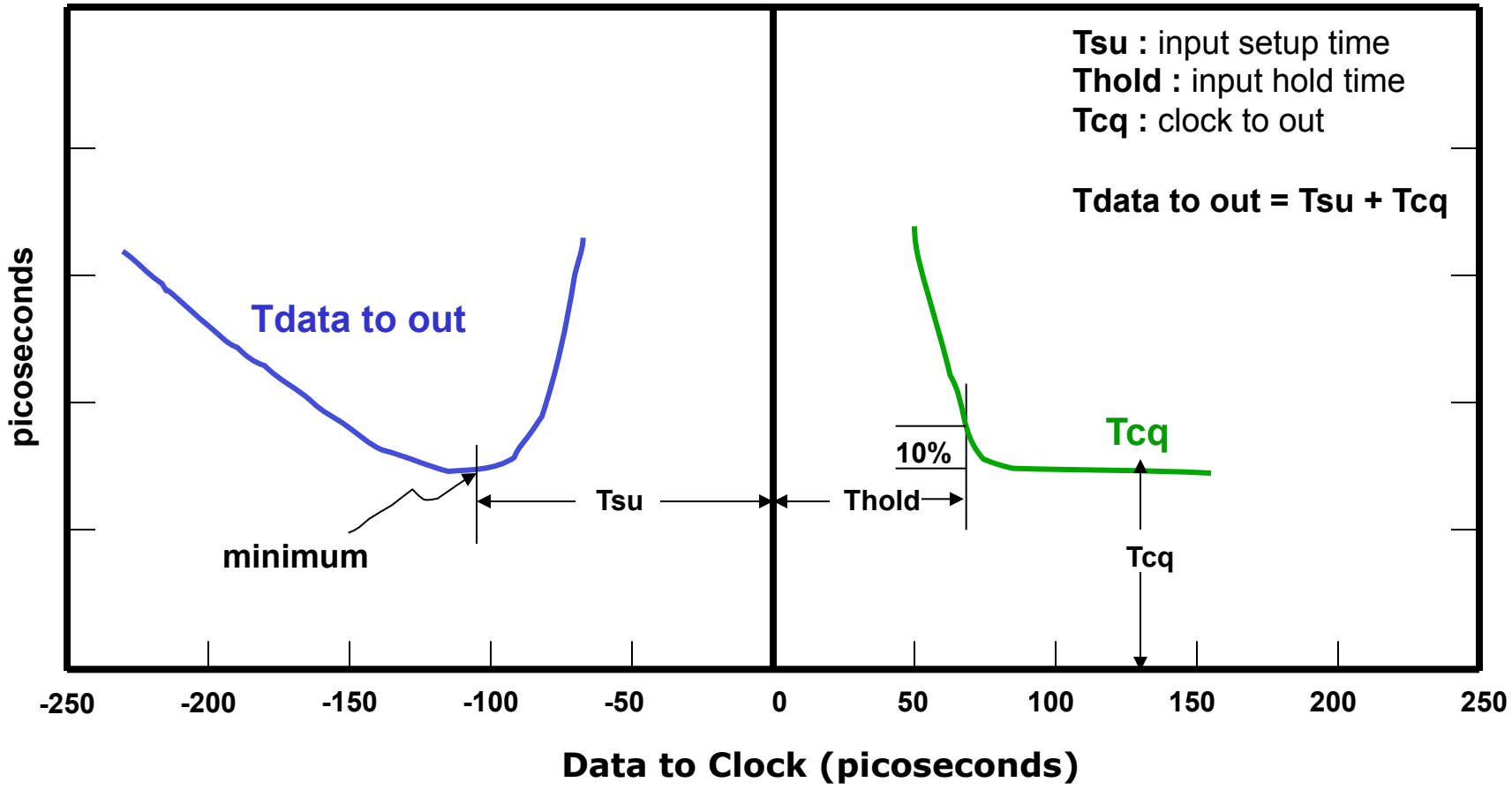
notice the 'push-out' in Tcq on the last 'passing' step; there is no output transition on the 'failing' step.

Tcq PUSH-OUT due to Th (ZOOM-IN)

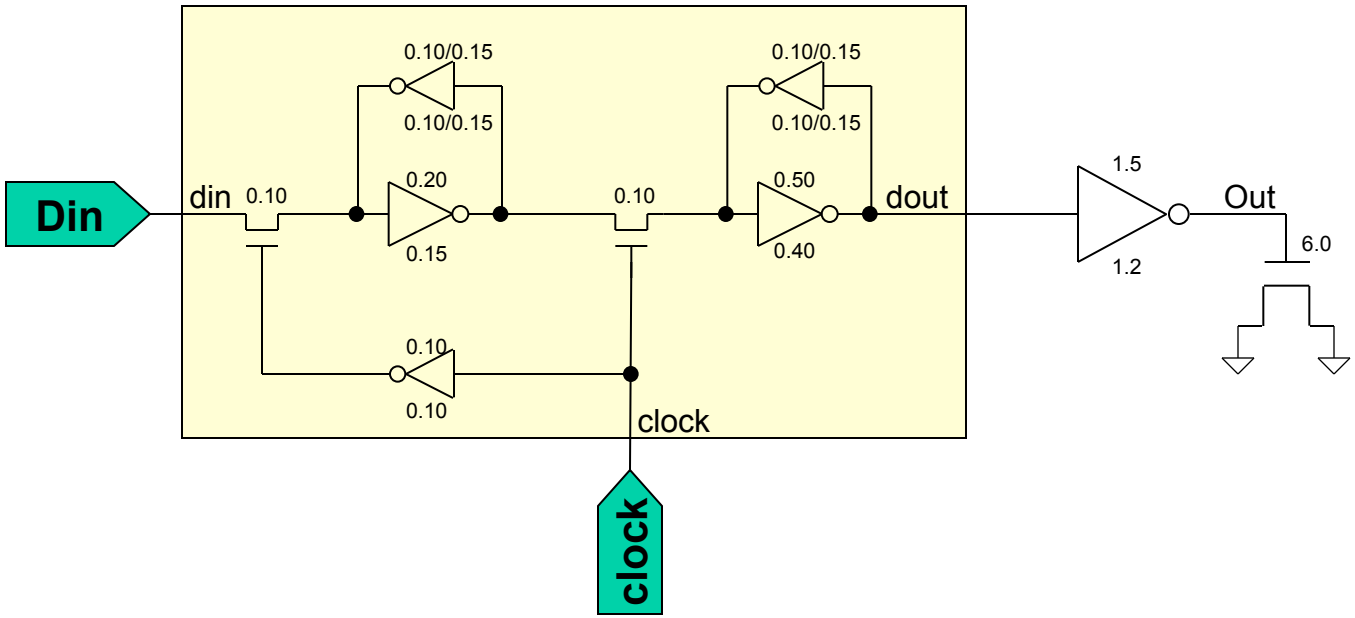


notice the ~40ps 'push-out' in Tcq on the last 'passing' step; there is no output transition on the 'failing' step.

FLOP Characterization



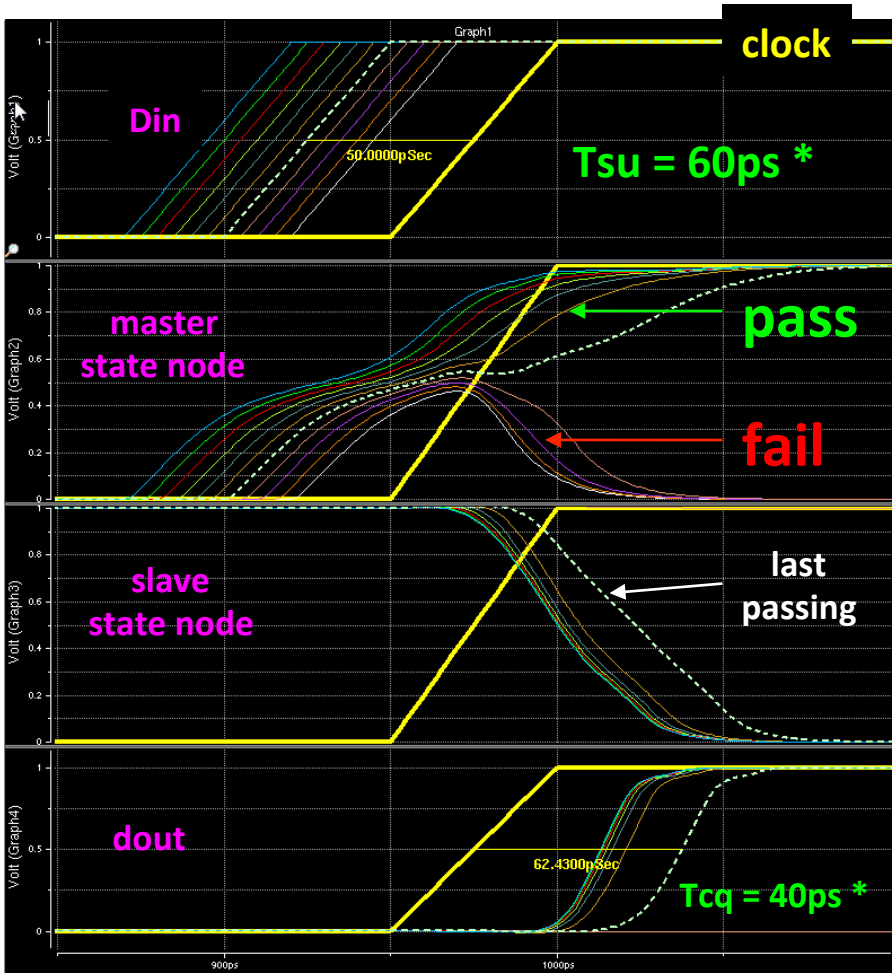
FLOP design a (non-inverting)

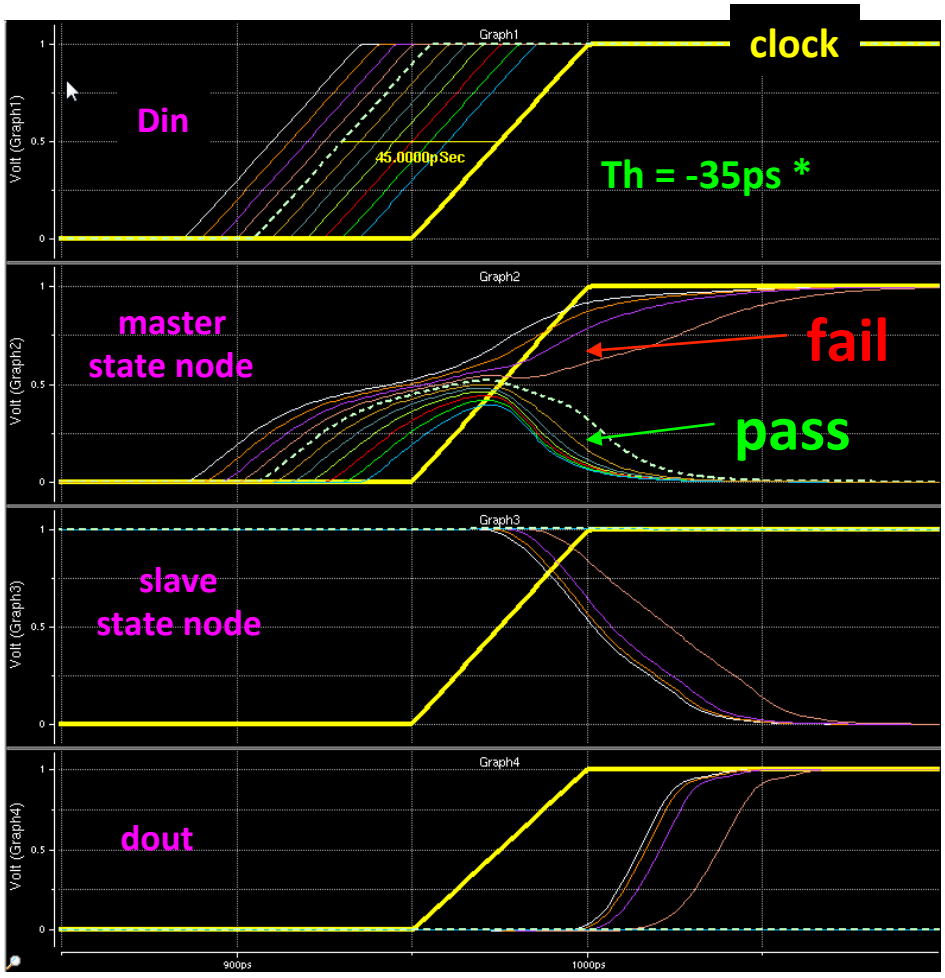


If a channel length is not specified, then use nominal 22nm transistor length.

FLOP design a (non-inverting)

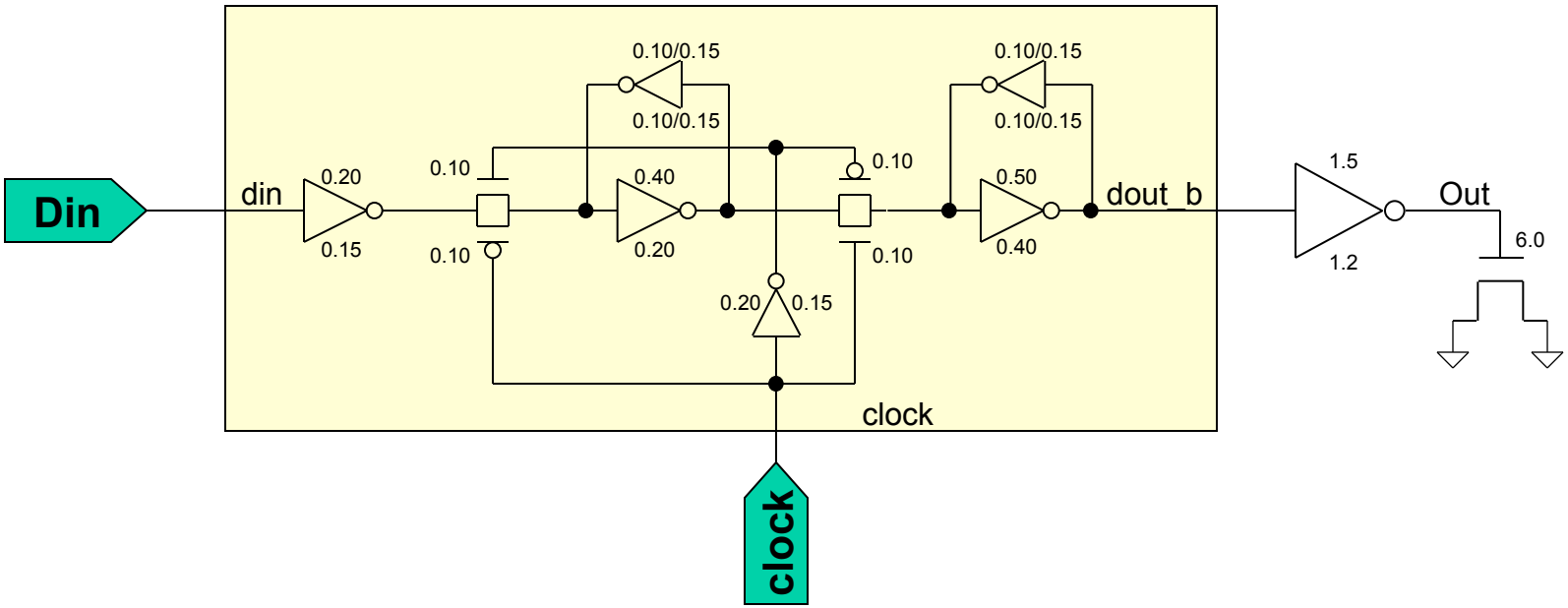
* With negligible Tcq pushout





Hi-to-low transition will be worse due to NFET-only SLAVE pass gate.

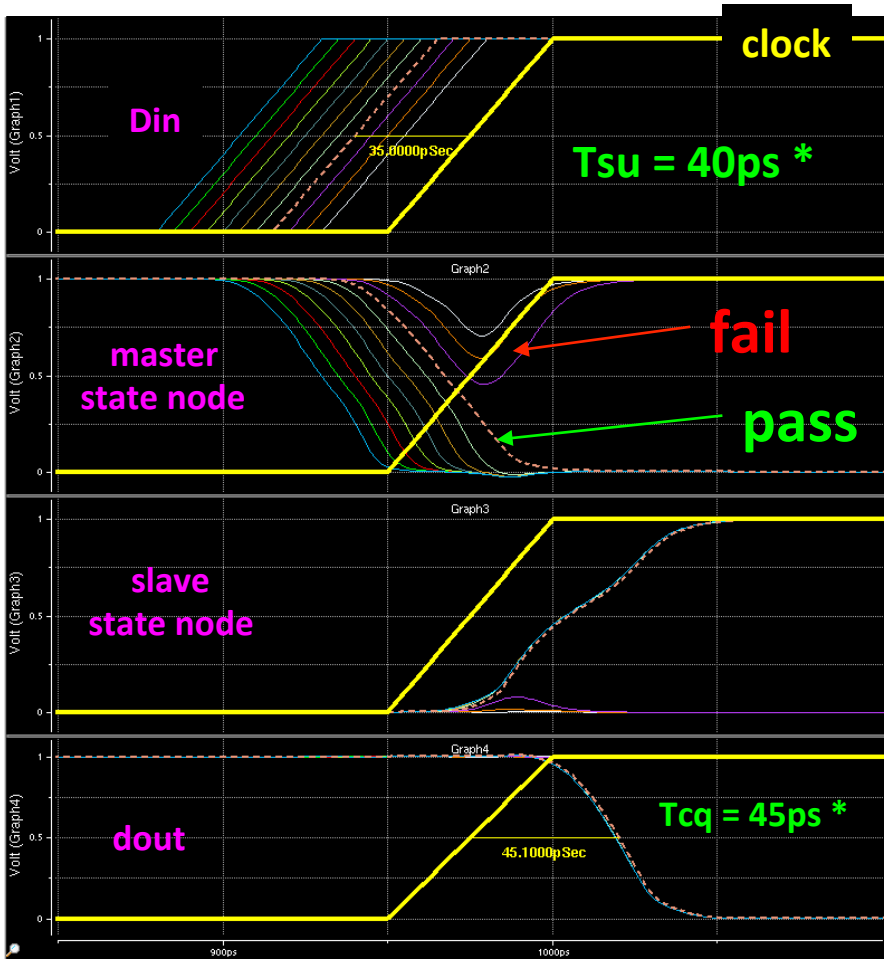
FLOP design b (inverting)

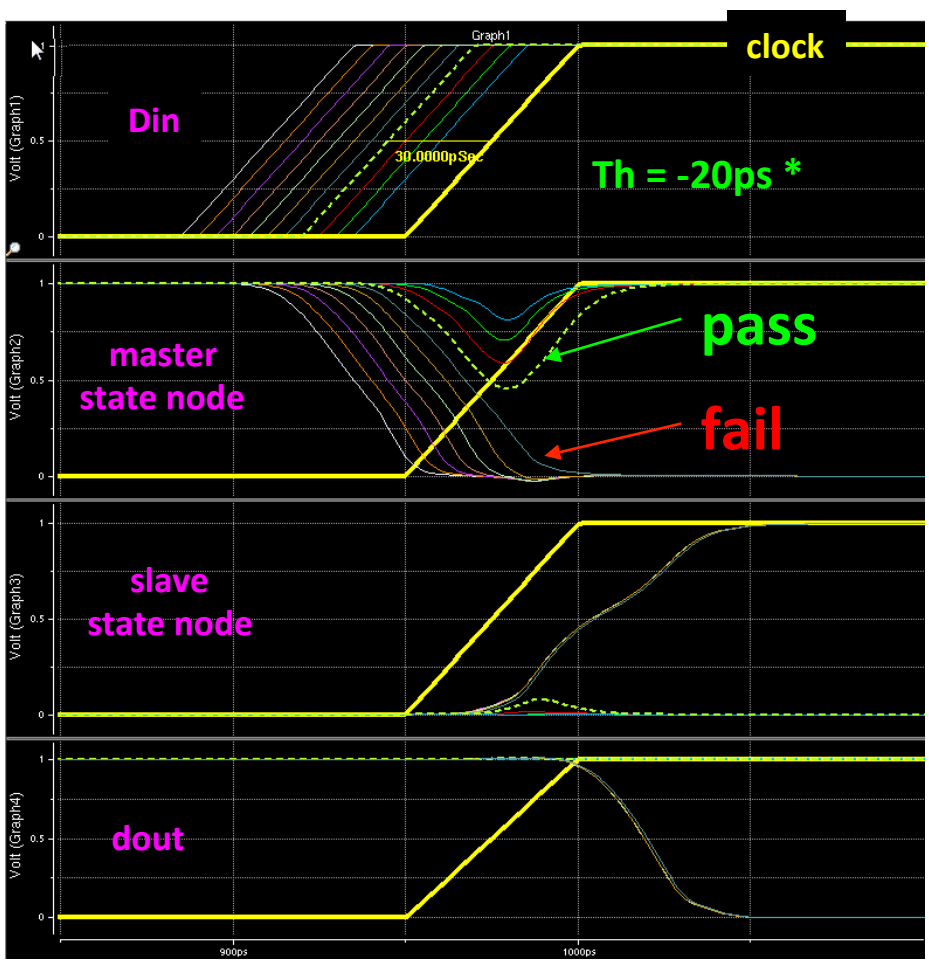


If a channel length is not specified, then use nominal 22nm transistor length.

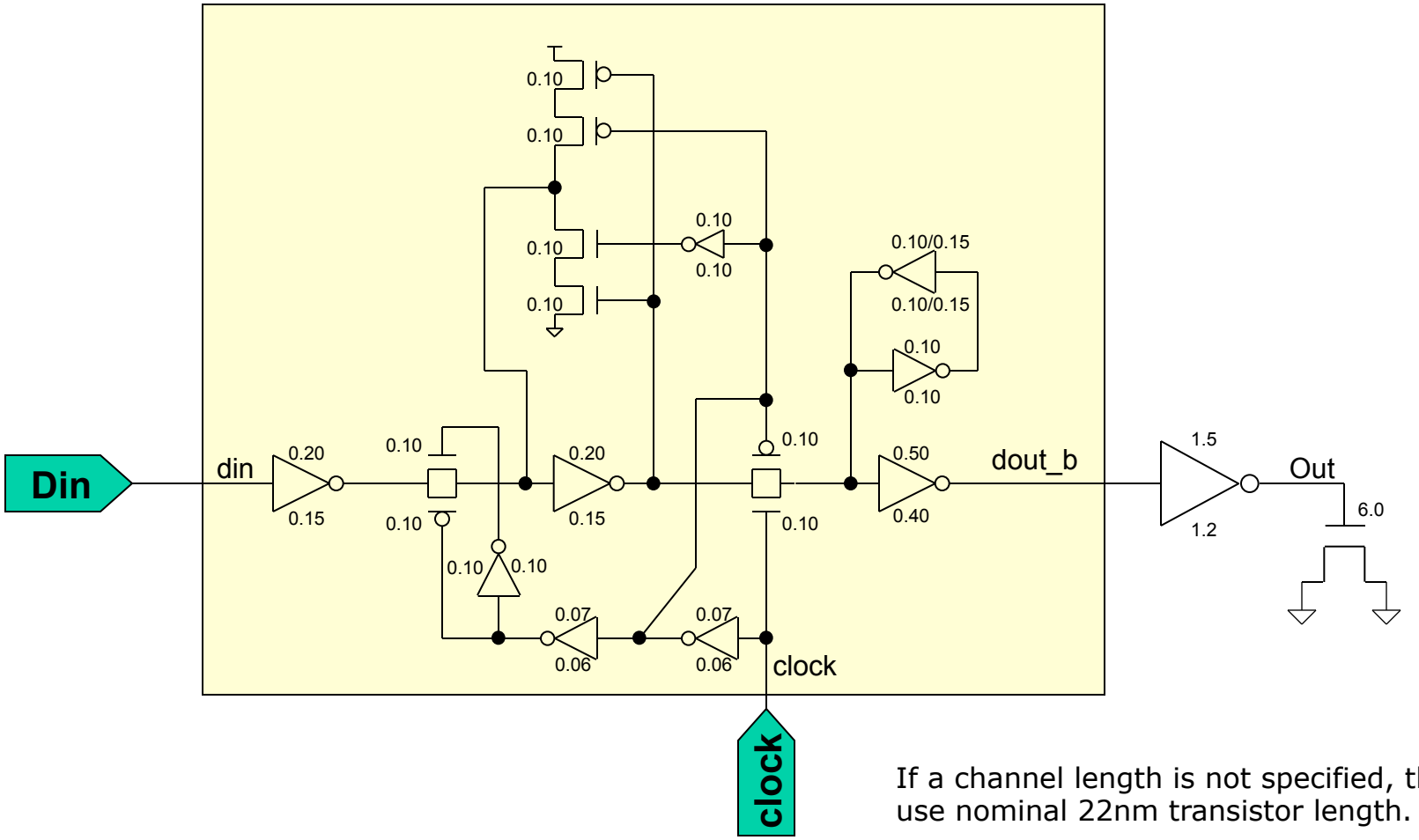
FLOP design b (inverting)

* With negligible Tcq pushout





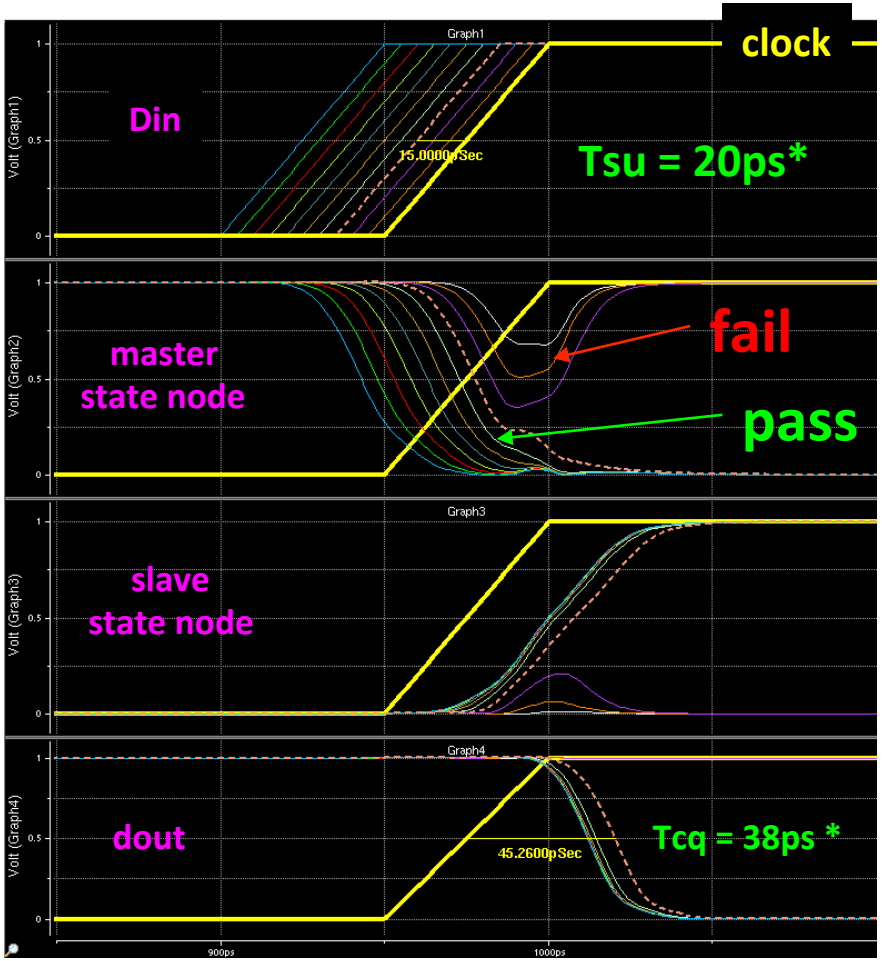
FLOP design c (inverting)

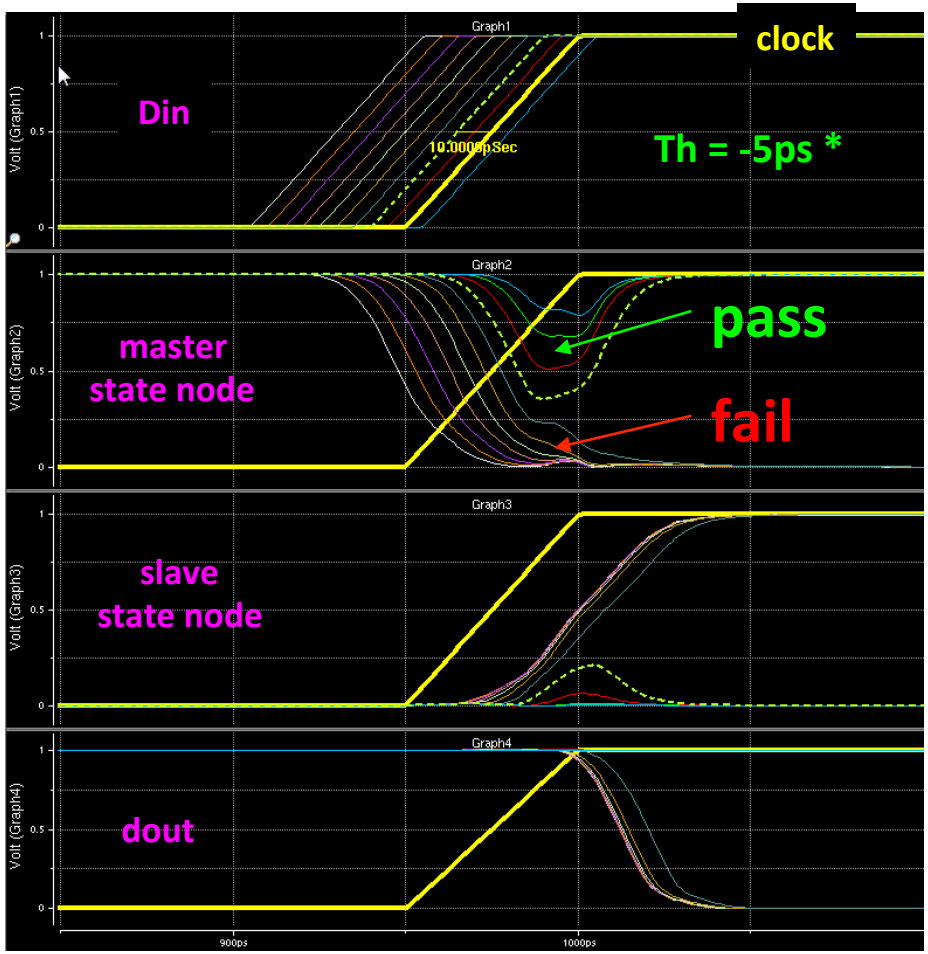


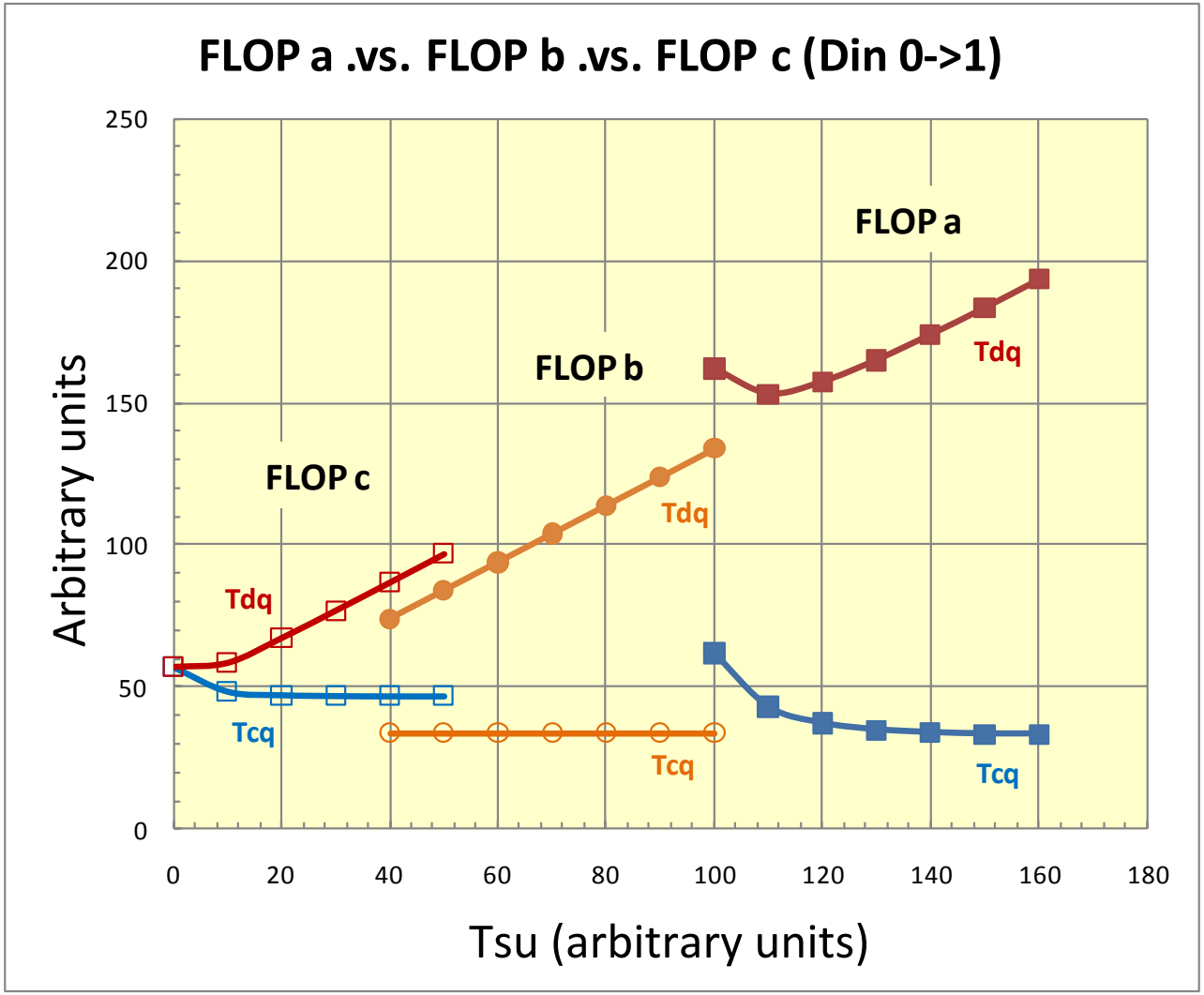
If a channel length is not specified, then use nominal 22nm transistor length.

FLOP design c (inverting)

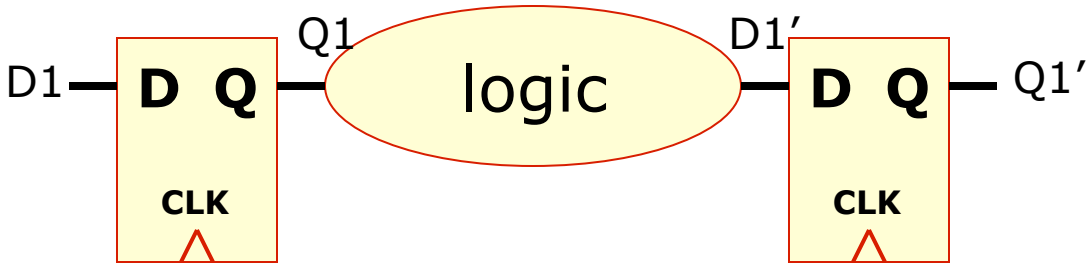
* With negligible Tcq pushout

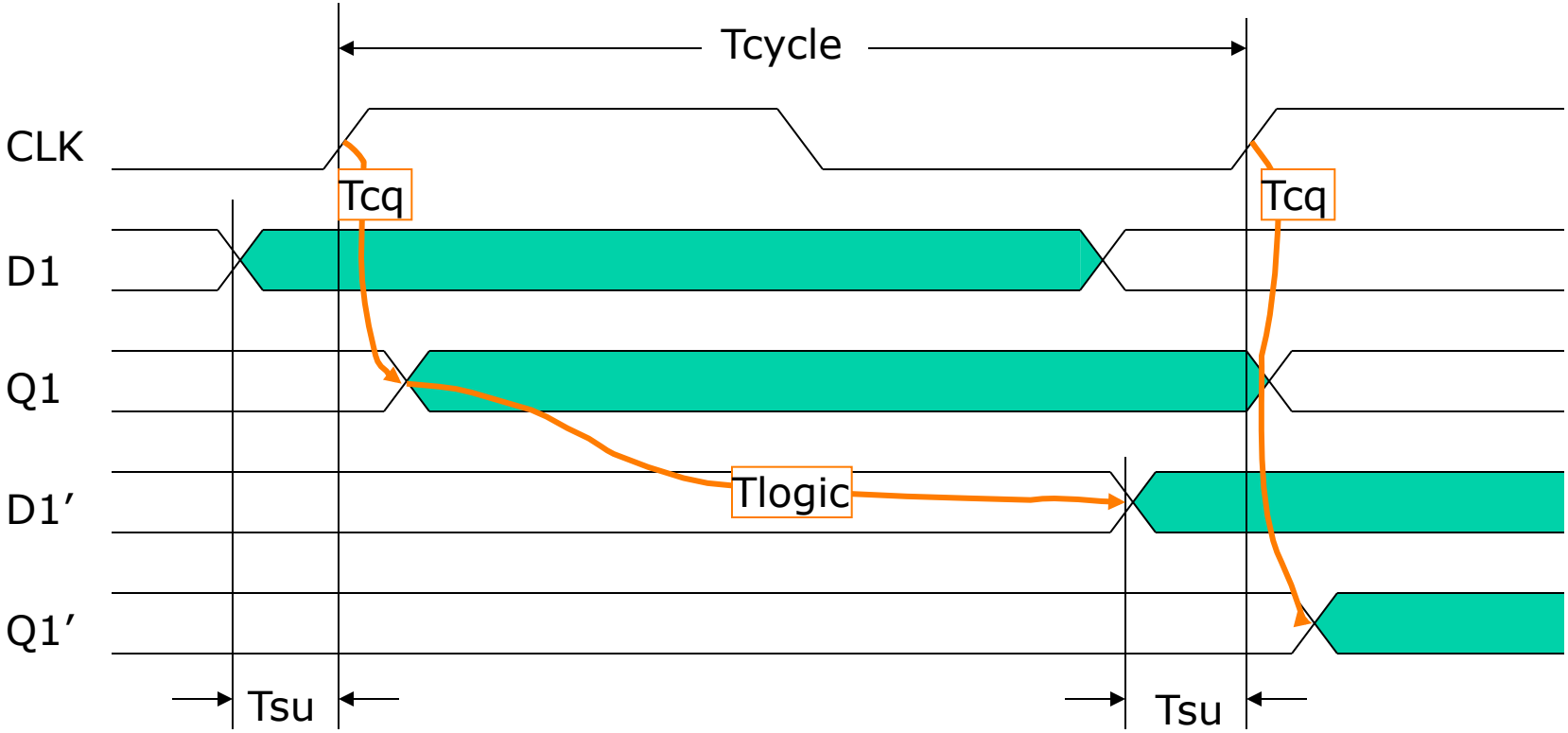





FLOP a .vs. FLOP b .vs. FLOP c (Din 0->1)
Arbitrary units
Tsu (arbitrary units)
250
200
150
100
50
0
0
20
40
60
80
100
120
140
160
180
FLOP a
FLOP b
FLOP c
Tdq
Tdq
Tdq
Tcq
Tcq
Tcq

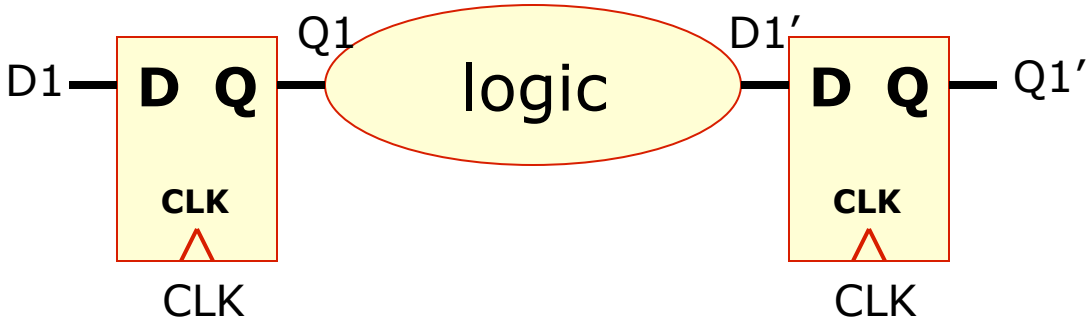
MAXDELAY

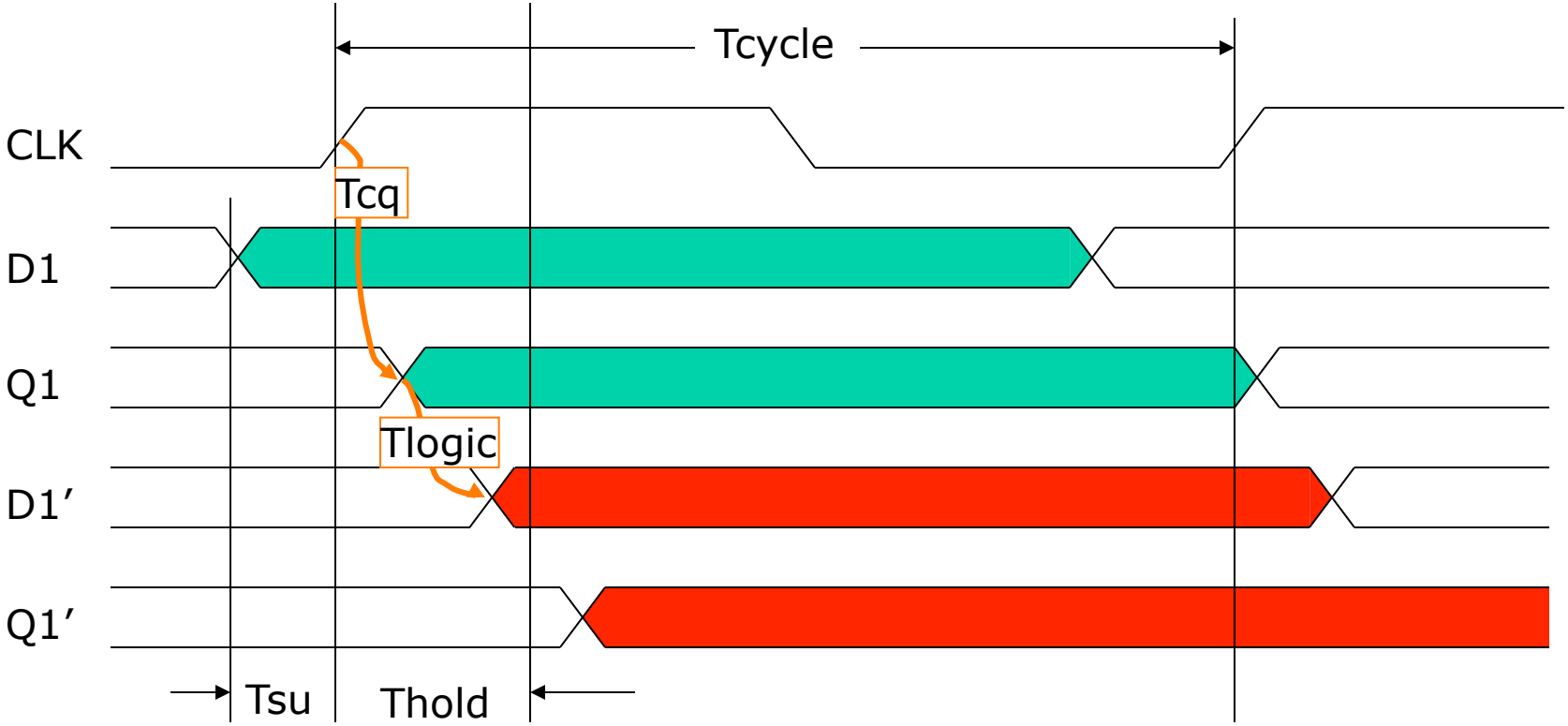




Tlogic < Tcycle – (Tcq + Tsu) or **Tcycle >= Tlogic + Tcq + Tsu**

MINDELAY

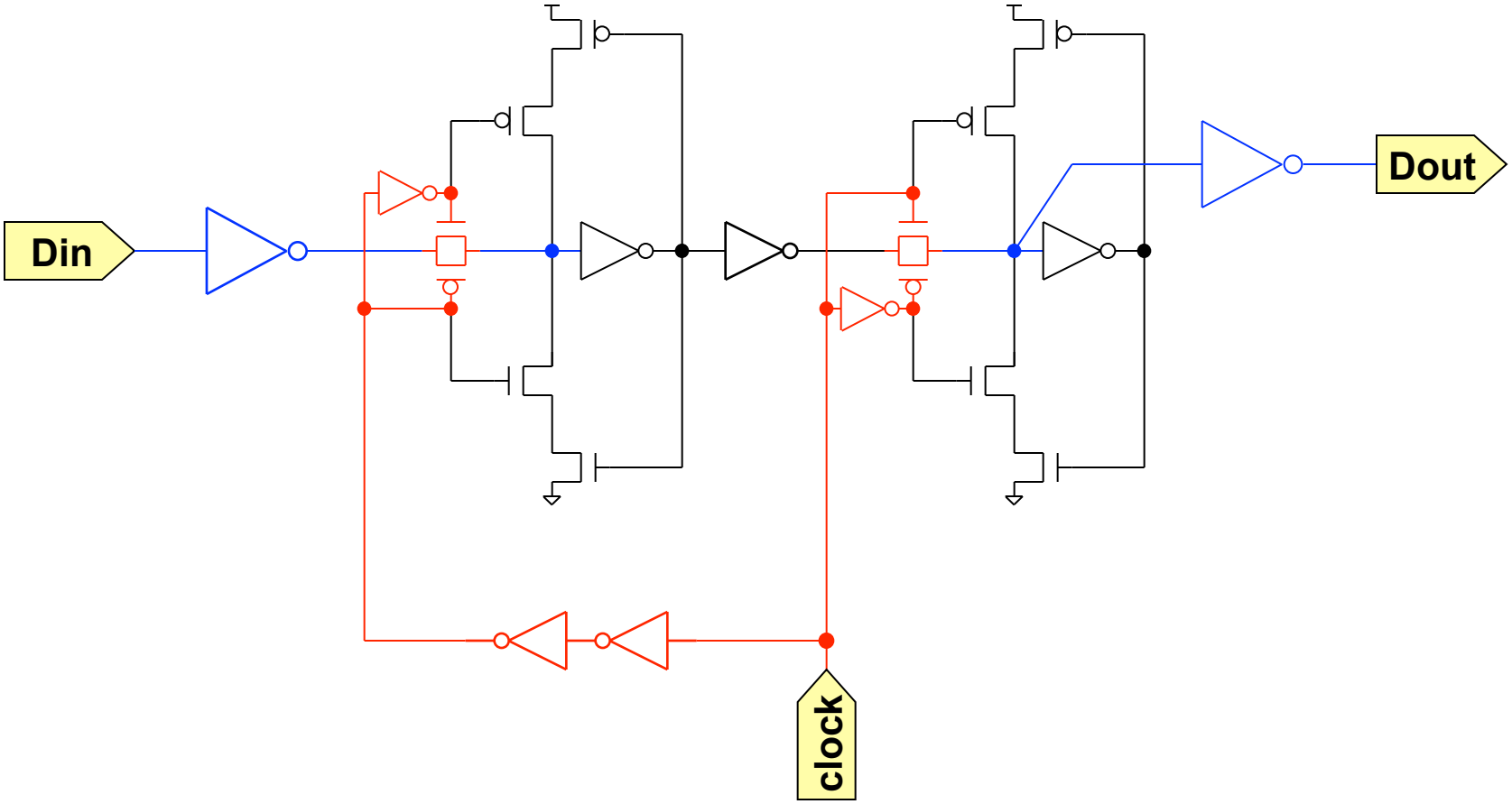




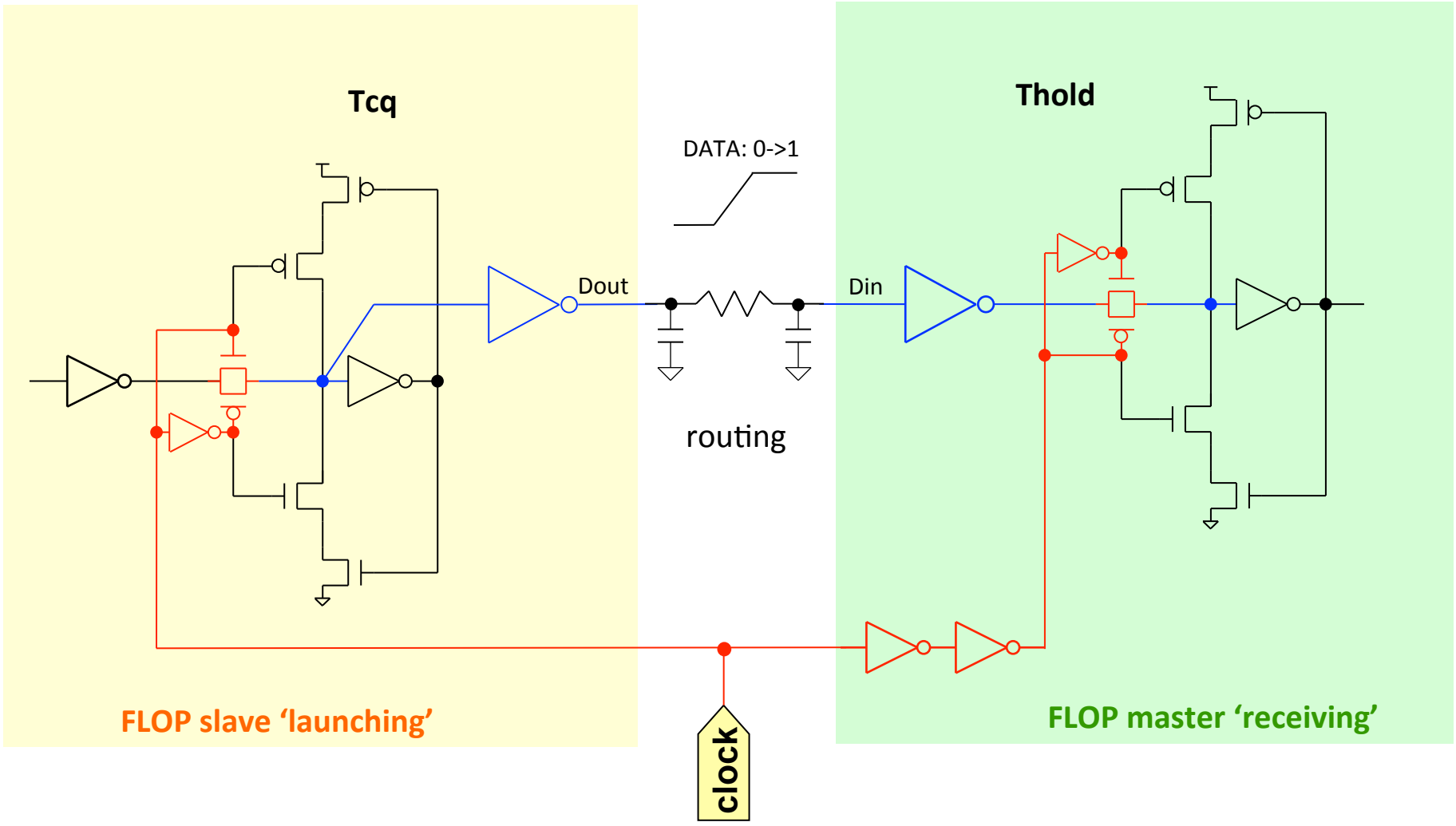
Tlogic > Thold – Tcq + Tskew

BETA Ratio Impact on Tsu, Th and Tcq

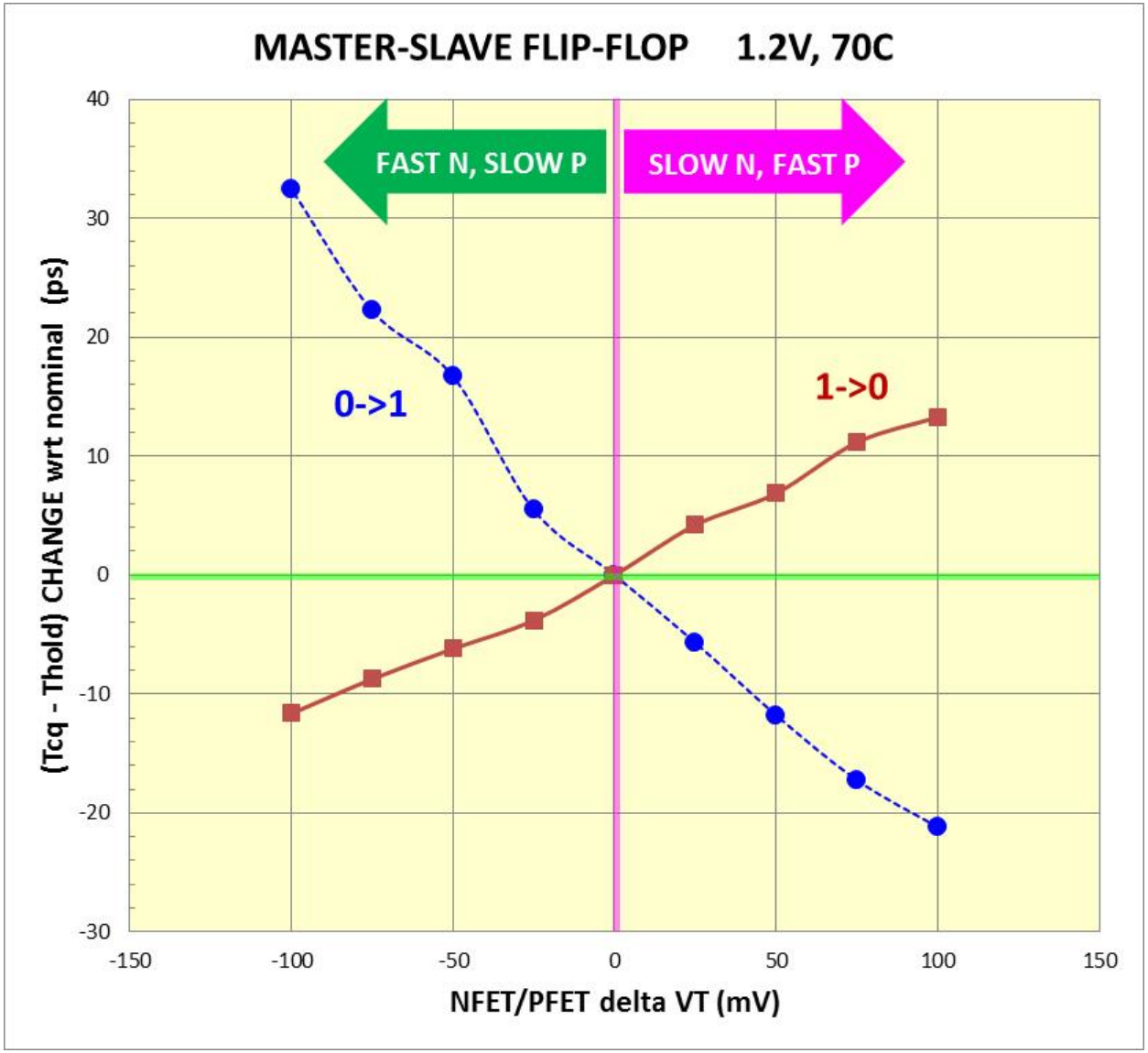
BETA = NFET IDSAT/PFET IDSAT



Back-To-Back FLOPs



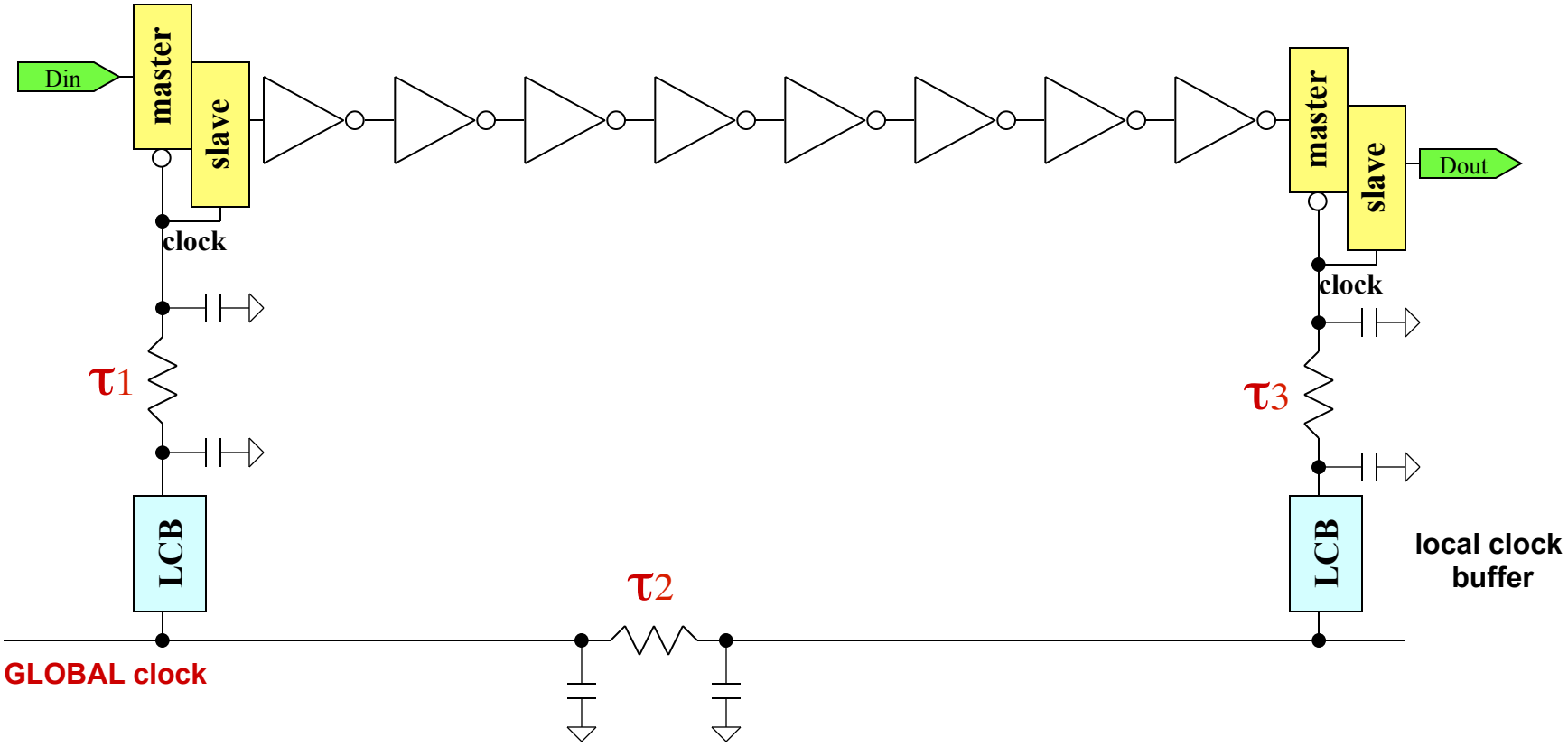
BETA Ratio Impact on Tsu, Th and Tcq



Increased MINDELAY margin

Reduced MINDELAY margin

Clock Skew Impact to Fmax

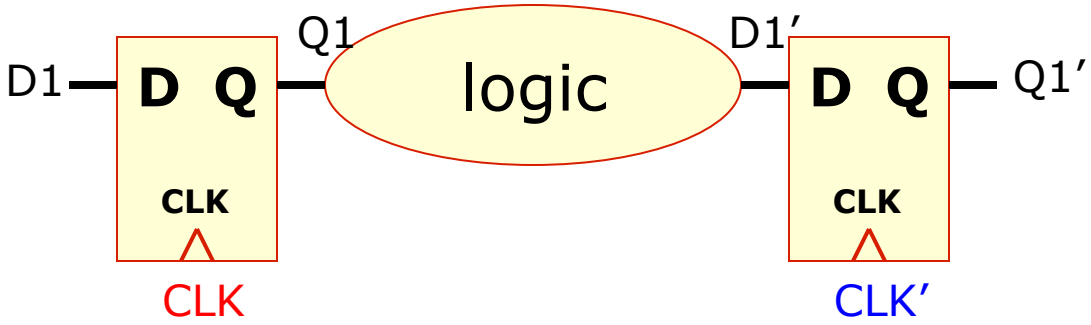


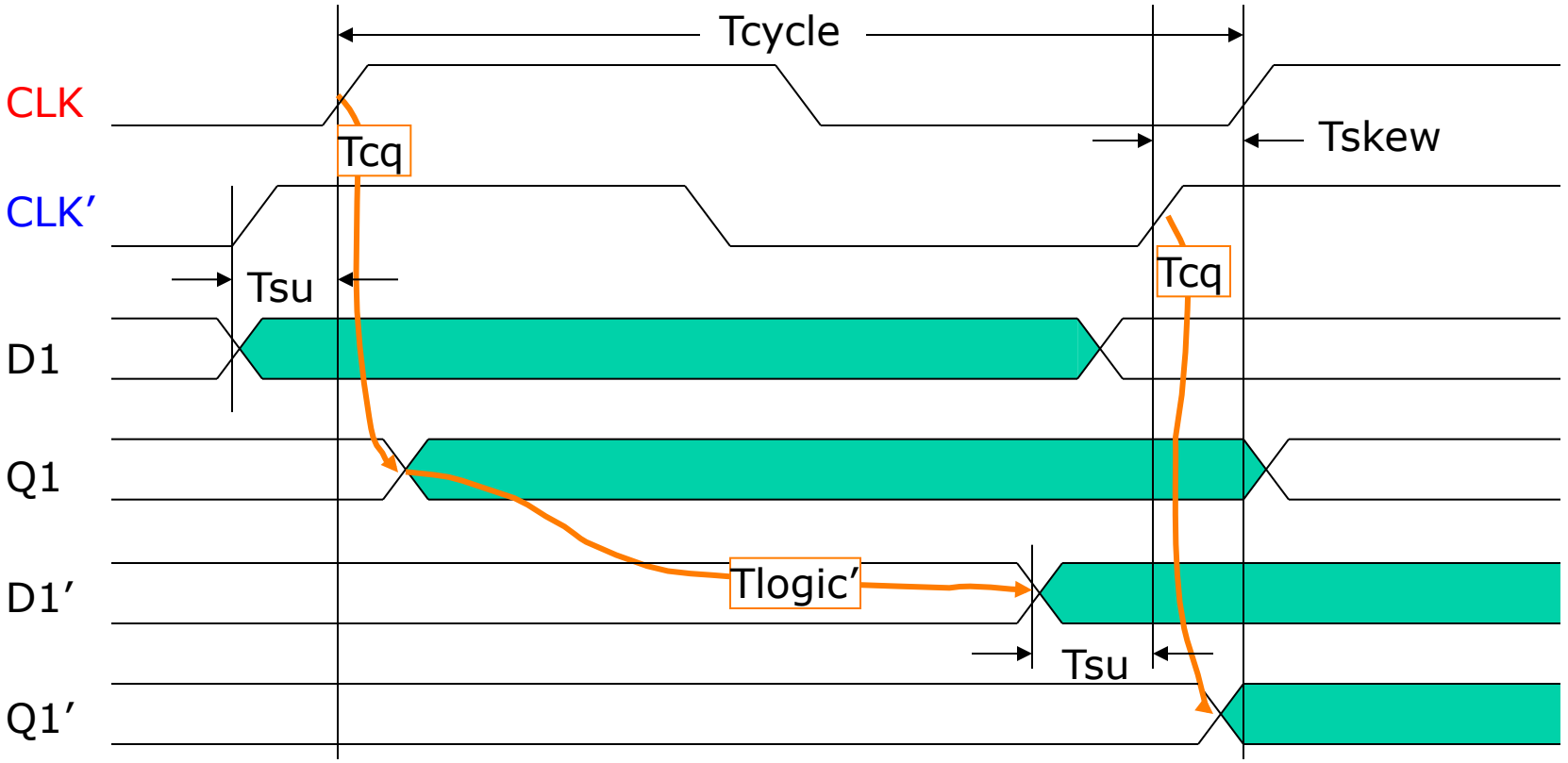
Tcycle = Tcq + Tlogic + Tsu + $T_{clock\_uncertainty}$

$T_{clock\_uncertainty}$ = clock skew + clock jitter

clock skew = $\tau 1 - \tau 2 - \tau 3$

MAXDELAY with Clock Skew





Tlogic < Tcycle – (Tcq + Tsu + Tskew)

DESIGN WINDOW

$$T_{hold} - T_{cq} + T_{skew} < T_{logic}$$

and

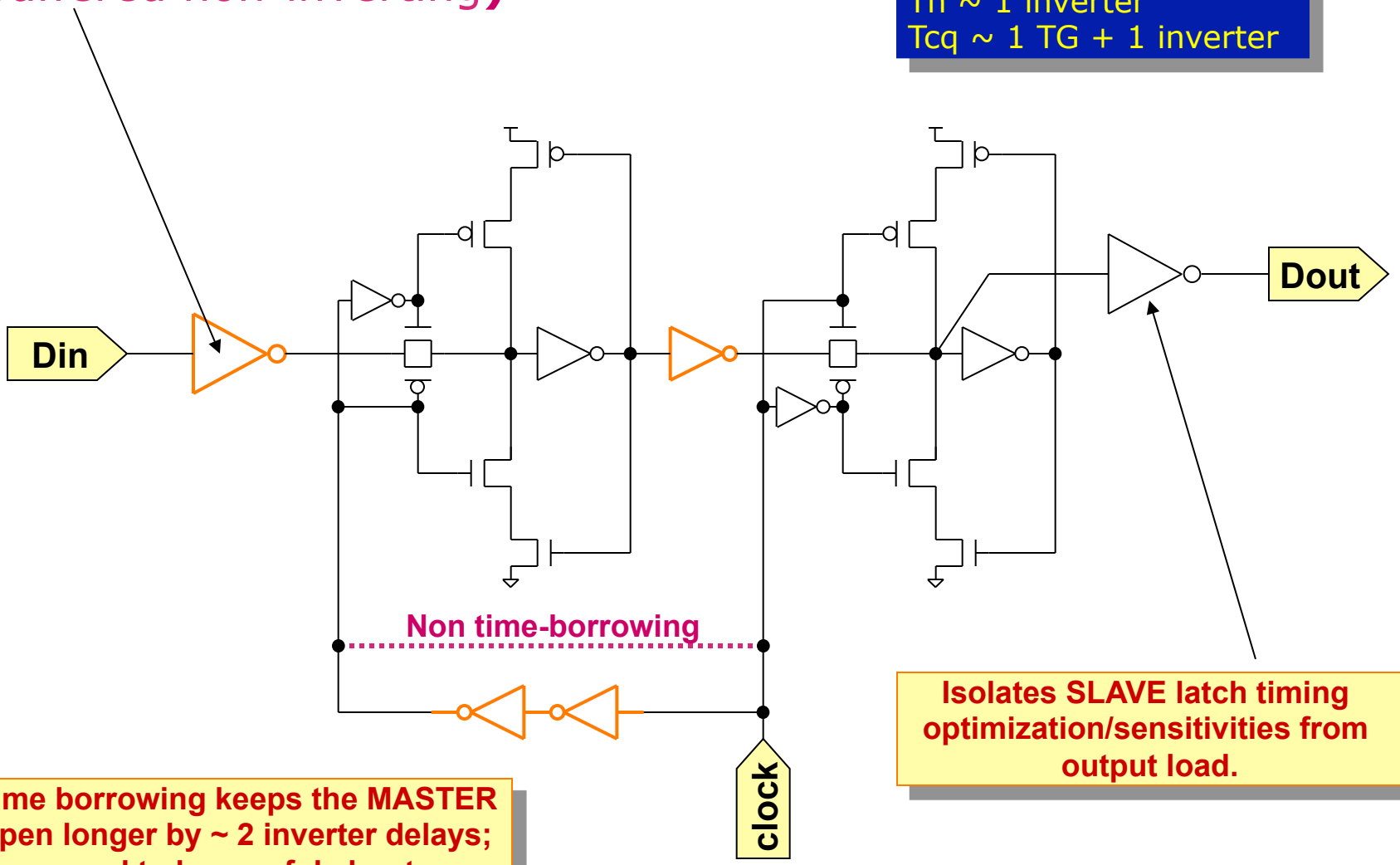
$$T_{logic} < T_{cycle} - (T_{cq} + T_{su} + T_{skew})$$

If Tcq > Thold + Tskew, then MINDELAY hazard is removed since Tlogic >= 0 always.

T-G Master-Slave FLOP

(buffered non-inverting)

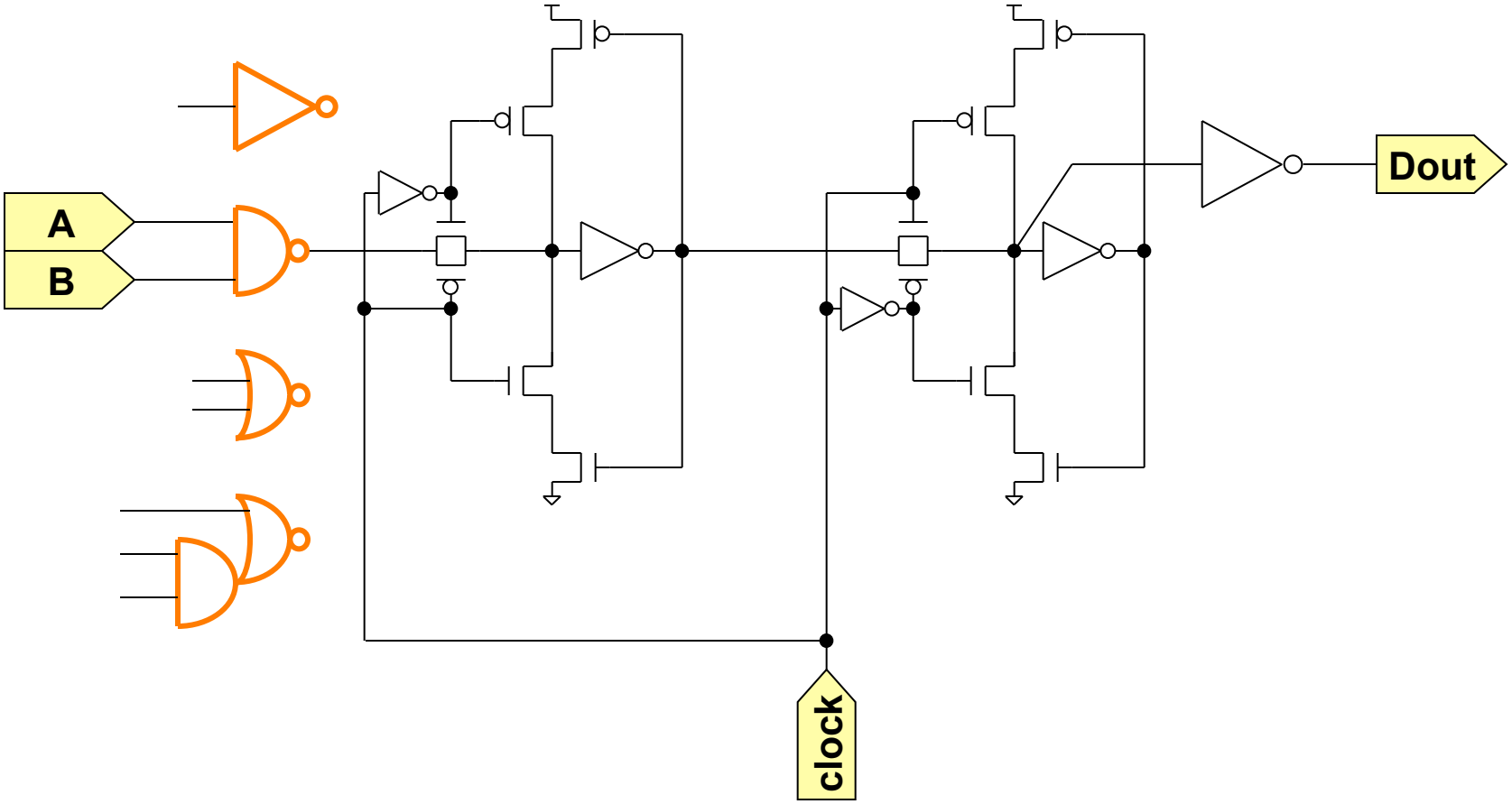
TIMING:
Tsu ~ 1 TG + 2 inverters
Th ~ 1 inverter
Tcq ~ 1 TG + 1 inverter



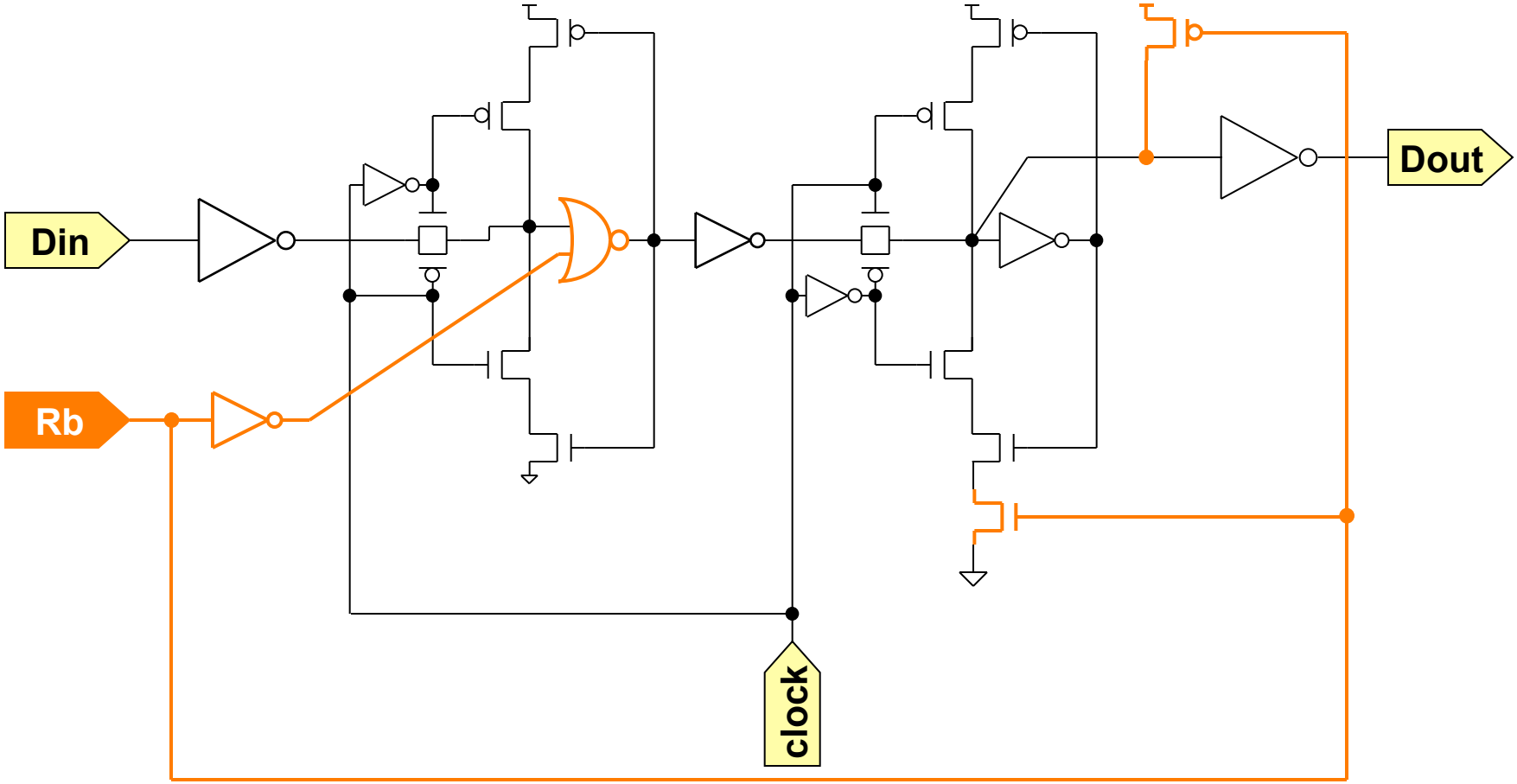
Isolates SLAVE latch timing optimization/sensitivities from output load.

Time borrowing keeps the MASTER open longer by ~ 2 inverter delays; need to be careful about MINDELAYS

Merged Function inverting FLOP



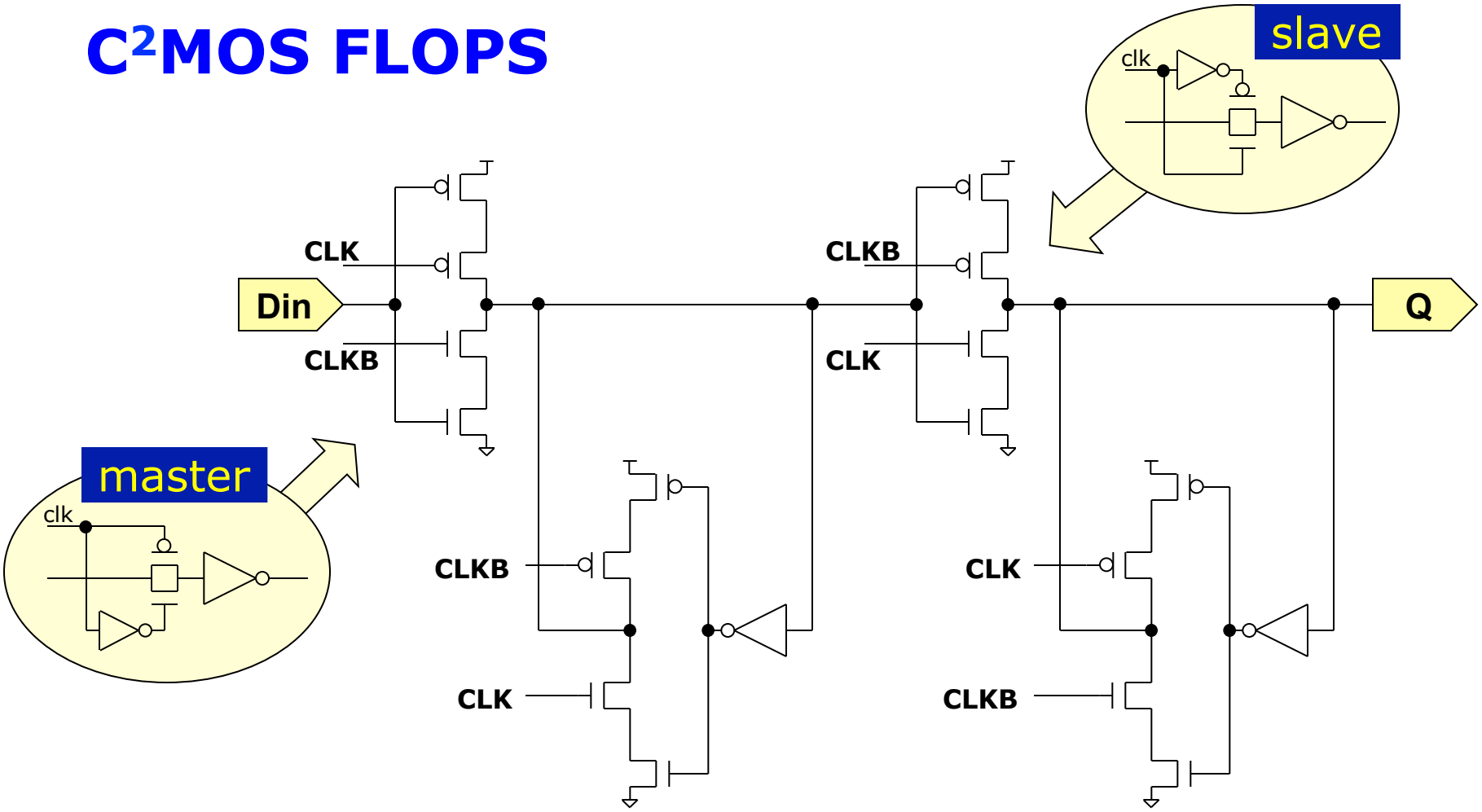
RESETABLE Master-Slave FLOP

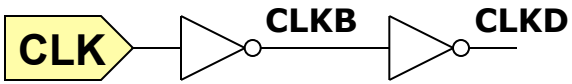


Other Circuit Topologies for M-S FLOPS

- **C^2MOS**
- **Hybrid Latch Flip-Flop (HLFF)**
- **Pulse Latch**
- **In Backup:**
  - True Single-Phase Clock FLOP
  - K-6 Dual-Rail ETL
  - Semi-Dynamic Flip-Flop (SDFF)

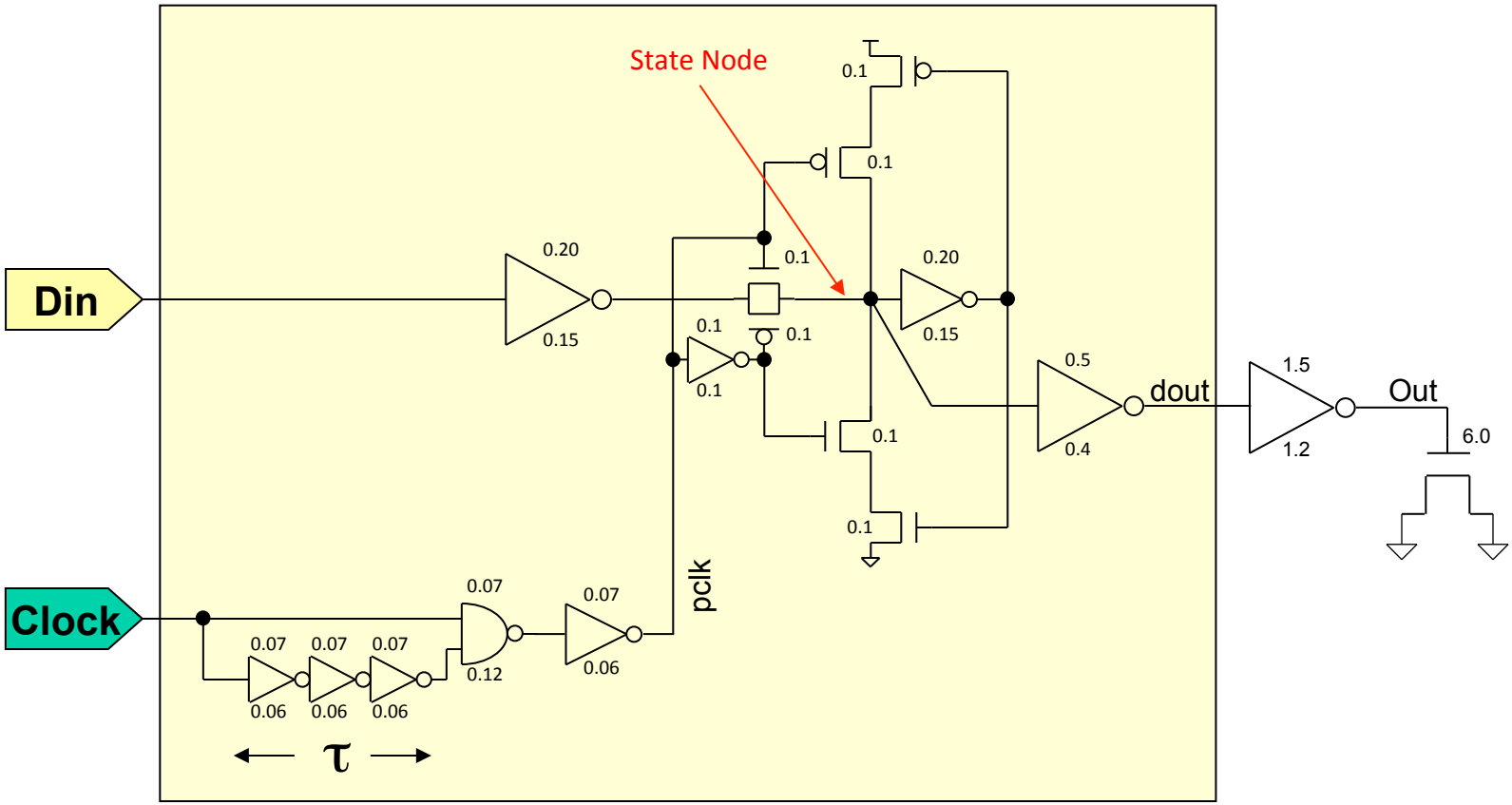
C²MOS FLOPS





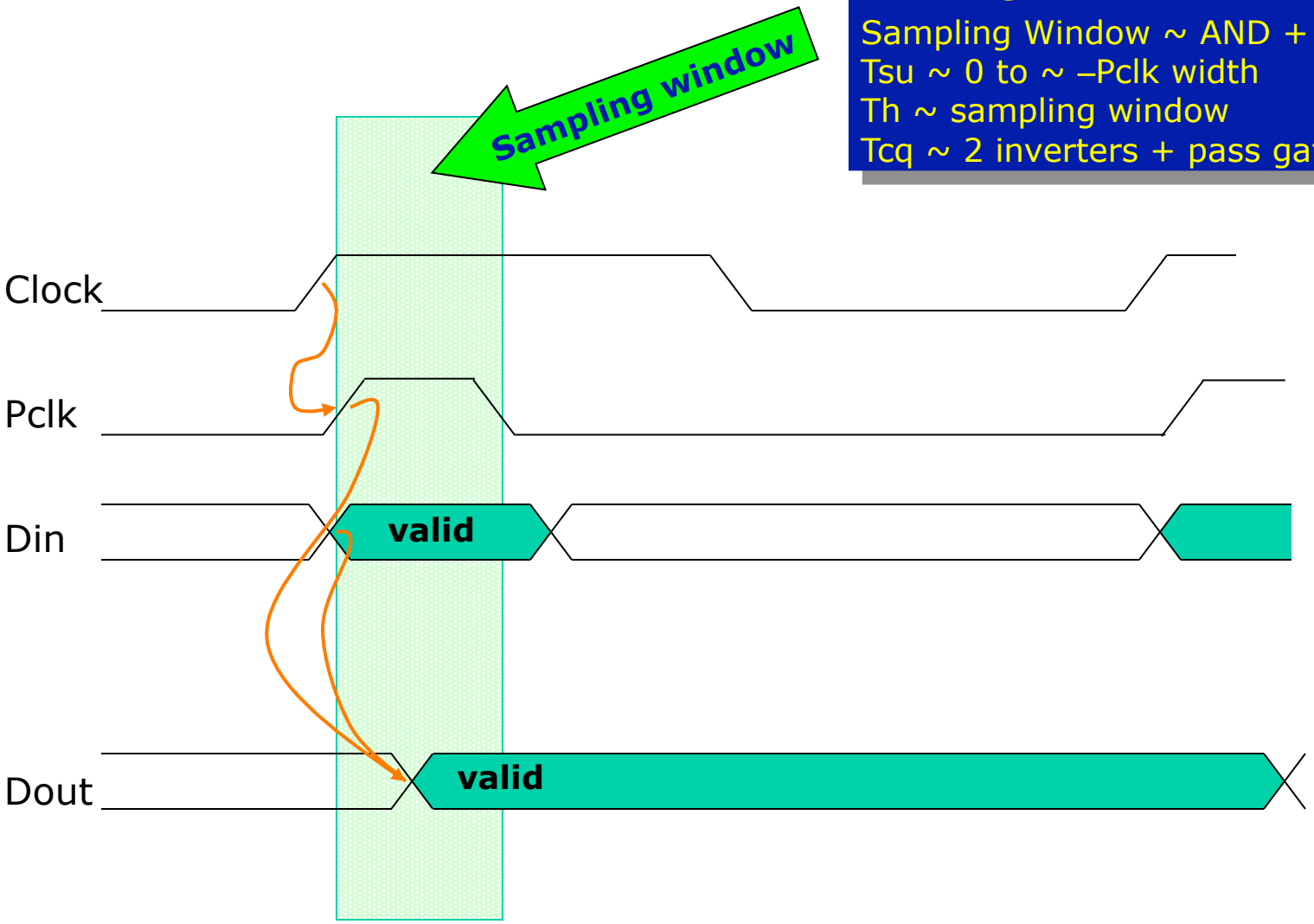
Clock slope becomes critical
Low power feedback
Poor driving capability

Pulse Latch

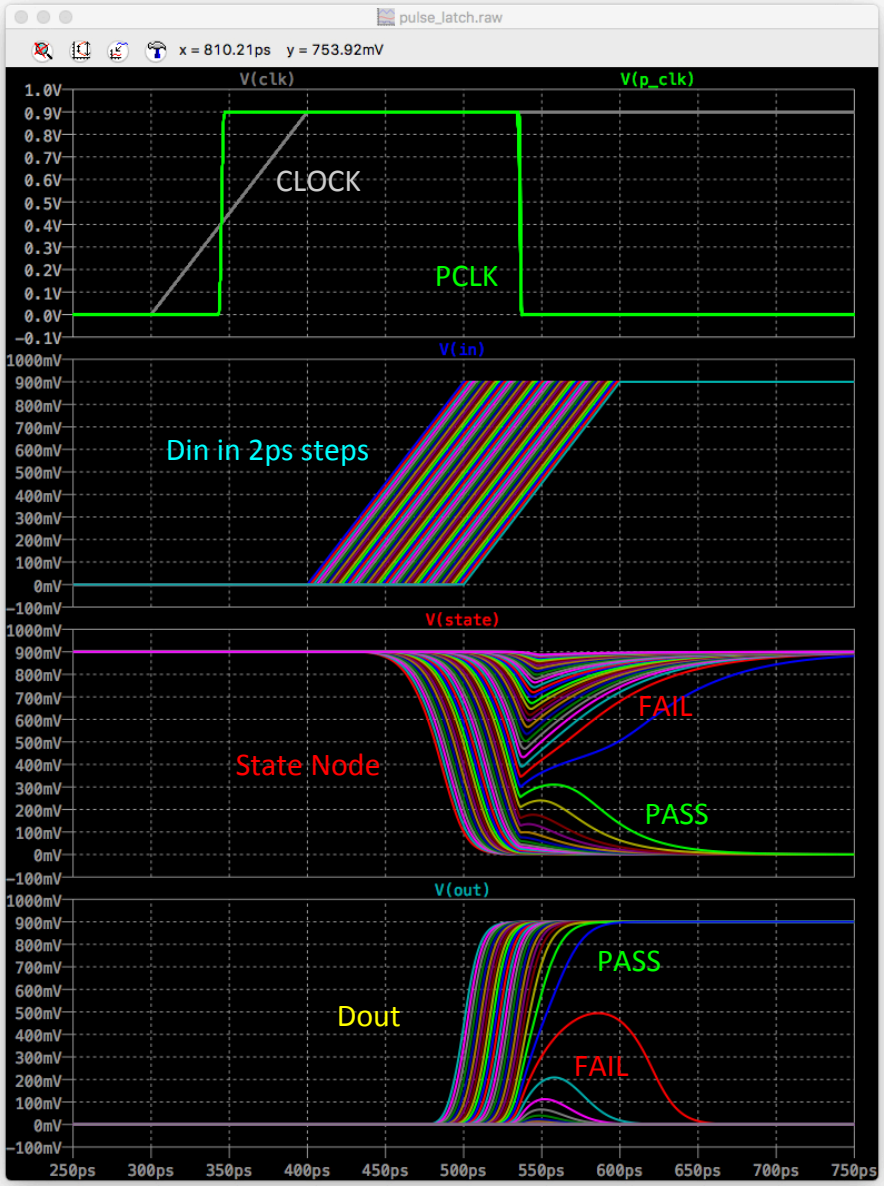

State Node
Din
Clock
pclk
dout
Out
τ
0.20
0.15
0.1
0.20
0.15
0.1
0.1
0.1
0.1
0.1
0.1
0.5
0.4
1.5
1.2
6.0
0.07
0.07
0.07
0.07
0.07
0.06
0.06
0.06
0.12

Pulse Latch Waveforms

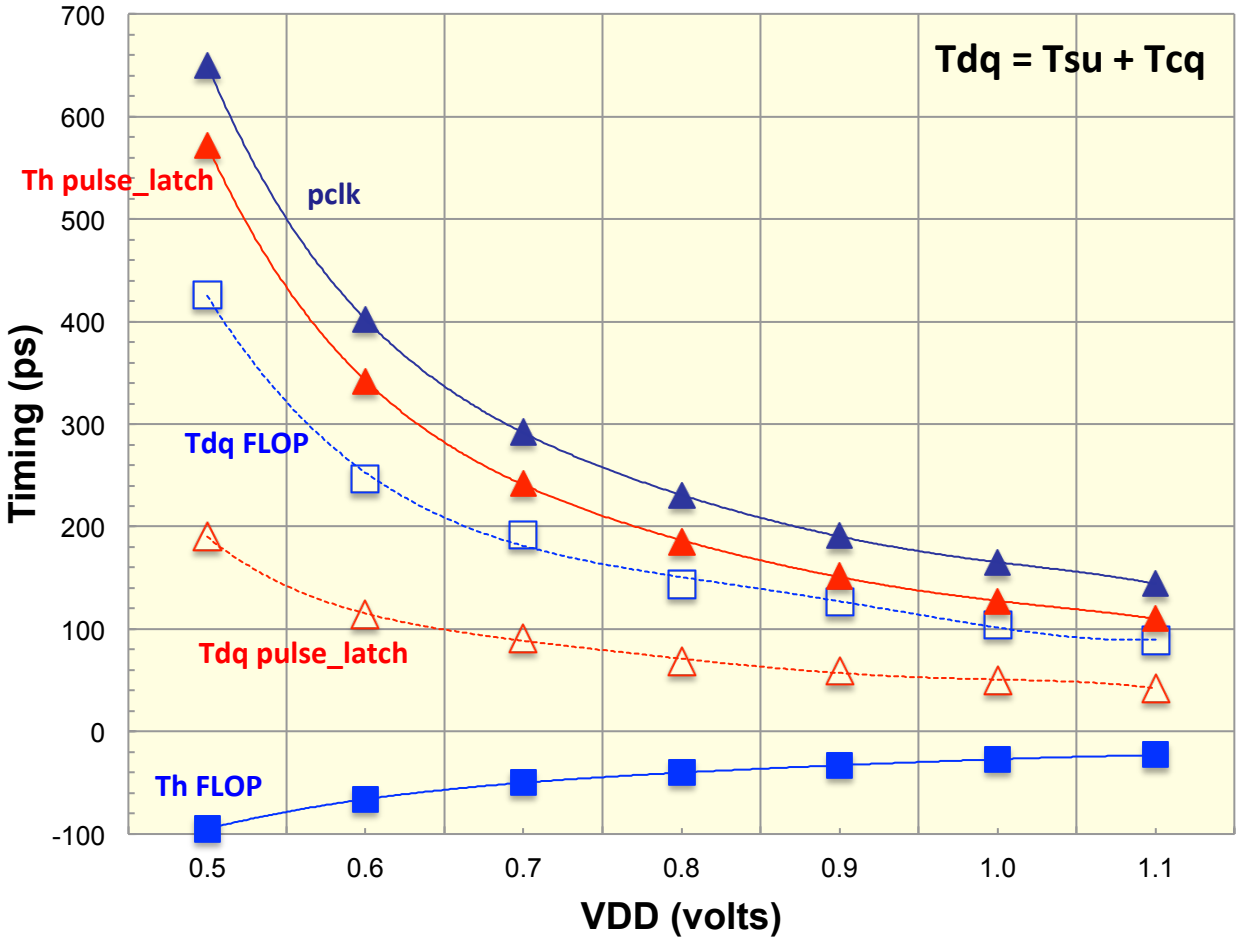
TIMING:
Sampling Window ~ AND + τ
Tsu ~ 0 to ~ –Pclk width
Th ~ sampling window
Tcq ~ 2 inverters + pass gate after Din



Pulse Latch Characterization

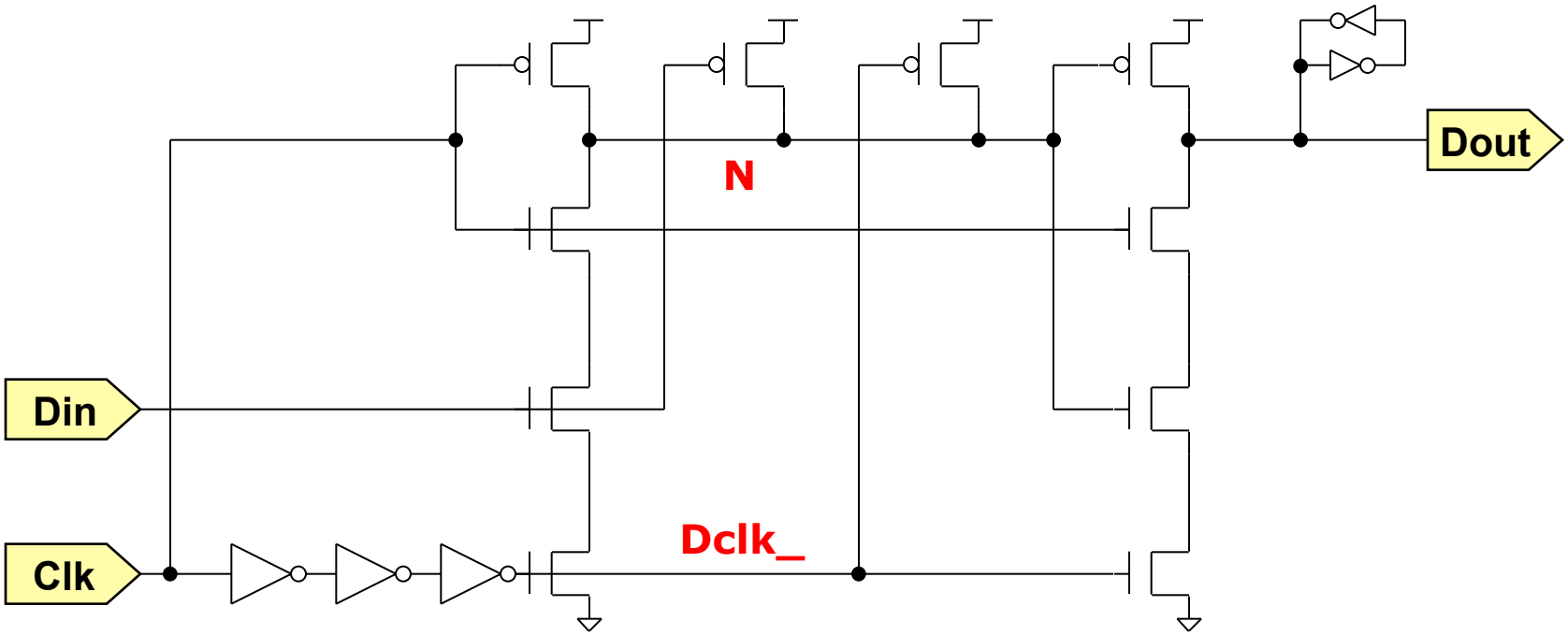


Pulse Latch Comparison with FLOP



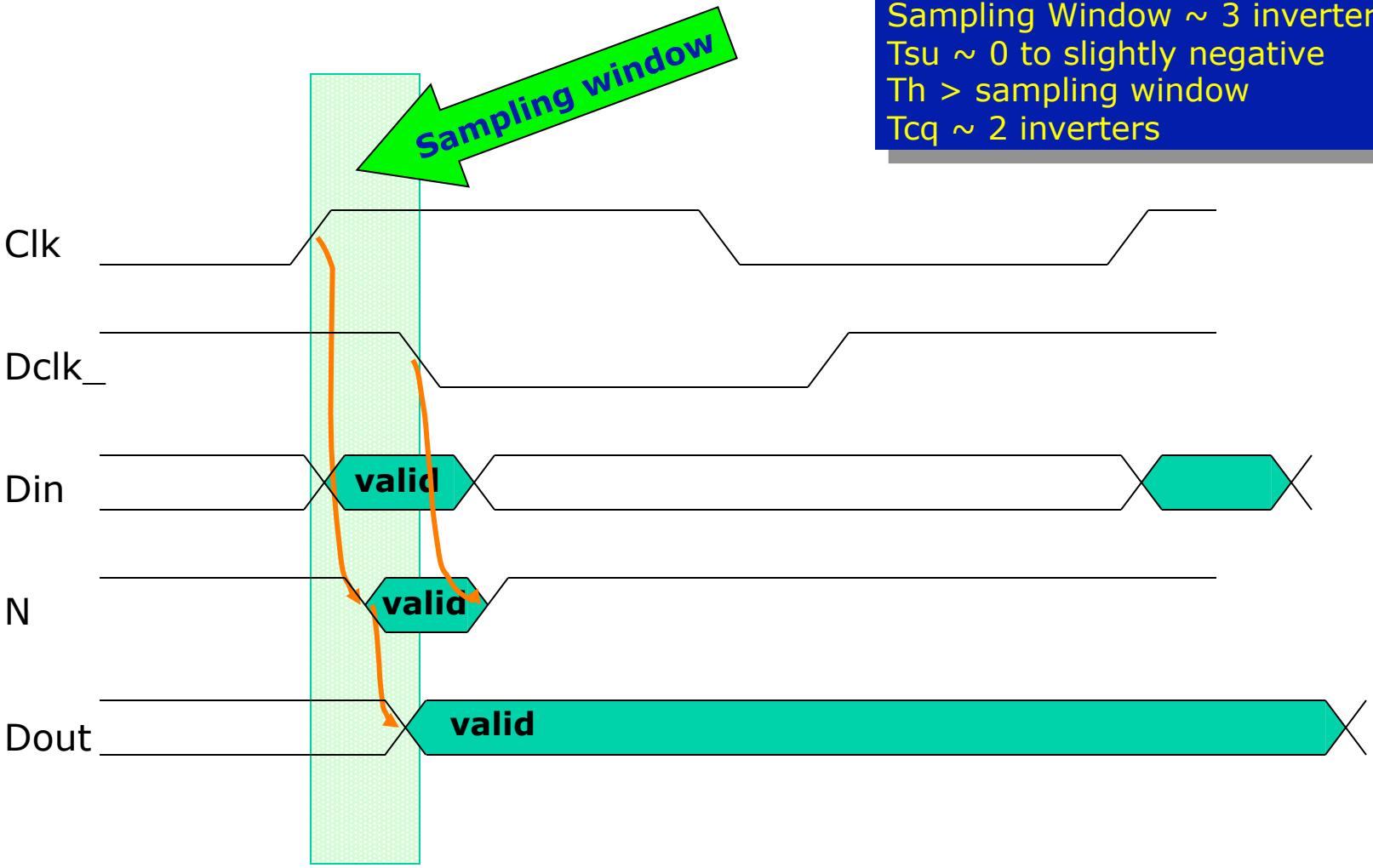
Hybrid Latch Flip-Flop (HLFF)

(AMD K-6, Partovi, ISSCC 1996)

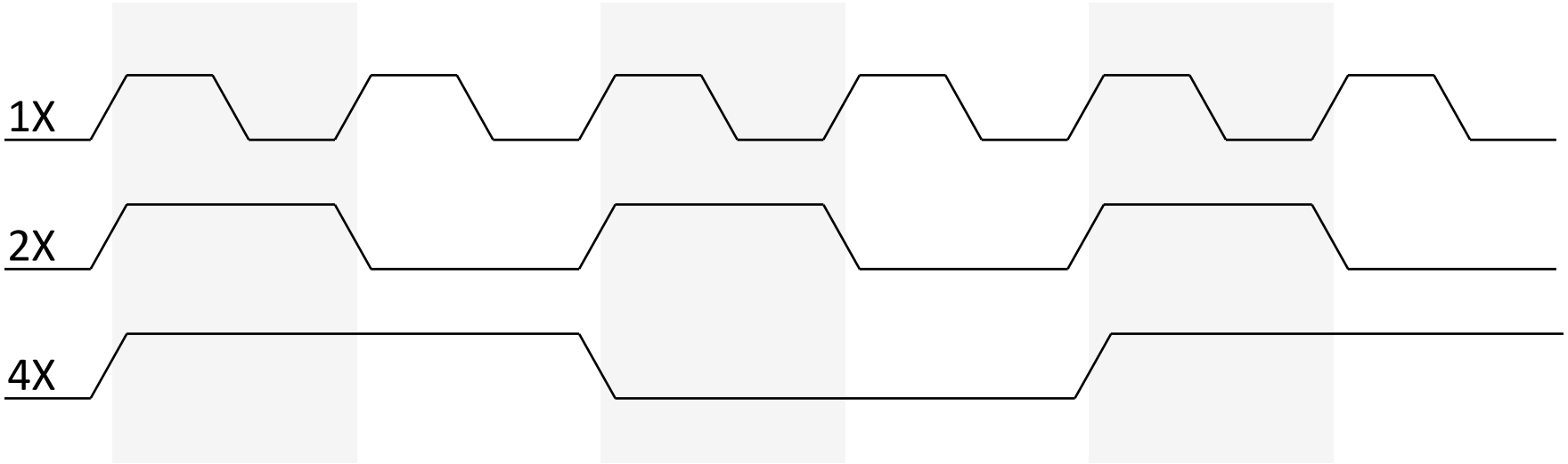


Hybrid Latch Flip-Flop (HLFF) Waveforms

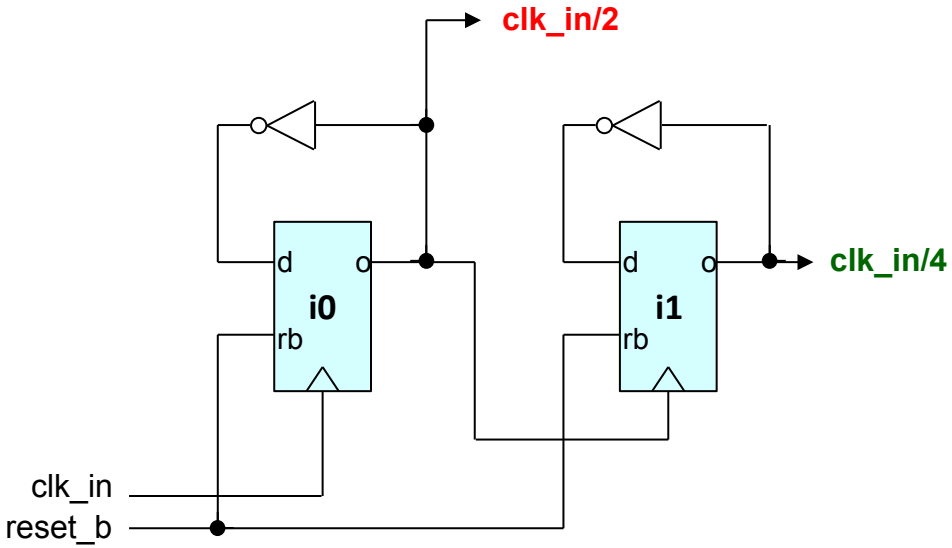
TIMING:
Sampling Window ~ 3 inverters
Tsu ~ 0 to slightly negative
Th > sampling window
Tcq ~ 2 inverters

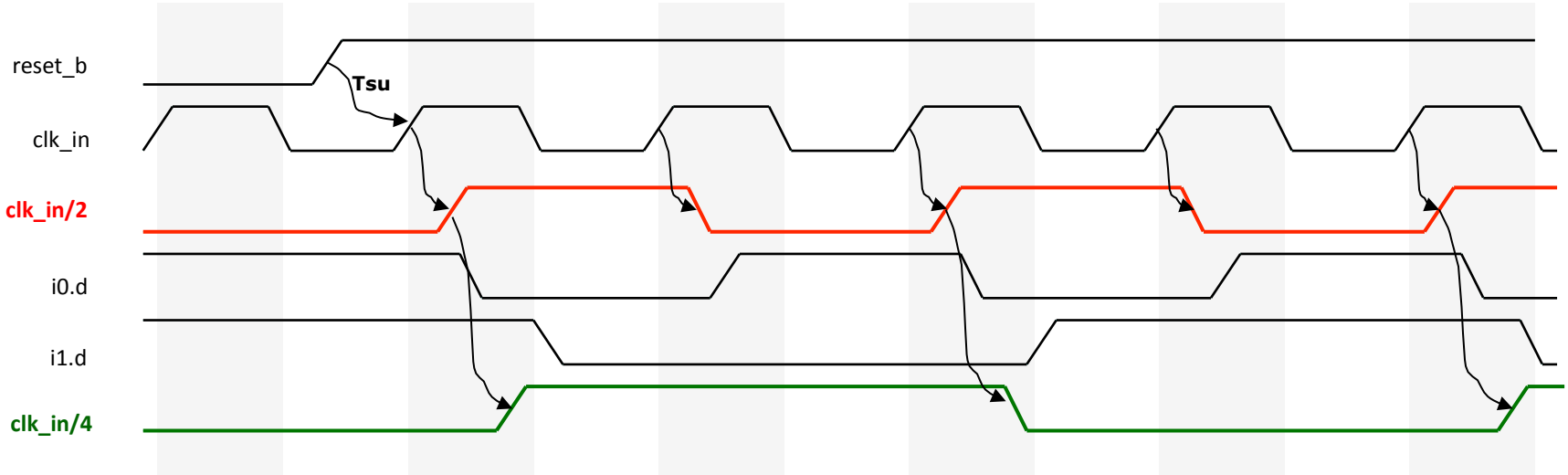


CLOCK DIVISION Using FLOPs

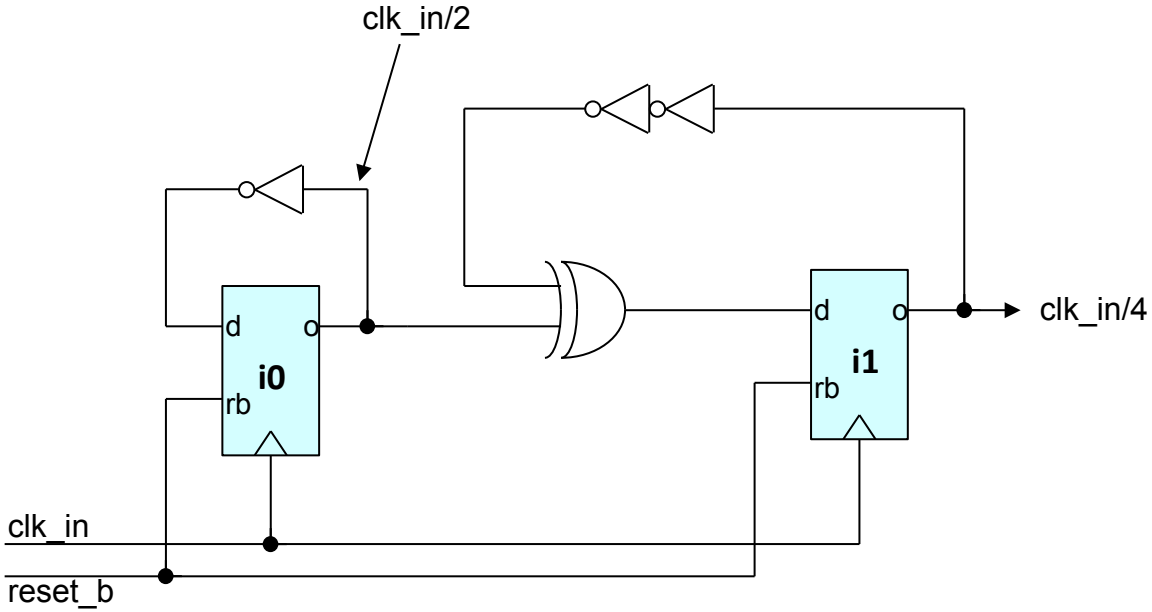


SIMPLE divide-by-2 and divide-by-4





Divide-by-4 using an XOR Gate



reset_b

clk_in

clk_in/2

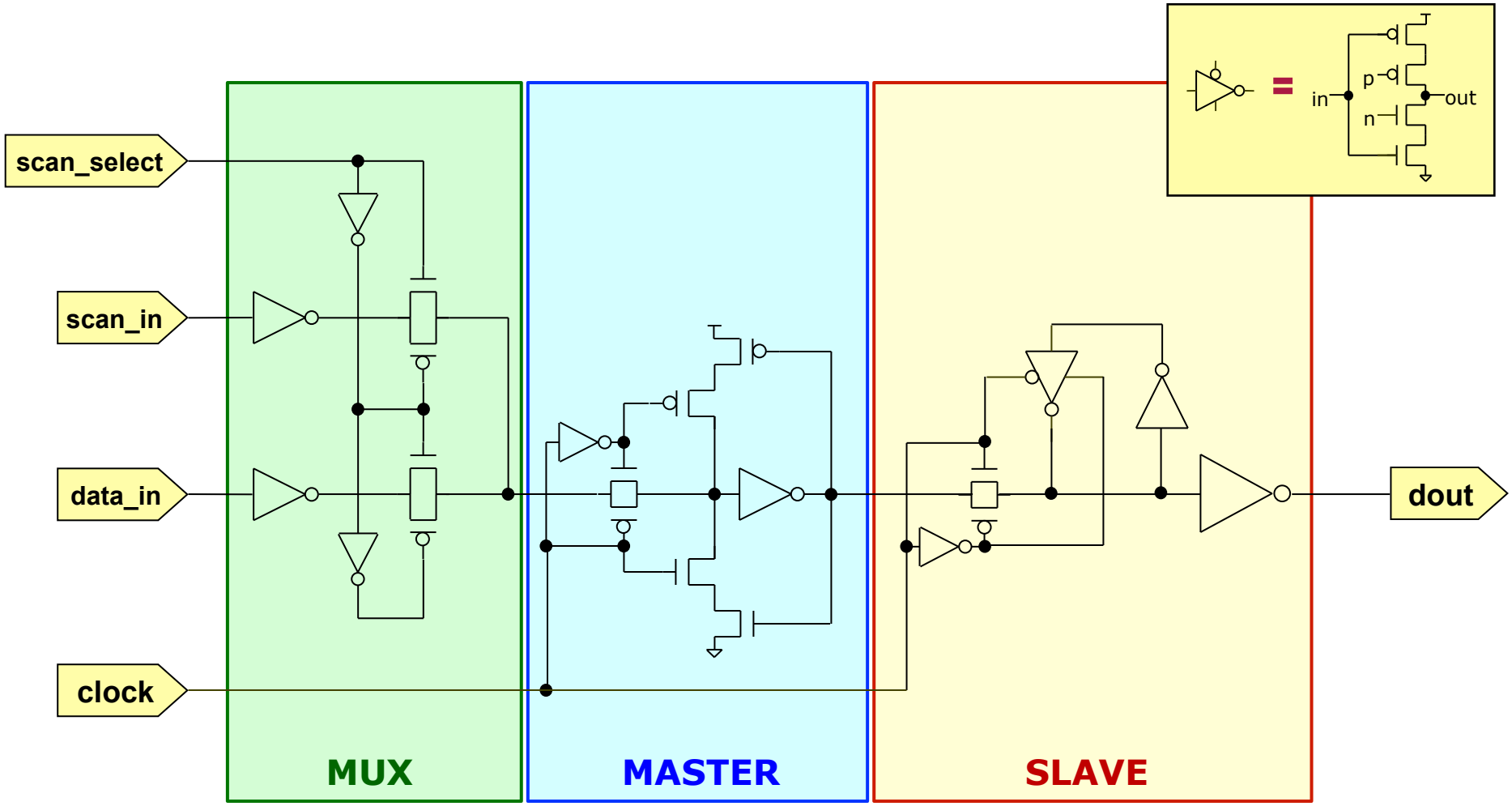
i0.d

i1.d

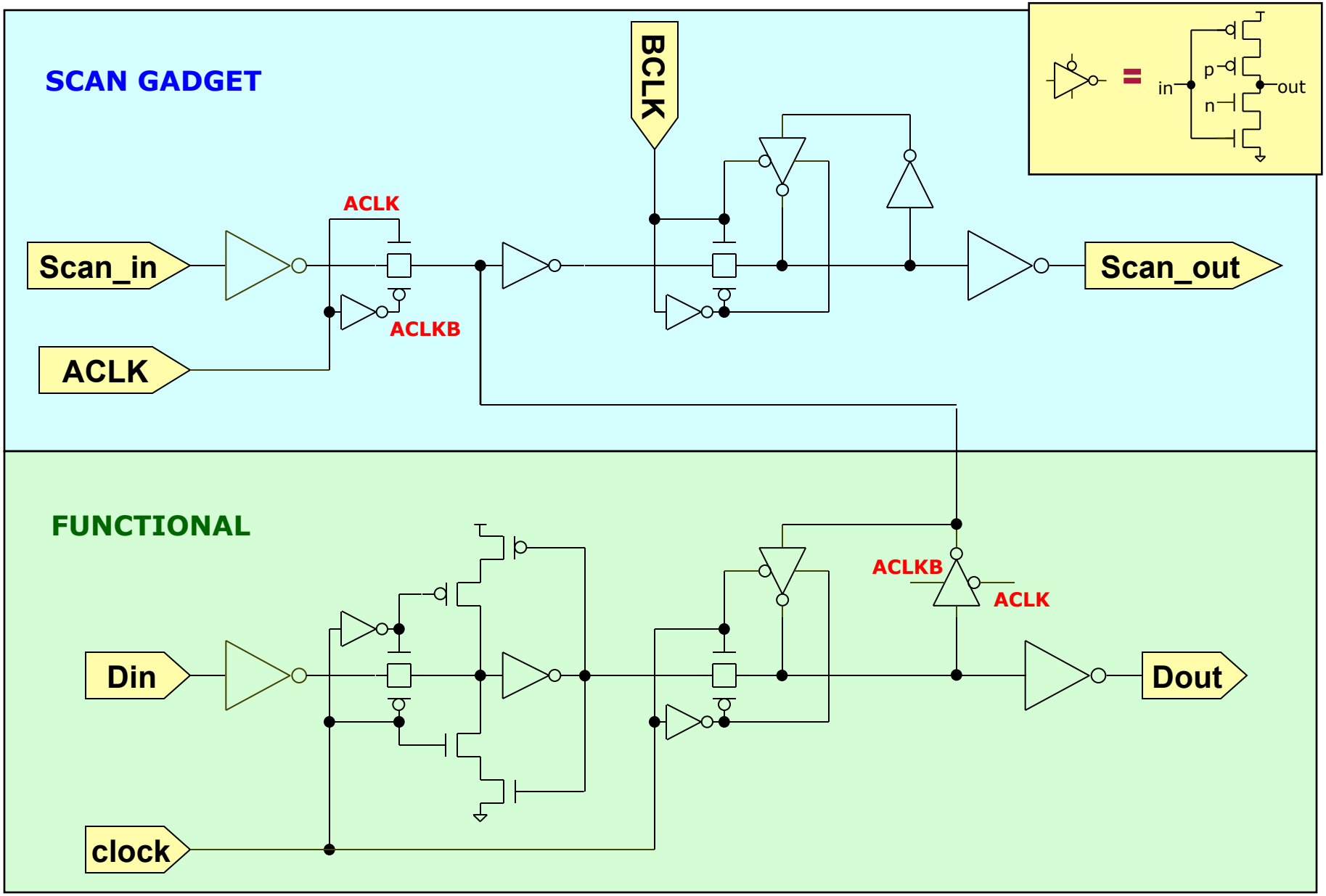
clk_in/4

Exercise for the student:
How is this implementation different (timing wise) to the prior one?

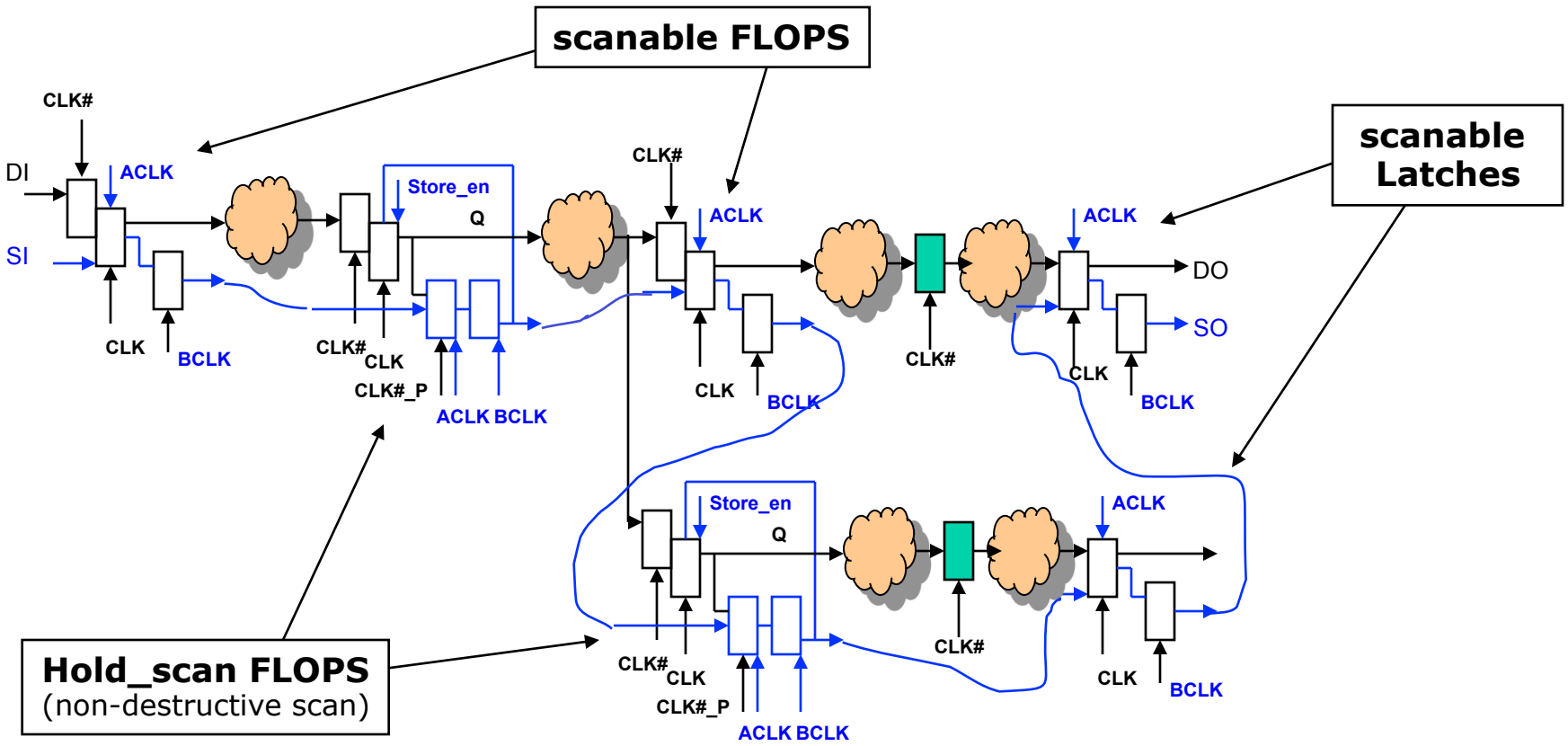
FLOP with SCAN (MUX-FLOP)



High Performance FLOP with SCAN



A Typical Scan Path



References

1. A. Chandrakasan, W.J. Bowhill, F. Fox, Design of High-Performance Microprocessor Circuits, IEEE Press, New York, 2001. Chapter 11 "Clocked Storage Elements" by Hamid Partovi, pages 207-234.
2. V. G. Oklobdzija, The Computer Engineering Handbook, CRC Press, Boca Raton, Florida, 2002. Chapter 10.2 "Latches and Flip-Flops" by Fabian Klass, pages 10.34-10.69.
3. R. J. Baker, H.W. Li, D.E. Boyce, CMOS Circuit Design, Layout, and Simulation, IEEE Press, New York, 1998. Chapter 13, pages 255-274.
4. V. G. Oklobdzija et. al. , Digital System Clocking: High-Performance and Low-Power Aspects, A Wiley-IEEE Press Publication, 264 pages, 2003.

Reference 2 has a very nice treatment of FLOPS/LATCHES, MIN/MAXDELAY, SKEW, etc with plenty of timing diagrams.

BACKUP

Transfer-Gate (T-G) Master-Slave FLOP

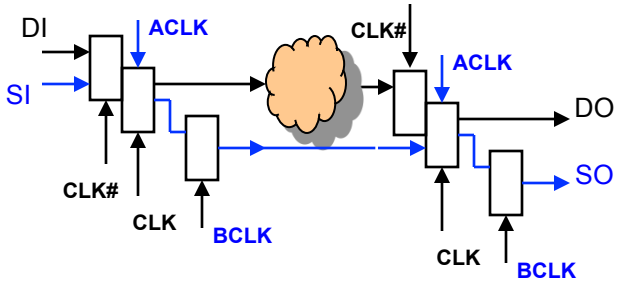
- Low power feedback
- Un-buffered inputs
  - input capacitance depends on the phase of the clock
  - over-shoot and under-shoot with long routes
  - Wire length must be restricted at the input
- Buffered input addresses above issues
- Low power
- Small clk-output delay, but positive setup
- Easily embedded scan, mux, other simple functions

Hybrid Latch Flip-Flop Highlights

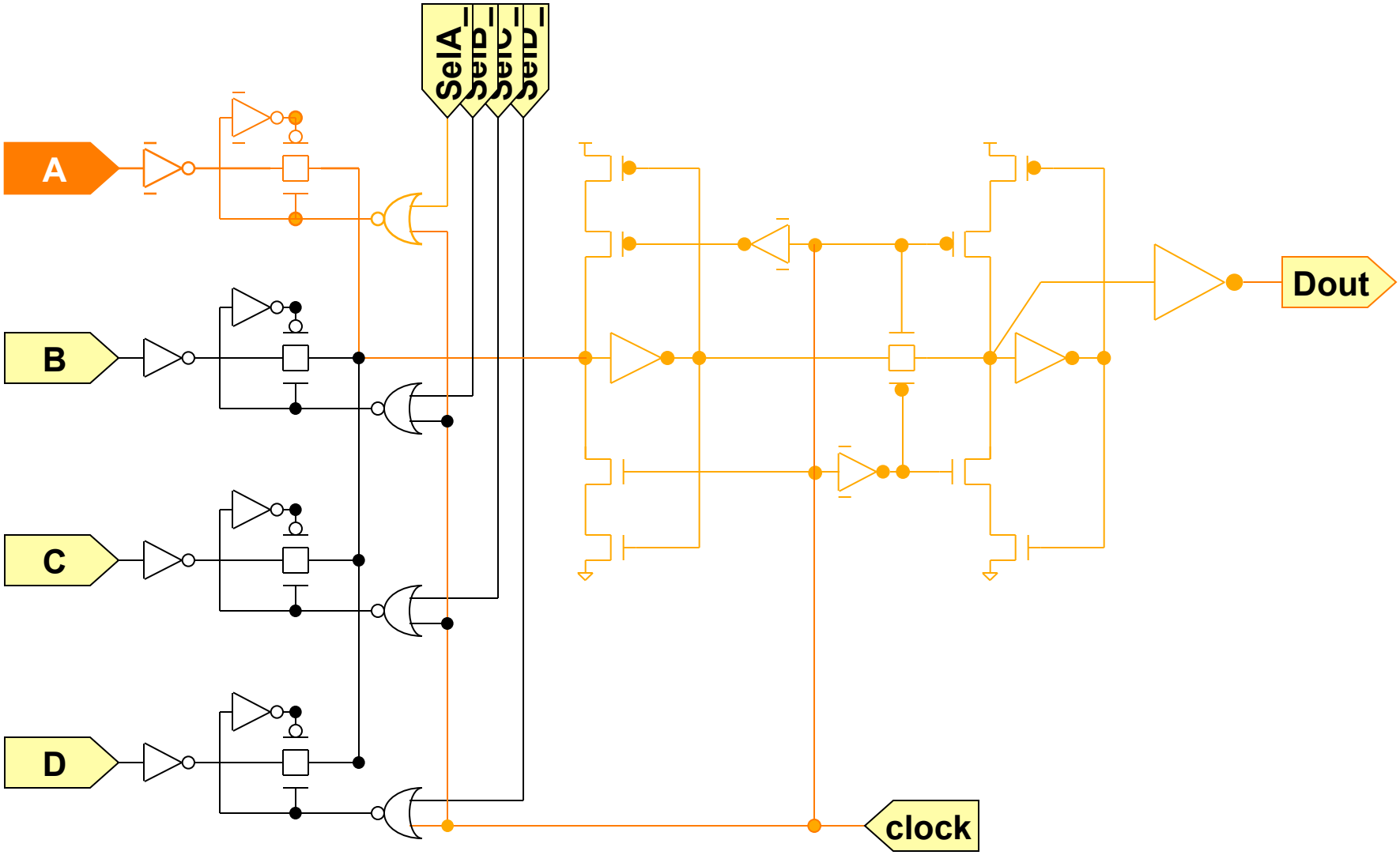
- **Flip-flop features:**
  - single phase clock
  - edge triggered, on one clock edge
- **Latch features: Soft clock edge property**
  - brief transparency, equal to 3 inverter delays
  - negative setup time
  - allows slack passing
  - absorbs skew
  - minimum delay between flip-flops must be controlled
- **Fully static**
- **Possible to incorporate logic**

ATPG Sequence Timing

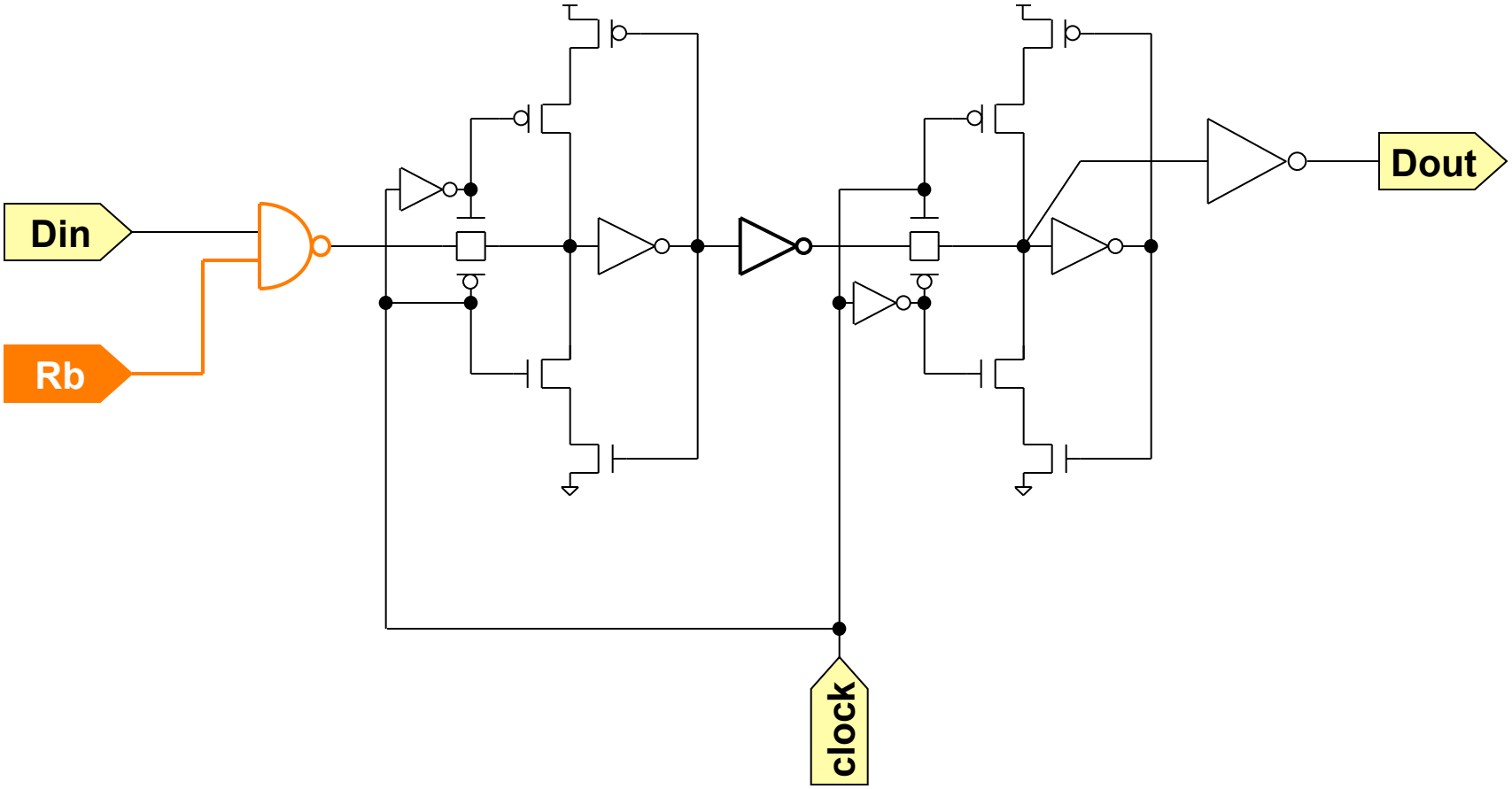
Aclk, Bclk Freq = 1/16 GCLK



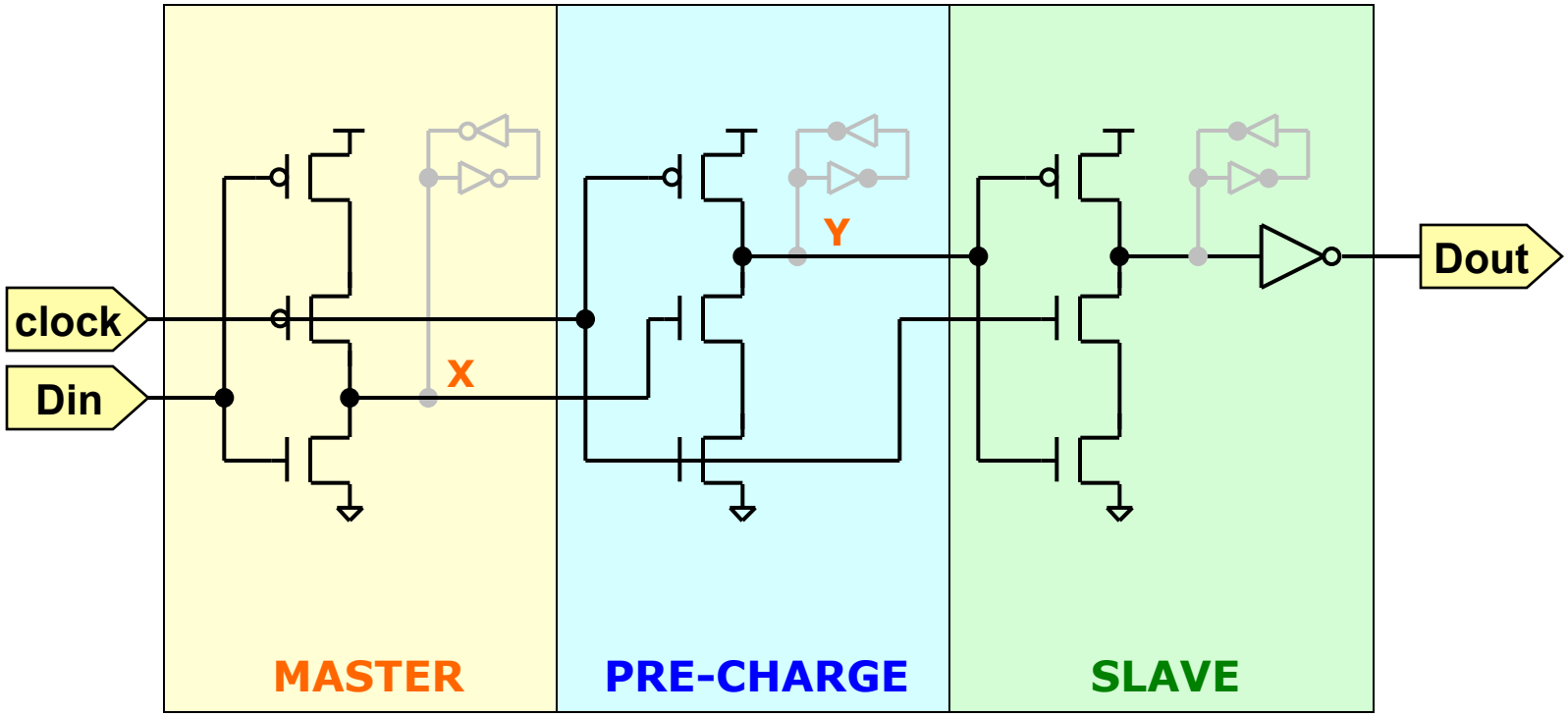
Merged Function MUX-FLOP



Another RESETABLE Master-Slave FLOP (synchronous)

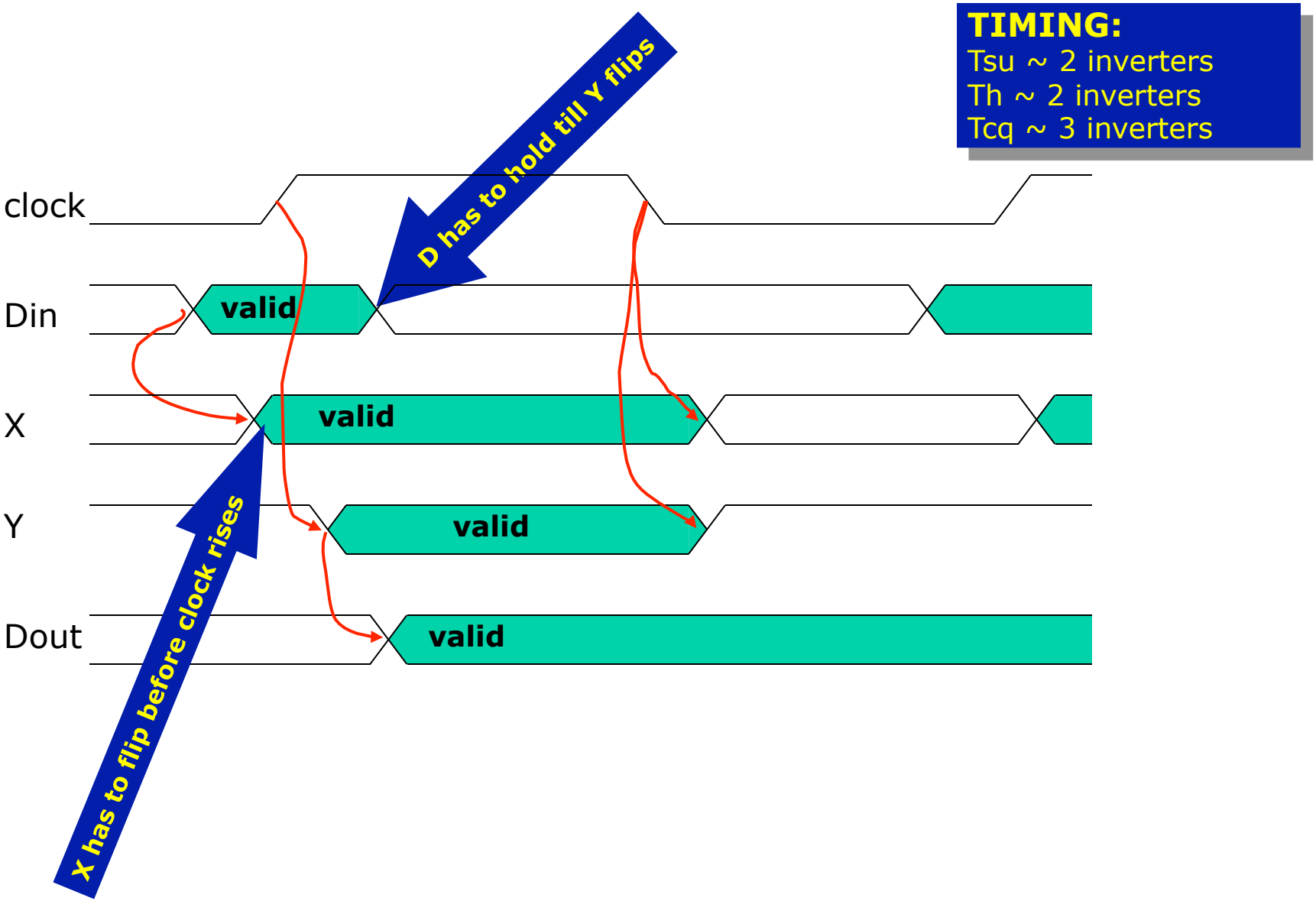


True Single-Phase Clock (TSPC) FLOP



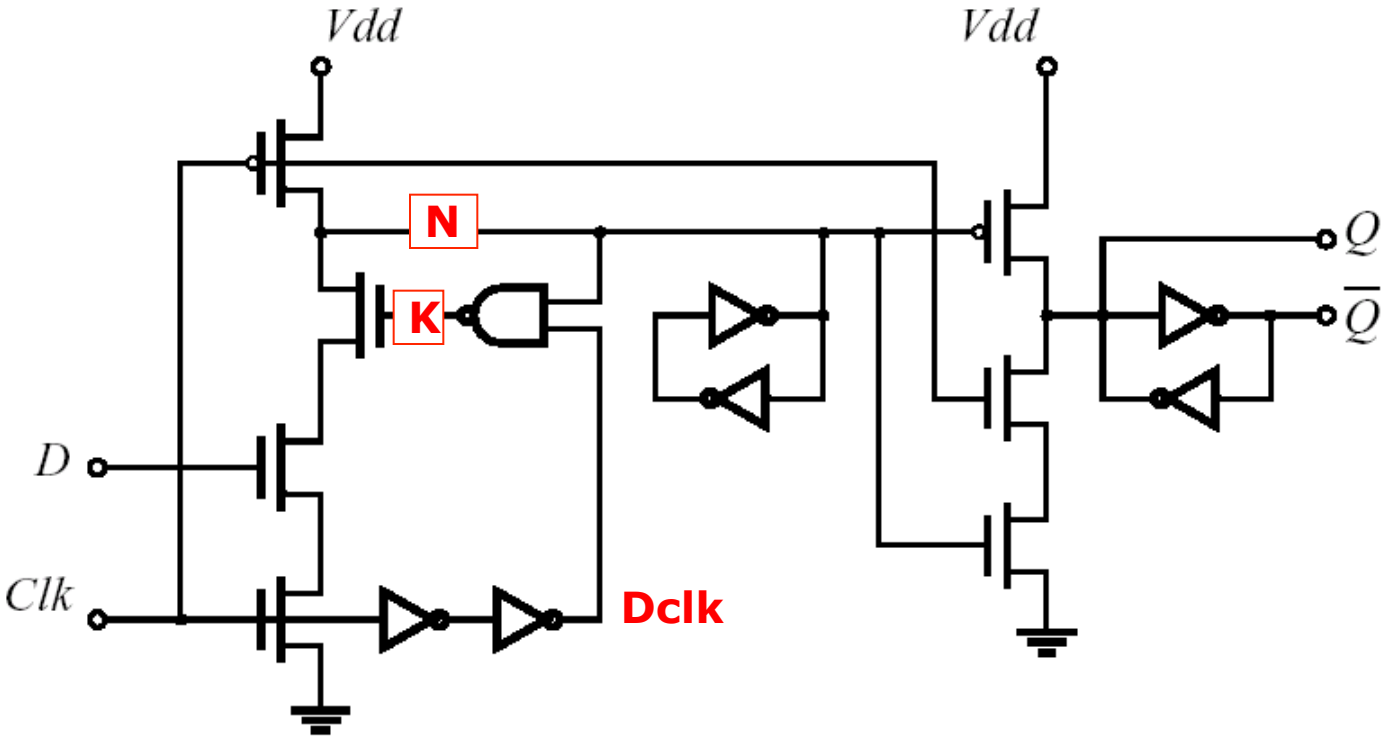
Clock power is low; no local inversion required.

True Single-Phase Clock FLOP Waveforms



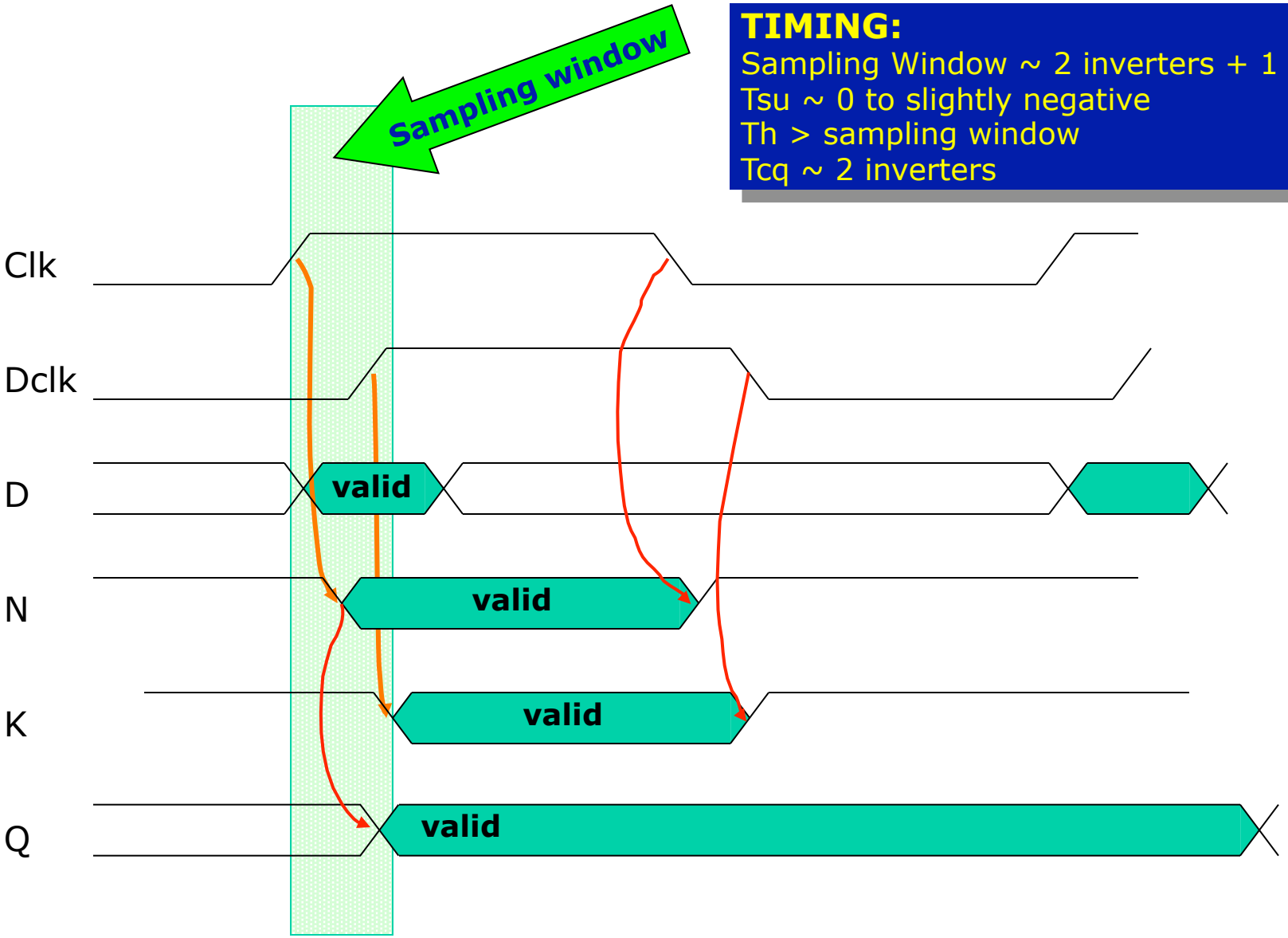
Semi-Dynamic Flip-Flop (SDFF)

- Sun UltraSparc III, Klass, VLSI Circuits'98



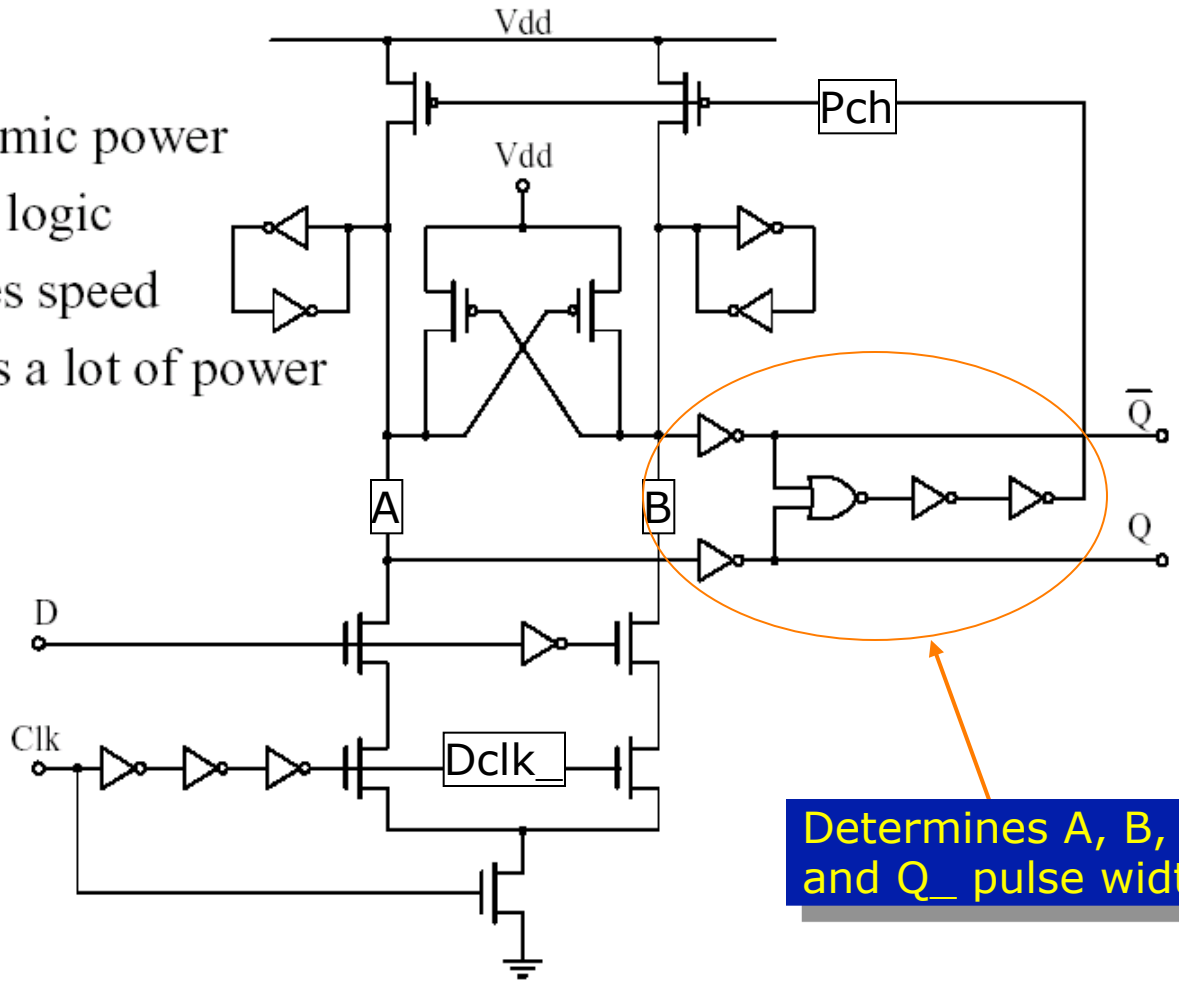
- Soft edge conditioned by data since first stage is pre-charged - cross-coupled latch is added for robustness
- Small penalty for adding logic
- Latch has one transistor less in stack - faster than HLFF, but 1-1 glitch exists

Semi-Dynamic Flip-Flop Waveforms



K-6 Dual-Rail ETL

- Self-reset property
  - increases dynamic power
  - drives domino logic
- Precharge increases speed
- Very fast but burns a lot of power
- Small clock load



K-6 Dual-Rail Waveforms

TIMING:
Sampling Window ~ 3 inverters
Tsu ~ 0 to slightly negative
Th > sampling window
Tcq ~ 2 inverters