VLSI 2 – ICC TUTORIAL

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ICC Tutorial Agenda

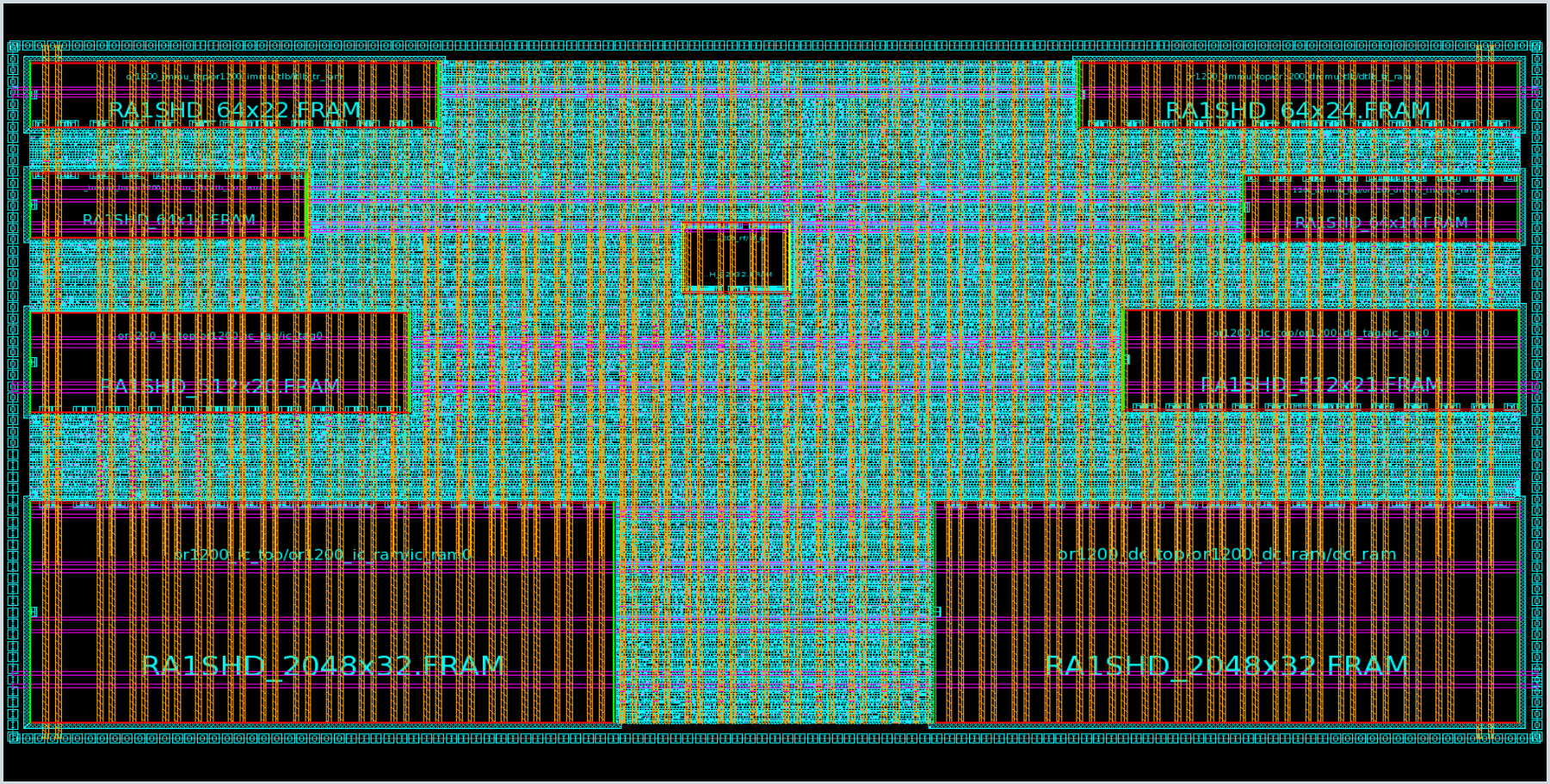
- Introduction to ICC
- ICC Design Flow
- Using the GUI
- Project Suggestions
- ICC Demonstration

Introduction to ICC

- ICC is:
  - Part of Synopsys's Galaxy Implementation Platform used for designing integrated circuits
  - A tool used for physical implementation of integrated circuits
- ICC is used to transform a gate-level netlist into a placed and routed layout that can be fabricated
- ICC inputs:
  - Synthesized gate-level netlist
  - Standard Cell Library
- ICC outputs:
  - Integrated circuit layout
- ICC user interfaces:
  - tcl commands through scripts or command line
  - GUI visual interface

Introduction to ICC

- Example of Layout Generated with ICC



ICC Design Flow: Overview

- Data Setup
- Floorplan Initialization and Placement
- Power Grid Synthesis and Analysis
- Clock Tree Synthesis and Design Routing
- LVS and DRC Verification
- Report Generation

ICC Design Flow: Data Setup

- Use tcl scripts for Data Setup
- Libraries to Setup
  - Logical Libraries (*.db): provide timing and functionality information for all standard cells and hard macros
  - Physical Libraries (*.mw): contain physical information of standard cells, macros, and pad cells necessary for placement and routing
  - Technology File (*.tf): contains metal layer technology parameters such as design rules for each layer/via
  - TLU+ Parasitic RC Model File (*.tlup): used to calculate RC delay values using net geometries
  - Design Milky Way file (*.mw): the Milky Way design library that will contain your OR1200 design

ICC Design Flow: Data Setup

- To Run the tcl Script and Save the Output Log File
  - At the UNIX prompt, type
    - module load synopsys/icc
    - icc_shell –f <name_of_tcl_script> | tee <log_file_name>
- Useful tcl Commands
  - set search_path
  - set target_library
  - set link_library
  - create_mw_lib

ICC Design Flow: Floorplan Initialization and Placement

- Use GUI
- Suggested Procedure
  - Specify pin/pad placement and dimensions
  - Initialize floorplan with core dimensions and overall dimensions
  - Place hard macros and specify standard cell placement blockages
  - Optional: write out hard macro placement coordinates to a text file for reuse in future iterations
  - Place standard cells using desired optimization algorithm
  - Fill empty spaces in between standard cells with filler cells
  - Perform congestion analysis to ensure that current placement is likely to be routable

ICC Design Flow: Floorplan Initialization and Placement

- Useful tcl Commands
  - set_pin_physical_constraints
  - initialize_floorplan
  - create_placement
  - legalize_placement
  - place_opt
  - insert_stdcell_filler
  - route_zrt_global –congestion_map_only true –effort low
  - write_floorplan -placement

ICC Design Flow: Power Grid Synthesis and Analysis

- Use GUI
- Suggested Procedure
  - Preroute standard cells to create Metal 1 power and ground straps
  - Route Metal 5 power and ground straps and verify appropriate connections
  - Route Metal 6 power and ground straps and verify appropriate connections
  - Perform congestion analysis
  - Perform Voltage Drop (aka IR drop) analysis
  - Read "ICC_Readme_Fall12.txt" file for more details on each of the steps listed above. This file can be found in the following directory: /home/projects/courses/fall_12/ee382m-17005/project_fall_12/fall_12_Archive/Readme

ICC Design Flow: Power Grid Synthesis and Analysis

- Useful tcl Commands
  - derive_pg_connection –power_net VDD –power_pin VDD –ground_net VSS –ground_pin VSS
  - set_preroute_drc_strategy
  - preroute_standard_cells
  - create_power_straps
  - analyze_fp_rail

ICC Design Flow: Clock Tree Synthesis and Design Routing

- Use GUI
- Clock Tree Synthesis Suggested Procedure
  - Set clock tree options and constraints
  - Synthesize all clocks required by design
  - Perform clock optimization
  - Connect synthesized clock cells to power and ground
  - Perform congestion analysis
- Design Routing Suggested Procedure
  - Specify routing constraints
  - Route design
  - Perform route search and repair to repair any design rule violations

ICC Design Flow: Clock Tree Synthesis and Design Routing

- Useful tcl Commands
  - set_clock_tree_options
  - create_clock
  - clock_opt
  - route_opt
  - route_search_repair

ICC Design Flow: LVS and DRC Verification

- Use GUI
- LVS and DRC Verification Suggested Procedure
  - Verify LVS (Layout vs. Schematic) and address any errors
  - Verify DRC (Design Rules Check) and address any errors
  - View errors using Error Browser
- Useful tcl Commands
  - verify_lvs –ignore_floating_port
  - verify_drc

ICC Design Flow: Report Generation

- Use GUI or tcl script
- Generate and Examine the Following Reports
  - Design report: list of design attributes
  - Area report: lists area statistics including combinational, non-combinational, and total area
  - Timing report: reports the single worst setup path in each clock group. Use this report to determine slack violations.
  - Power report: uses user-annotated switching activity to calculate the net switching power, cell internal power, and cell leakage power
  - Port report: displays information about all the ports of the design
  - spef output: RC parasitic file used by Primetime for timing analysis

ICC Design Flow: Report Generation

- Useful tcl Commands
  - report_design
  - report_area
  - report_timing
  - report_power
  - report_port
  - write_parasitics

Using the GUI

- Launching the GUI
  - At the UNIX prompt, type
    - module load synopsys/icc
    - icc_shell –gui
- Opening the Design (i.e. the Milky Way Library)
  - Specify the search path and the link libraries by copying the following lines from the tcl scripts to the GUI command line
    - set project_dir “<enter_your_project_dir_here>”
    - set search_path “<enter_your_search_path_here>”
    - set link_library “<enter_your_link_library_here>”
  - Open the Milky Way Library using File → Open Library
  - Open the design using File → Open Design
- Use the “man” and “help” commands in the command line to get more information on any given command

Project Suggestions

- Read all of the read me files in the following directory: /home/projects/courses/fall_12/ee382m-17005/project_fall_12/fall_12_Archive/Readme
- Layout is a visual design process; so use the GUI extensively
- Script Notes
  - Use provided ICC scripts to setup your libraries ONLY
  - Don't trust the provided ICC scripts except for library setup
  - Write your own ICC scripts once you are familiar with the ICC GUI and what each command does
  - Read the "ICC_Readme_Fall12.txt" file for more information on each of the scripts that will help you get started
- The memory macros are needed by both DCC and ICC; so these should be synthesized as early as possible

Project Suggestions

- Save your design with a new name after each step in the ICC Design Flow (use the "save_mw_cel –as <design_name>" tcl command)
  - For example, after the Floorplan Initialization and Placement, save your design as "or1200_top_placement"
  - For the Power Grid Synthesis and Analysis, start with the "or1200_top_placement" design and create your power grid. Once the power grid has been synthesized, save the design as "or1200_top_power_grid"
- Review and understand all Warnings and Errors generated in the log files
  - Decide if Warnings are critical
  - All Errors are critical and should be resolved
- Create your own directory in the /scratch folder. Run ICC from this directory

ICC Demonstration

- Introduction to Scripts
- Run Scripts
- Review Output Log for Errors and Warnings
- Open Design in GUI
- Manually Place Macros
- Write Out Macro Placement Coordinates to Text File
- Save Design
- Close Design and GUI