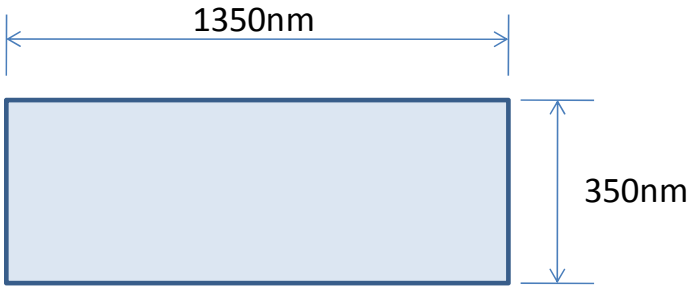
Problem 1 (20 Points)
Determine the capacitances for the following structures:

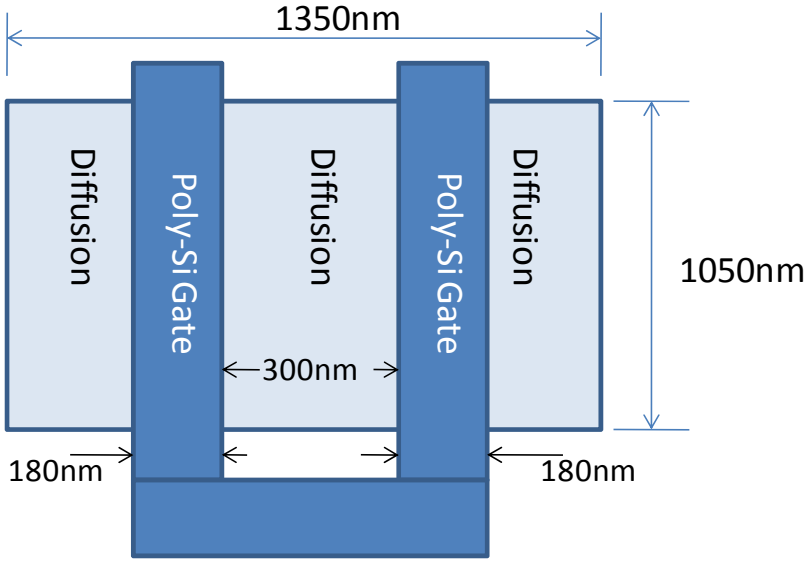
a) Diffusion capacitance



Where: C_{bottom} = 23 ff/μ^2 and $C_{sidewall}$ = 10 ff/μ

Total DIFFUSION Capacitance= **10.86ff + 34.00ff = 44.86ff**

b) Gate and Diffusion Capacitances



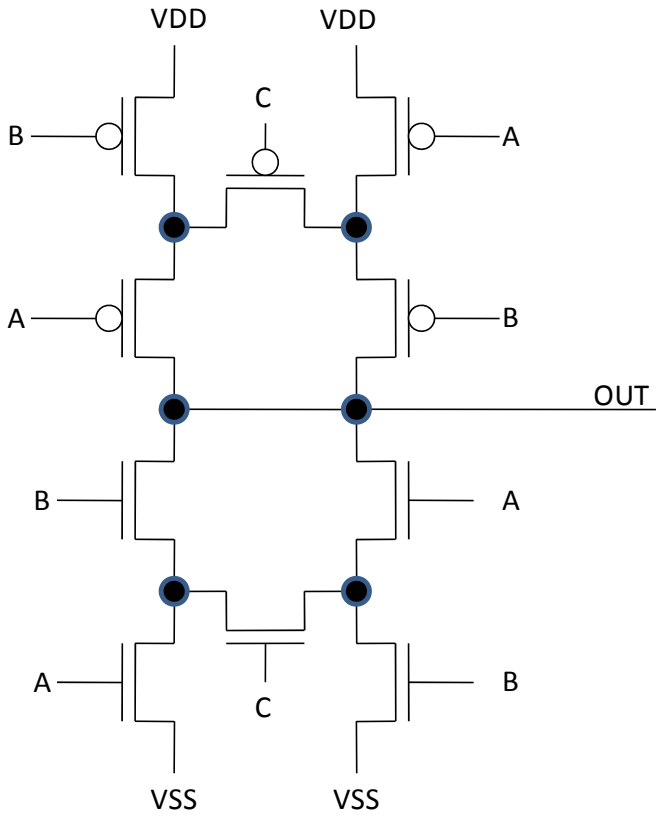
Where: C_{bottom} = 29 ff/μ^2 $C_{sidewall}$ = 15.5 ff/μ C_{gate} = 11.6 ff/μ^2

Total DIFFUSION Cap= **128.34ff (sidewall) + 30.14ff (bottom) = 158.49ff**

Total GATE Cap = **2.1924ff + 2.1924ff = 4.3848ff**

Problem 2. Transistor Mapping & Sizing (20 Points)

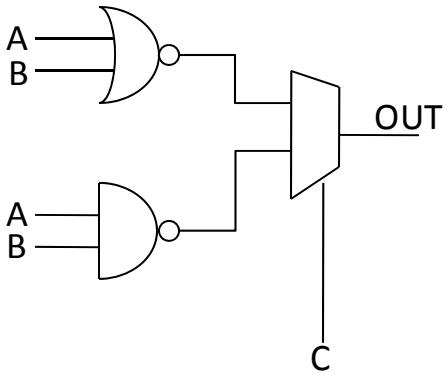
a) What is the truth table for the following circuit?



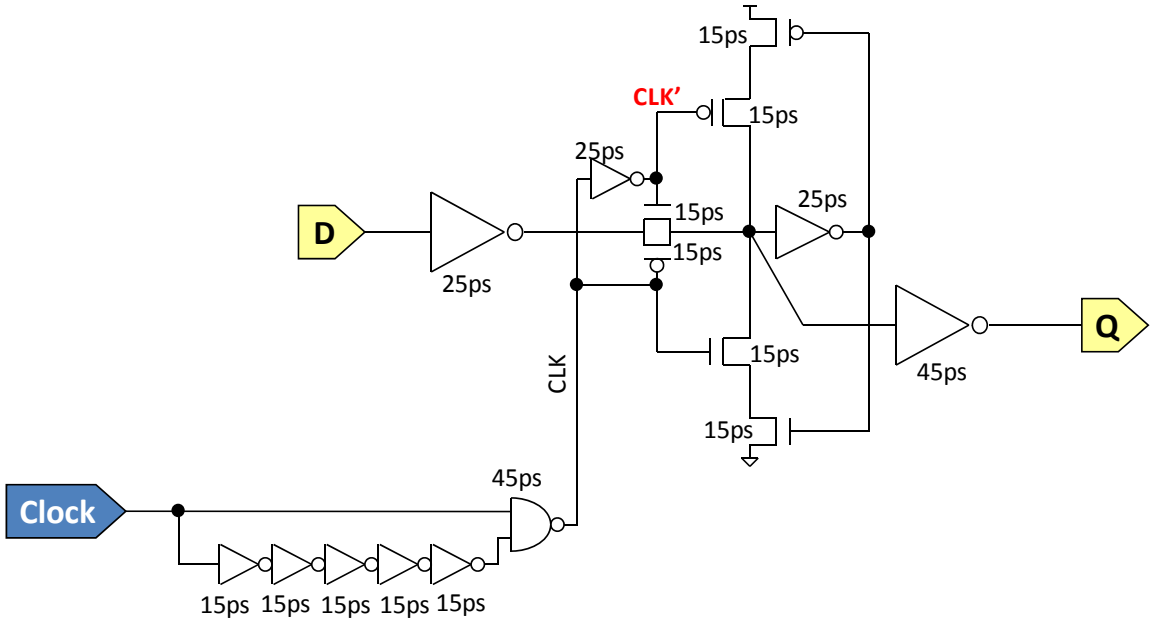
A	B	C	OUT
0	0	0	1
0	1	0	1
1	0	0	1
1	1	0	0
0	0	1	1
0	1	1	0
1	0	1	0
1	1	1	0

b) Size the transistors so that they can drive a load which is 3X minimum size inverter. **PMOS = 6 NMOS = 3** assuming a fanout of 3.

c) Draw the logic gate equivalent of this circuit



Problem 3: Sequential Elements (20 Points)



NOTE: Critical timing is from Clock to CLK' Time from Clock to CLK' is 145ps for CLK' going low and 70ps for CLK' going high.

a) What is the T_{setup} time

25ps + 15ps + 25ps + 15ps – 145ps = -65ps

NOTE: negative setup time is typical of a pulse latch

b) What is the T_{hold} time?

145ps -25ps = 120ps

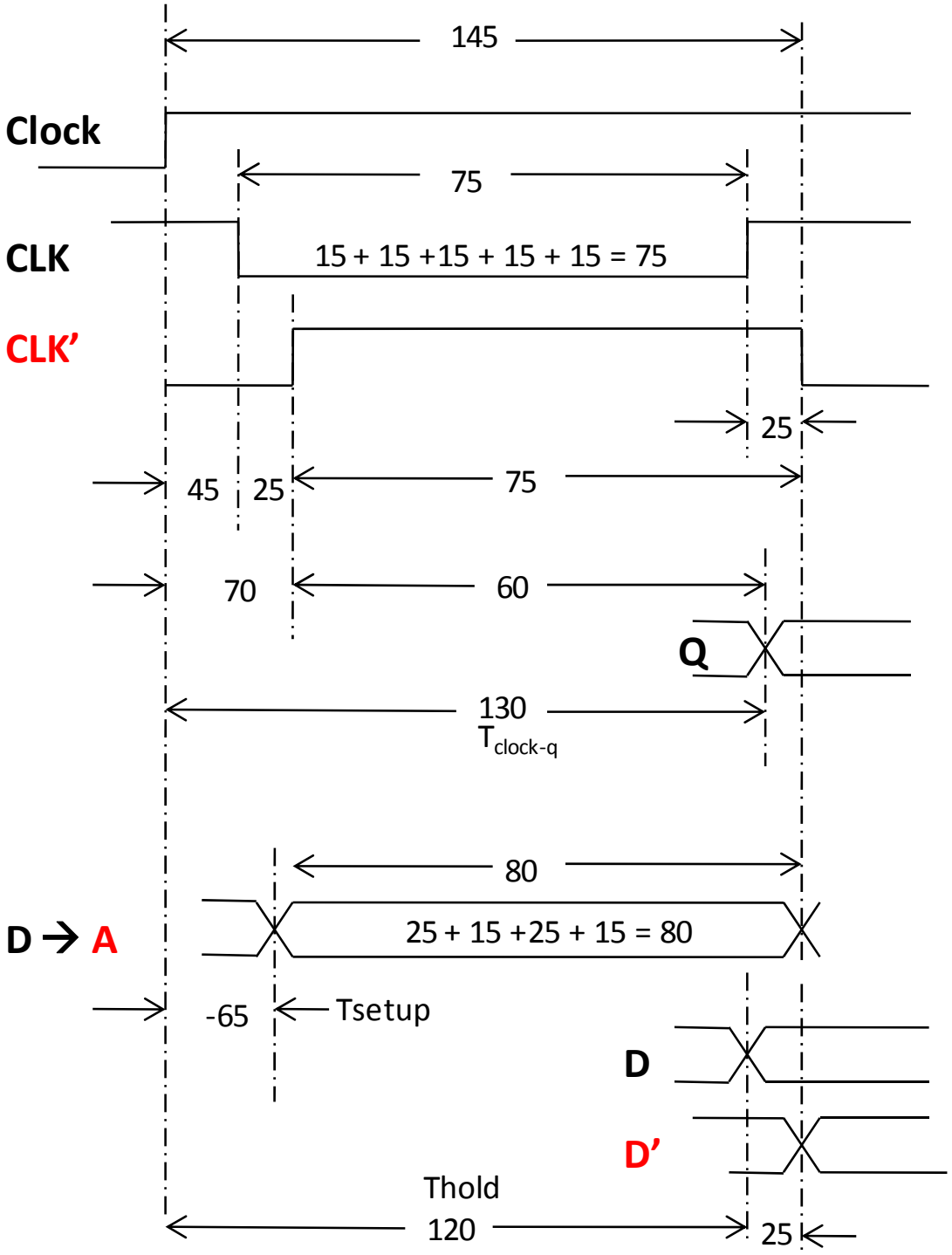
NOTE: Excessive hold times are typical of a pulse latch

c) What is the $T_{clock\text{-}q}$ time?

70ps + 15ps + 45ps = 130ps

d) What is the pulse width of the CLK signal?

15ps + 15ps + 15ps + 15ps + 15ps = 75ps



NOT TO SCALE (obviously ☺)

Problem 5. Logical Effort (20 Points)

Design a 10-input AND gate network for minimum delay using nothing more than the following standard cell gates:

Gate type	1x	2x	3x
INV	✓	✓	✓
2-NAND	✓	✓	✓
3-NAND	✓	✓	n/a
2-NOR	✓	✓	n/a
3-NOR	✓	✓	n/a

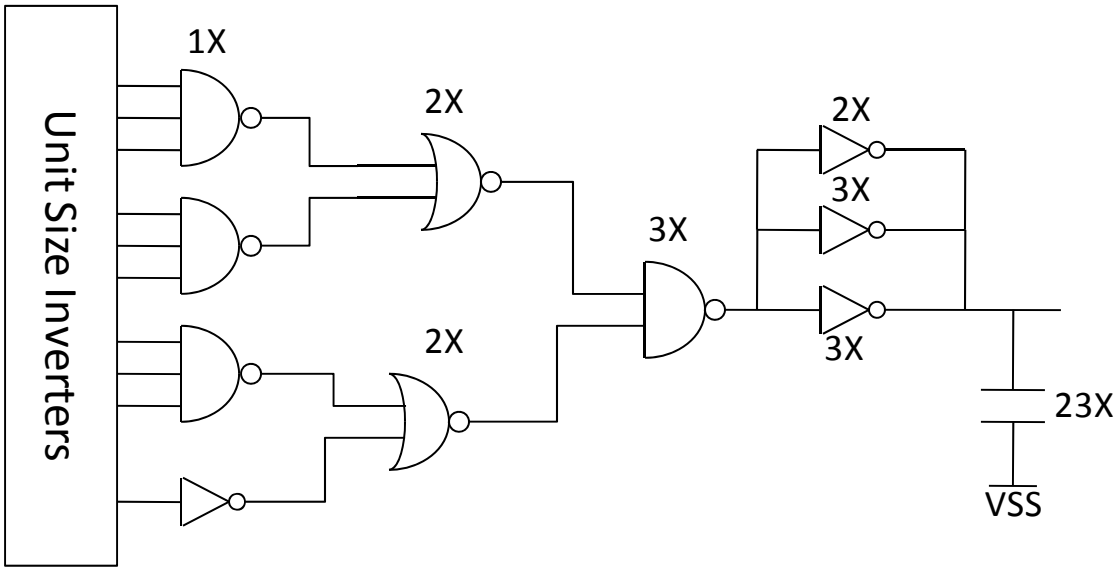
NOTE: n/a indicates not available

The network is driven by unit size inverters and the output is driving a load of 23 unit size inverters. Compute the delay using logical effort technique.

H = 23
B = 1 (No Branching)
Assume 5 stages (including unit size inverter)
INV -> NAND-3 -> NOR2 –> NAND2 -> INV

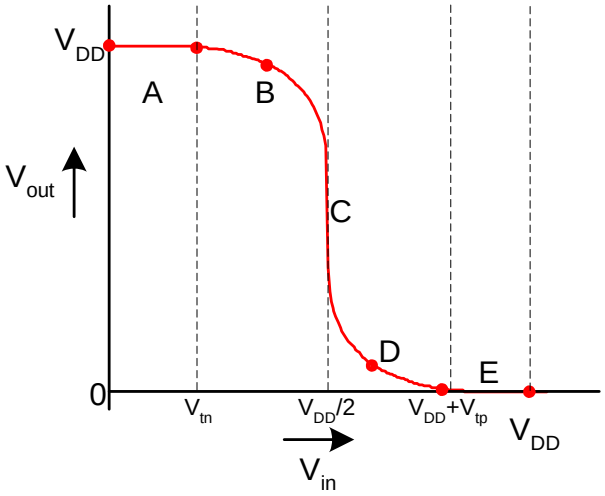
G=1 * 5/3 * 5/3 * 4/3 * 1 = 100/27

F = GBH = 23 * 1 * 100/27 = 106.48
$f = F^{1/5} = 2.43$
D = (5 * 2.54) + 1 + 3 + 2 + 2 + 1 = 21.71 (if we use a fanout of 2.54)
Lets use 3.00 to size gates:
INV = 69/3 ≈ 24 -> 16/8 which is 8X device
NAND2 = 24/3 * 4/3 ≈ 12 which is a 3X device
NOR2 = 12/3 *5/3 ≈ 8 which is a 2X device
NAND3 = 8/3 * 5/3 ≈ 4 which is a 1X device

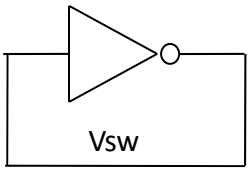


Problem 5. Device Operation (20 Points)

Derive the analytic expression for Vsw where Vout=Vin=Vsw (switch point) for region C for the inverter transfer function shown to the right.



Assume that | Vtp | = Vtn and βn = βp



Recall that the currents through each transistor are equal in the switch point region: $Idsn = -Idsp$

The current through the NMOS device in saturation is: $\frac{\beta n}{2}(Vin - Vtn)^2$

The current through the PMOS device in saturation is: $\frac{\beta p}{2}(Vin - Vdd - Vtp)^2$

The switching point where both transistors are saturated (region C) is found by solving for equal currents. Therefore

$$\frac{\beta n}{2}(Vin - Vtn)^2 = -\frac{\beta p}{2}(Vin - Vdd - Vtp)^2$$

Since βp = βn and |-Vtp| = Vtn we get:

$Vin = \frac{Vdd}{2}$ which is what we expected

The real gnarly solution when Bp ≠ Bn and Vtp ≠ Vtn is shown below

$$\frac{\beta_n}{2}(V_{in} - V_{tn})^2 = \frac{\beta_p}{2}(V_{in} - V_{DD} - V_{tp})^2$$

$$V_{in}^2(\beta_n - \beta_p) + V_{in}(-2\beta_n V_{tn} + 2\beta_p(V_{DD} + V_{tp})) + (\beta_n V_{tn}^2 - \beta_p(V_{DD} + V_{tp})^2) = 0$$

$$V_{in} = \frac{\beta_n V_{tn} - \beta_p(V_{DD} + V_{tp}) + (V_{DD} + V_{tp} - V_{tn})\sqrt{\beta_n \beta_p}}{\beta_n - \beta_p}$$

$$= \frac{V_{DD} + V_{tp} + \sqrt{\frac{\beta_n}{\beta_p}} V_{tn}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$