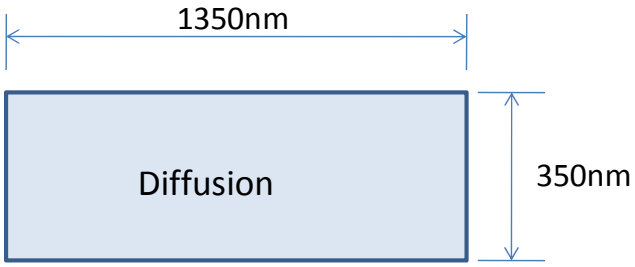
**Problem 1 (10 Points)**
Determine the capacitances for the following structures:

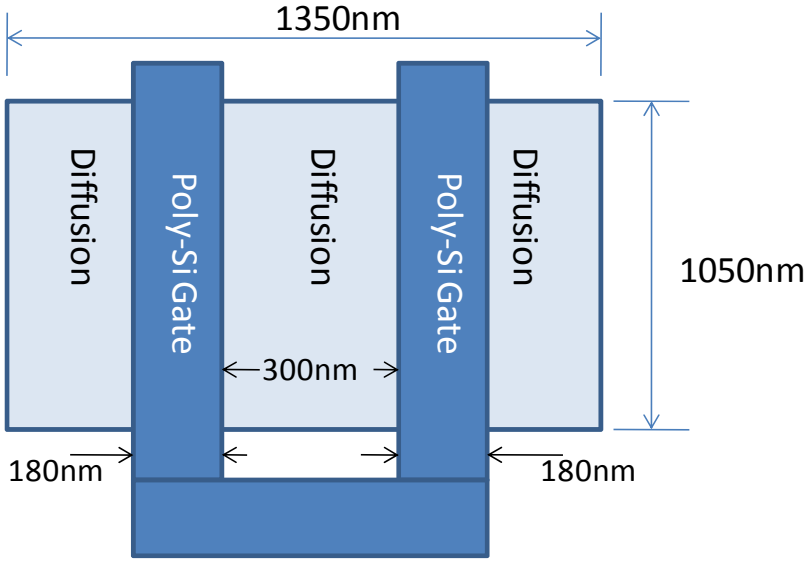
a) Diffusion capacitance




Where: $C_{bottom}$ = 23 ff/μ$^2$ and $C_{sidewall}$ = 10 ff/μ

DIFFUSION Capacitance= 10.86ff + 34.00ff = 44.86ff

b) Gate and Diffusion Capacitances



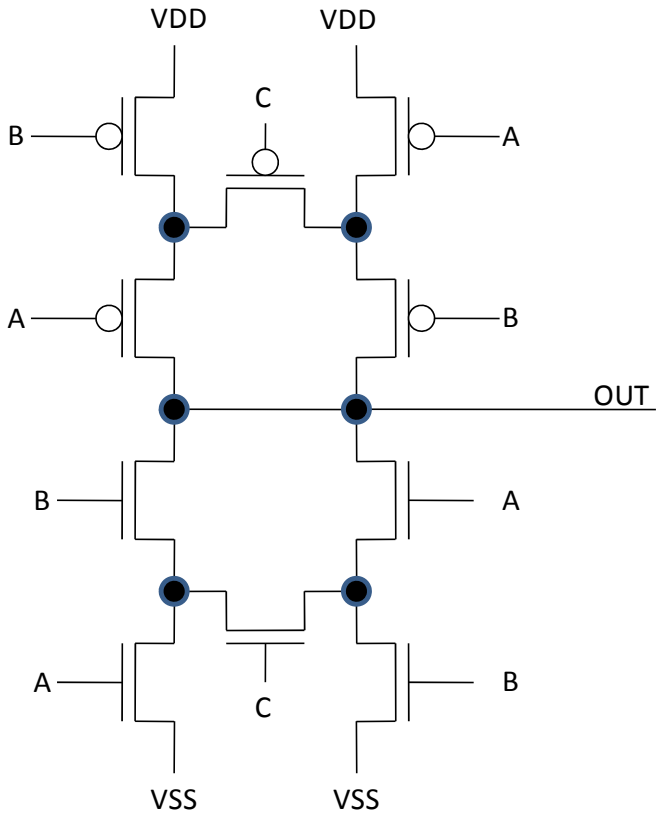

Where: $C_{bottom}$ = 29 ff/μ$^2$ $C_{sidewall}$ = 15.5 ff/μ $C_{gate}$ = 12.6 ff/μ$^2$

Total DIFFUSION Capacitance= 128.34ff (sidewall) + 30.14ff (bottom) = 158.49ff

Total GATE Capacitance= 2.3814ff + 2.3814ff = 4.7628ff

**Problem 2. Transistor Mapping & Sizing (20 Points)**

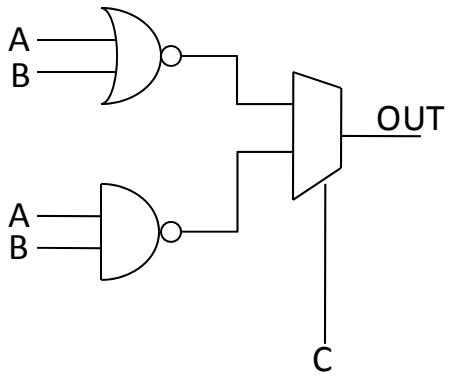
a) What is the truth table for the following circuit?




| A | B | C | OUT |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

b) Size the transistors so that they can drive a load which is 3X minimum size inverter. PMOS = 6 NMOS = 3 assuming a fanout of 3

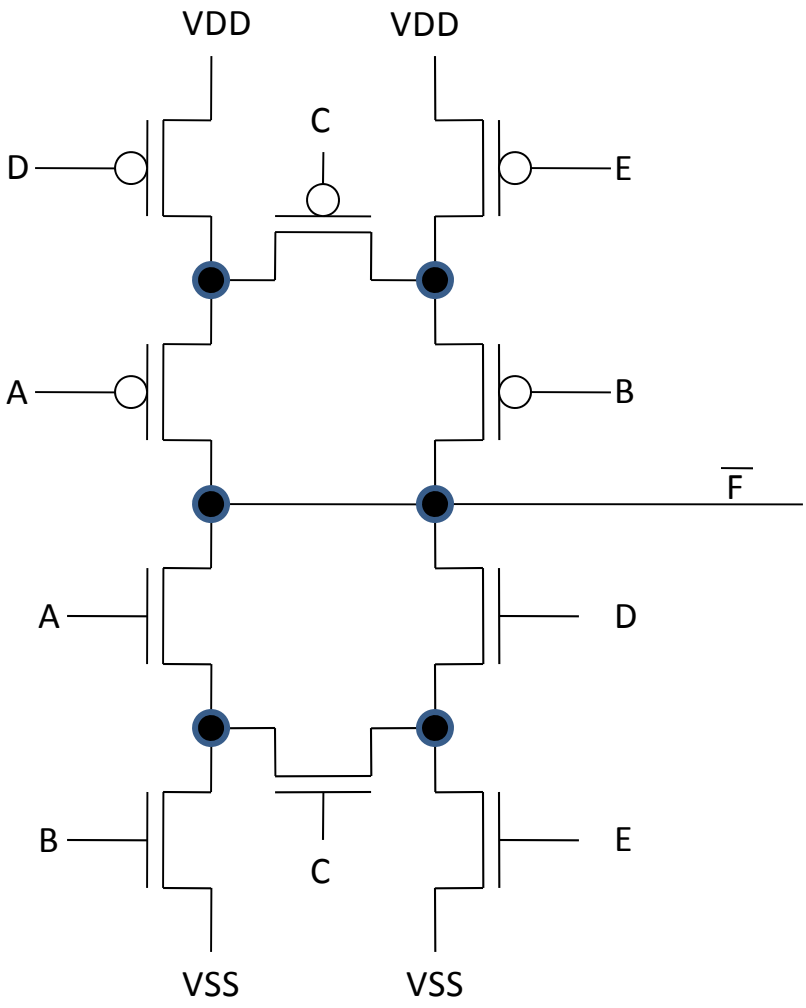
c) Draw the logic gate equivalent of this circuit



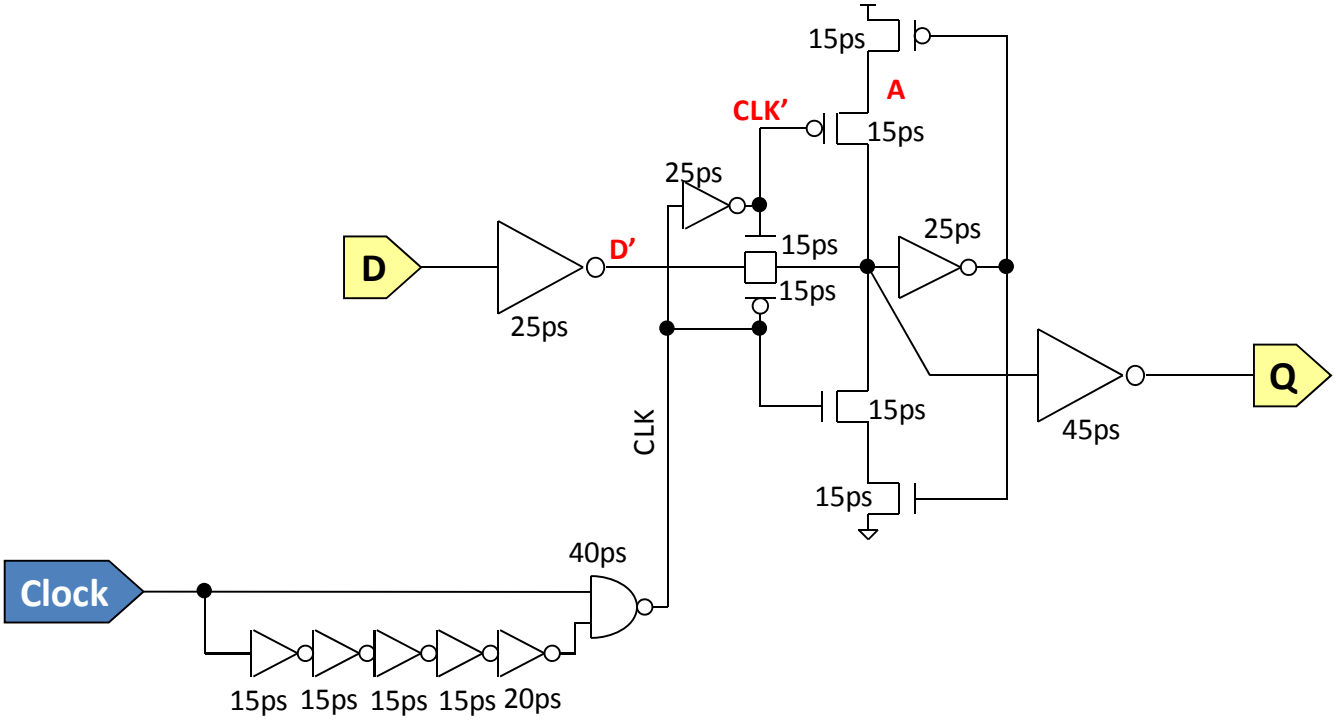
**Problem 3. Logic Mapping (20 Points)**

Implement the following expression in STATIC CMOS logic using **no more** than **10** total (PMOS or NMOS) transistors.

$$\overline{F} = (A.B) + (A.C.E) + (D.E) + (D.C.B)$$



**Problem 4: Sequential Elements (15 Points)**




**NOTE: Critical timing is from Clock to CLK' Time from Clock to CLK' is 145ps for CLK' going low and 65ps for CLK' going high.**

a) What is the $T_{setup}$ time

**25ps + 15ps + 25ps + 15ps – 145ps = -65ps**

NOTE: negative setup time is typical of a pulse latch

b) What is the $T_{hold}$ time?

**145ps -25ps = 120ps**

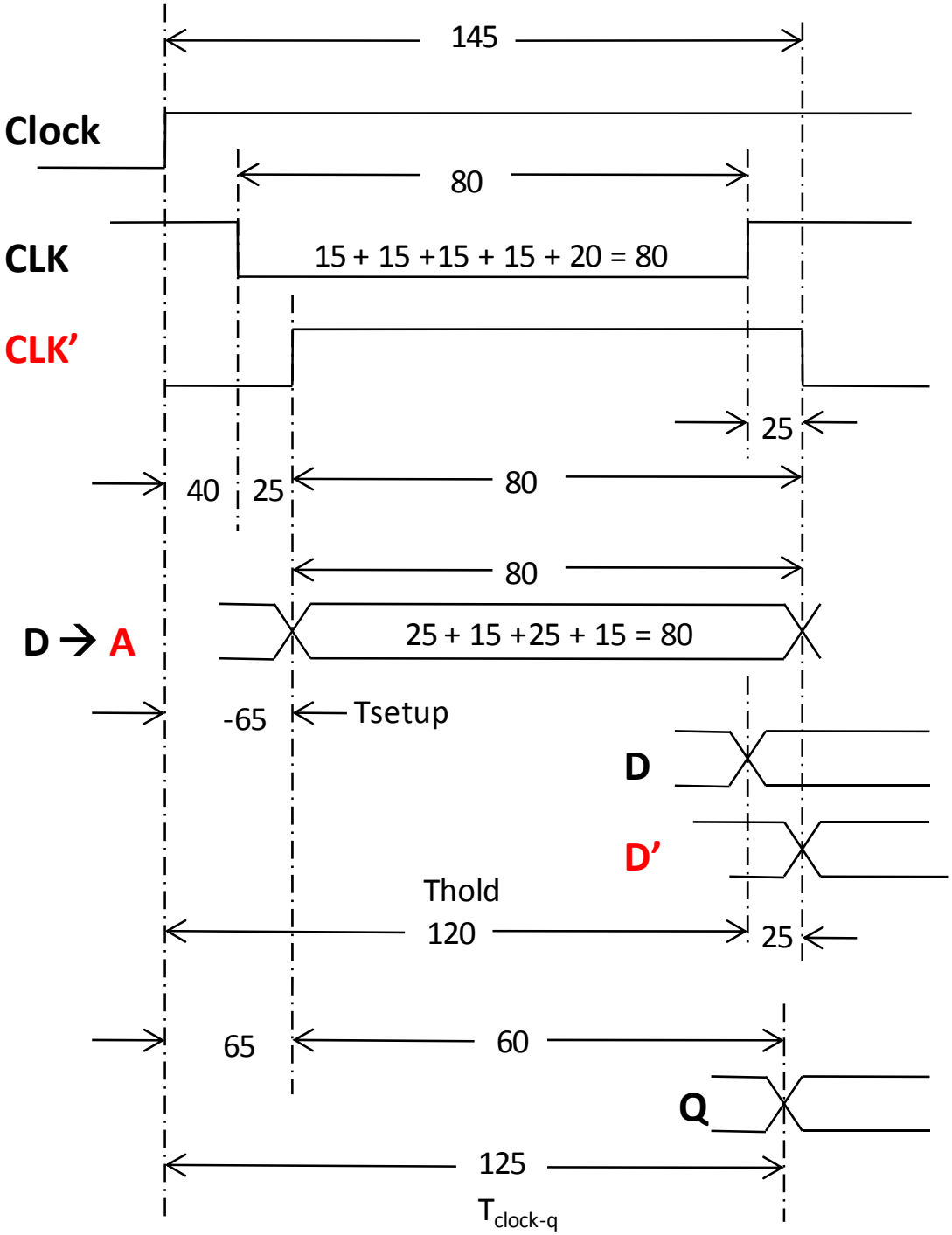
NOTE: Excessive hold times are typical of a pulse latch

c) What is the $T_{clock-q}$ time?

**65ps + 15ps + 45ps = 125ps**

d) What is the pulse width of the CLK signal?

**15ps + 15ps + 15ps + 15ps + 20ps = 80ps**




NOT TO SCALE (obviously ;-)

**Problem 5. Logical Effort (15 Points)**

Design a 10-input AND gate network for minimum delay using nothing more than the following standard cell gates:

| Gate type | 1x | 2x | 3x |
|---|---|---|---|
| INV | ✓ | ✓ | ✓ |
| 2-NAND | ✓ | ✓ | ✓ |
| 3-NAND | ✓ | ✓ | n/a |
| 2-NOR | ✓ | ✓ | n/a |
| 3-NOR | ✓ | ✓ | n/a |

NOTE: n/a indicates not available

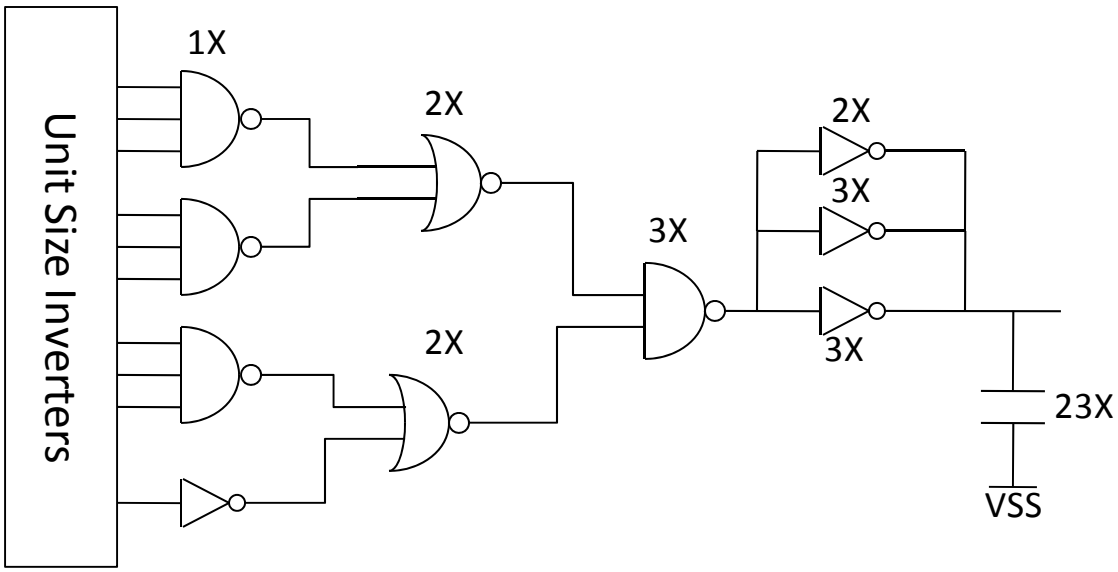
The network is driven by unit size inverters and the output is driving a load of 23 unit size inverters. Compute the delay using logical effort technique.

H = 23
B = 1 (No Branching)
Assume 5 stages (including unit size inverter)
INV -> NAND-3 -> NOR2 –> NAND2 -> INV

G=1 * 5/3 * 5/3 * 4/3 * 1 = 100/27

F = GBH = 23 * 1 * 100/27 = 106.48
f = $F^{1/5}$ = 2.54 Lets use 3.00 to size gates
D = (5 * 2.54) + 1 + 3 + 2 + 2 + 1 = 21.71 (if we use a fanout of 2.54)

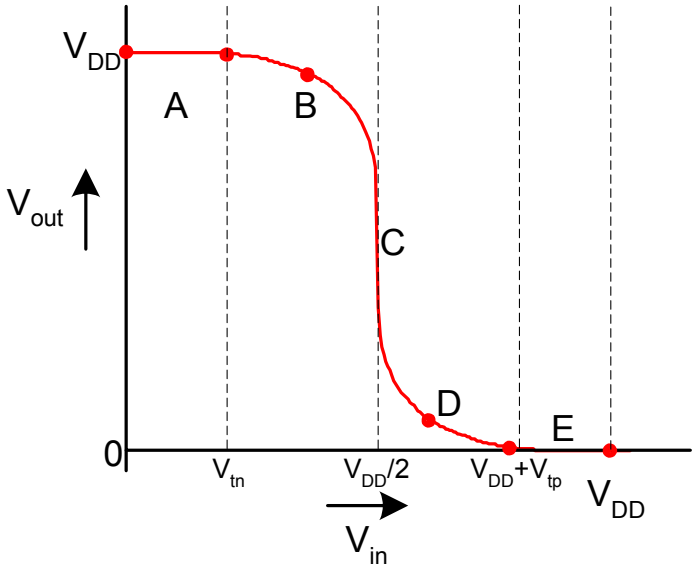
INV = 69/3 ≈ 24 -> 16/8 which is 8X device
NAND2 = 24/3 * 4/3 ≈ 12 which is a 3X device
NOR2 = 12/3 *5/3 ≈ 8 which is a 2X device
NAND3 = 8/3 * 5/3 ≈ 4 which is a 1X device



**Problem 6. Device Operation (20 Points)**

Derive the analytic expression for Vout as a function of Vin for regions B and D for the inverter transfer function shown to the right. Assume that | Vtp | = Vtn and βn = βp

| Region | nMOS | pMOS |
|---|---|---|
| A | Cutoff | Linear |
| B | Saturation | Linear |
| C | Saturation | Saturation |
| D | Linear | Saturation |
| E | Linear | Cutoff |




REGION B:

In region B, the NMOS is saturated and PMOS is linear:

$$\frac{\beta}{2}\left(V_{\text{in}}-V_t\right)^2=\beta\left(\left(V_{\text{in}}-V_{DD}\right)-\frac{\left(V_{\text{out}}-V_{DD}\right)}{2}+V_t\right)\left(V_{\text{out}}-V_{DD}\right)$$

$$V_{\text{out}}=\left(V_{\text{in}}+V_t\right)+\sqrt{\left(V_{\text{in}}+V_t\right)^2-\left(V_{\text{in}}-V_t\right)^2+V_{DD}\left(V_{DD}-2V_{\text{in}}-2V_t\right)}$$

REGION D:

In region D, the nMOS is linear and the pMOS is saturated:

$$\frac{\beta}{2}\left(V_{\text{in}}-V_{DD}+V_t\right)^2=\beta\left(V_{\text{in}}-V_t-\frac{V_{\text{out}}}{2}\right)\left(V_{\text{out}}\right)$$

$$V_{\text{out}}=\left(V_{\text{in}}-V_t\right)-\sqrt{\left(V_{\text{in}}-V_t\right)^2-\left(V_{DD}-V_{\text{in}}-V_t\right)^2}$$