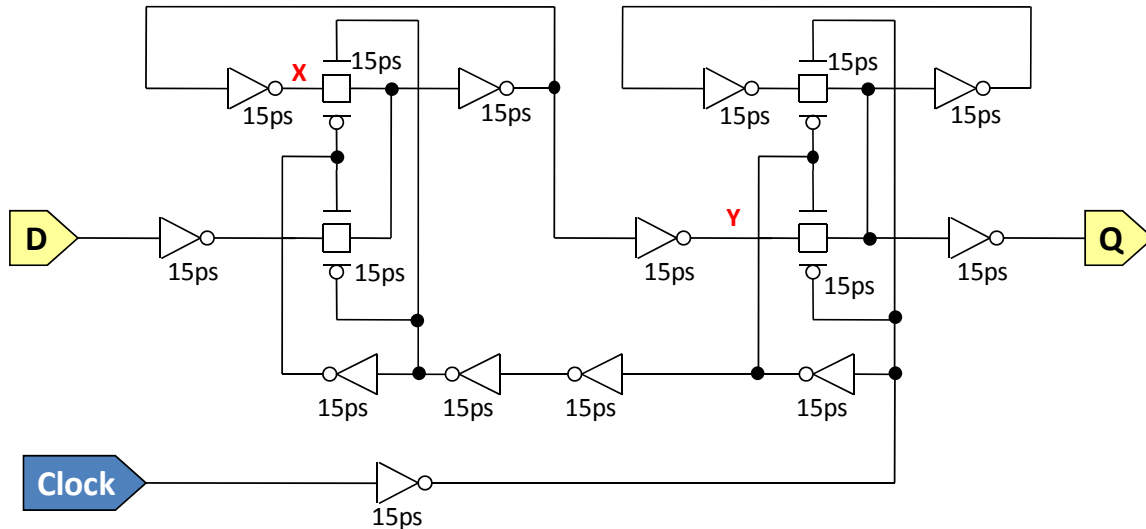


Problem 1 Flip-Flop Timing (25 Points)

The logic gates of the flip-flop below all have a delay of 15ps.



a) What is the SETUP time?

$$(15\text{ps} + 15\text{ps} + 15\text{ps} + 15\text{ps}) - (15\text{ps} + 15\text{ps}) = 30\text{ ps}$$

Input path from D to NMOS Clock Inverters to Slave stage

NOTE: The two inverter delay between the clocks to Master and Slave stages requires that the data is set up to the slave stage (node Y) earlier than to node X in the master stage so that there is not a Clock->Q push-out.

b) What is the CLOCK - Q Delay

$$15\text{ps} + 15\text{ps} + 15\text{ps} + 15\text{ps} = 60\text{ ps}$$

inv inv pass inv

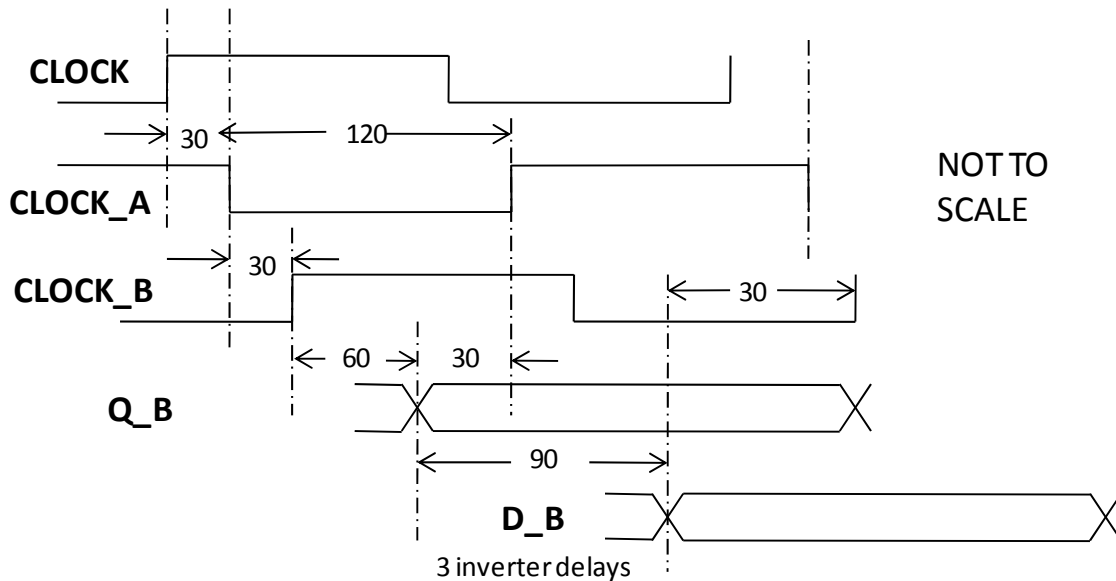
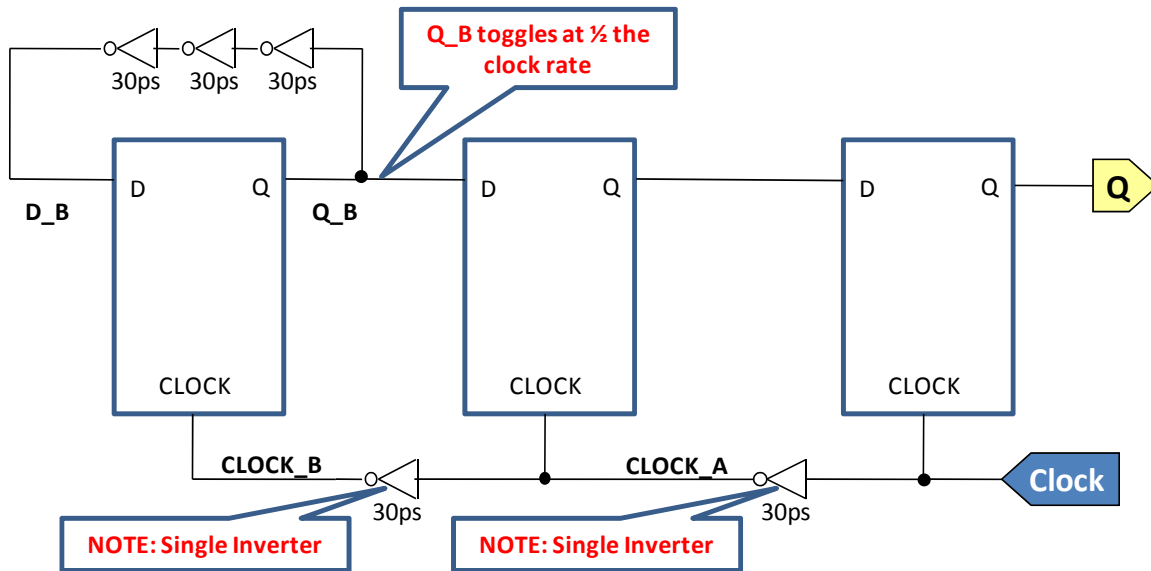
If you use Ops for the setup time, the Clock-Q delay will be 90ps.

c) What is the HOLD time?

$$(15\text{ps} + 15\text{ps} + 15\text{ps} + 15\text{ps} + 15\text{ps}) - (15\text{ps}) = 60\text{ ps}$$

Clock inverters inv
on D input

Problem 2. Maximum Clock Frequency (25 Points)



a) What the fastest clock rate that this circuit can be operated at?

The fastest clock rate is determined by 1 of 2 paths:

1. The setup and hold time of the first flip-flop: $CLOCK_B \rightarrow Q_B \rightarrow D_B = 180ps$
2. The setup and hold time of Q_B to the second flip-flop = $120ps$

The second path is a half cycle path. Assuming that the clock is a 50% duty cycle the minimum clock period is $120ps + 120ps = 240ps$

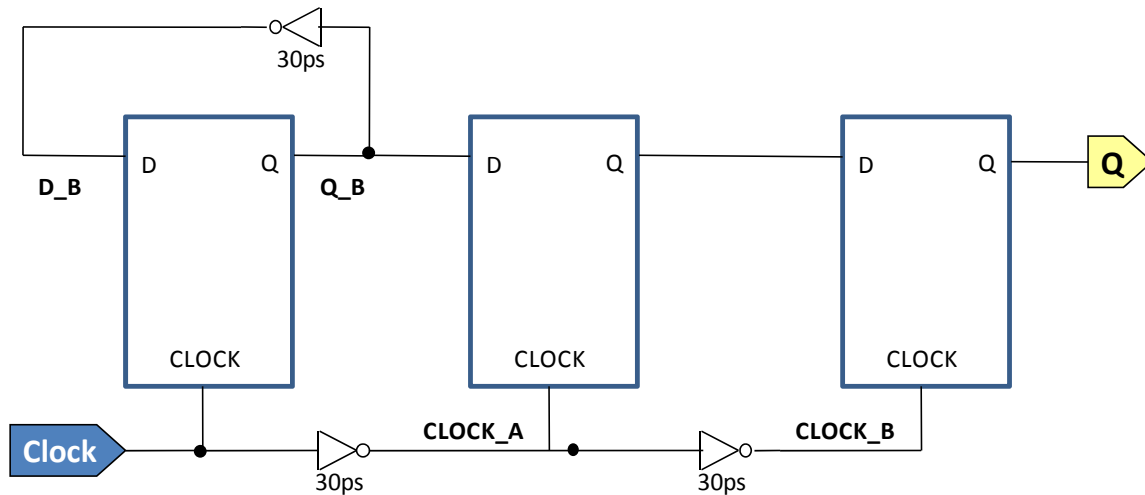
The maximum clock frequency is: $1/240ps = 4.167 GHz$

b) What is the frequency of the output Q when running at the fastest CLOCK rate?

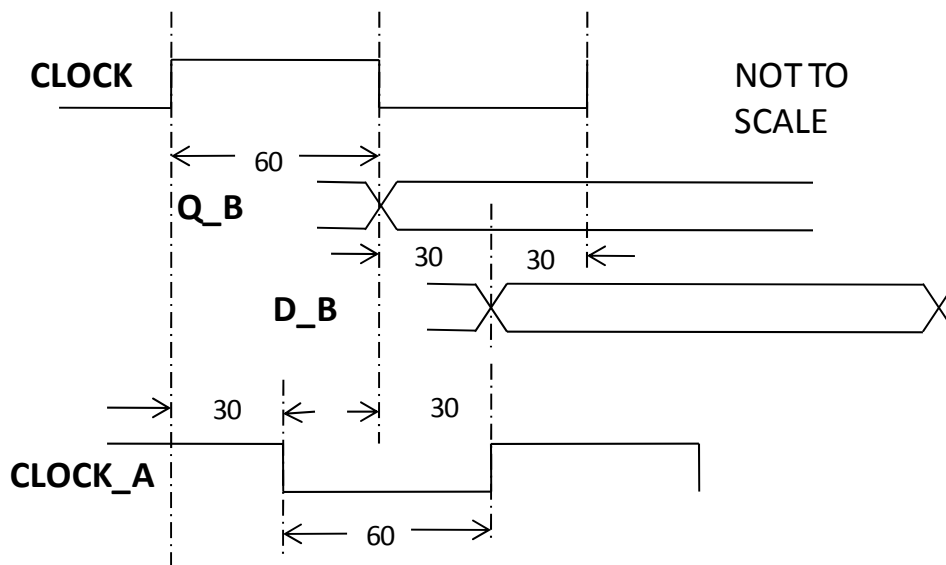
Because the first flip-flop is a divide-by-2 circuit, the frequency of output Q is $4.167\text{GHz}/2 = 2.083\text{ GHz}$

c) How would you speed up this circuit?

Restructure the clocks and remove 2 inverters (can't remove 3 inverters or the circuit quits working)



d) What is the fastest frequency this circuit could operate at given the changes made in part (c).

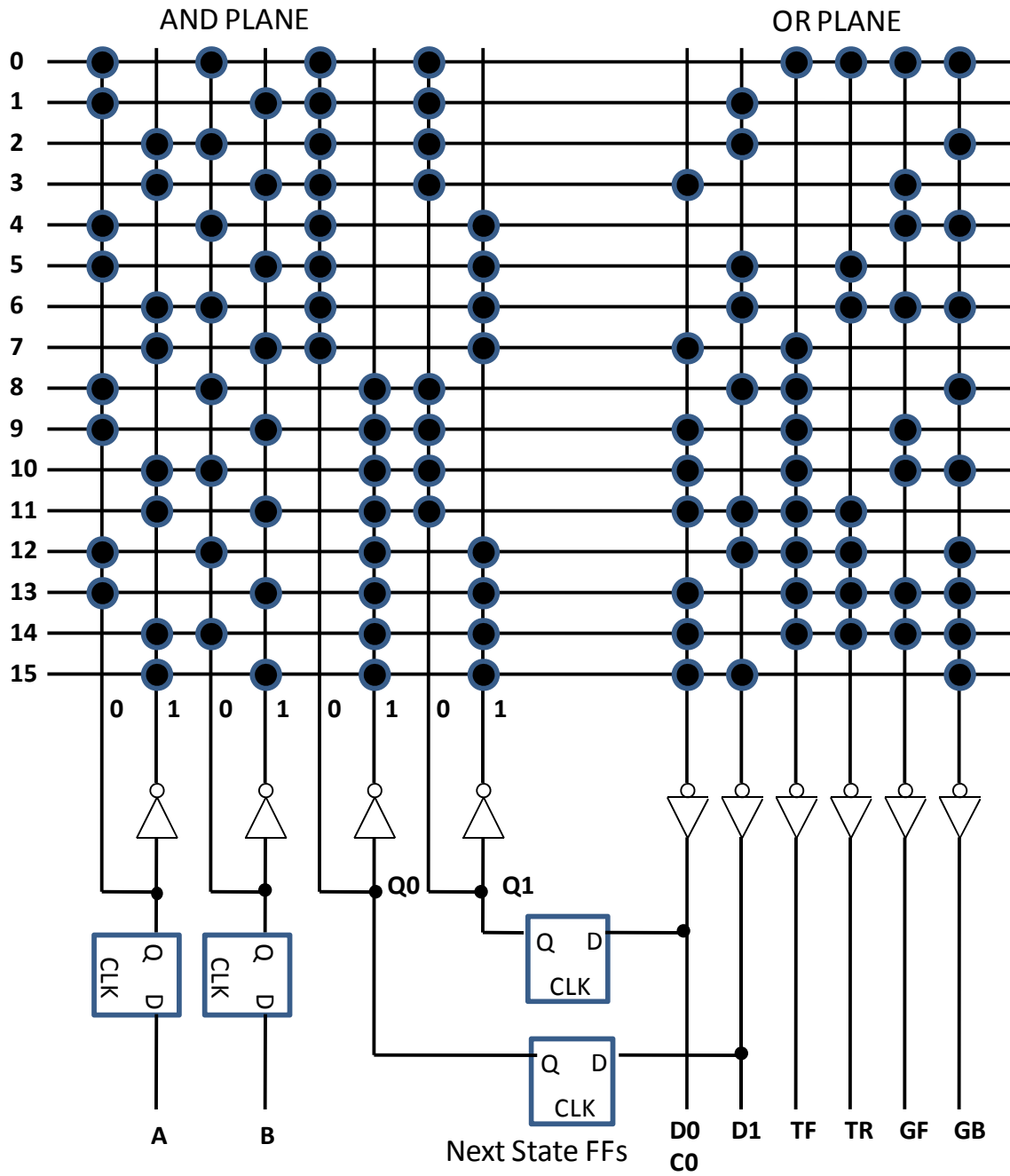


The fastest clock rate is determined by 1 of 2 paths:

1. The setup and hold time of the first flip-flop: $Q_B \rightarrow D_B = 90\text{ps}$
2. The setup and hold time of Q_B to the second flip-flop = 60ps

The second path is a half cycle path. Assuming that the clock is a 50% duty cycle the minimum clock period is $60\text{ps} + 60\text{ps} = 120\text{ps}$

The maximum clock frequency is: $1/120\text{ps} = 8.33\text{ GHz}$



Problem 4. Domino Logic (25 Points)

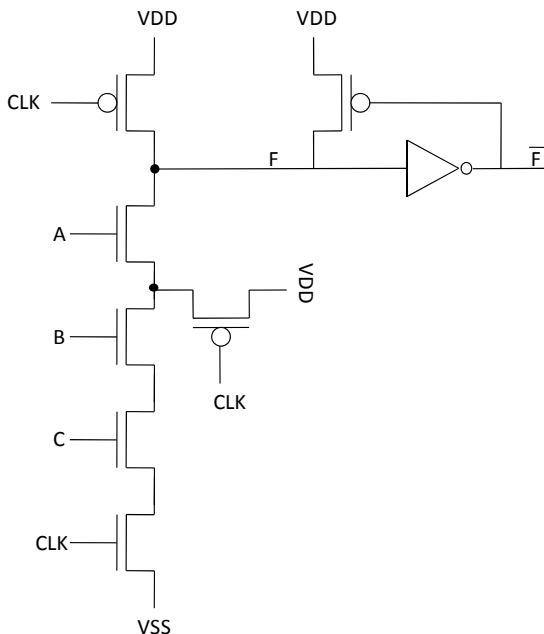
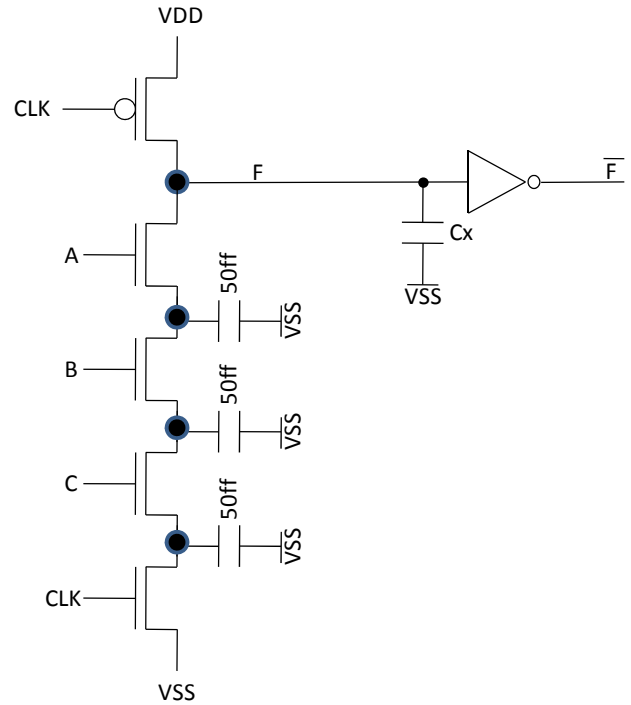
The inputs to a domino are always LOW during the precharge phase (CLK=LOW) and can transition from a LOW->HIGH during the evaluation phase (CLK=HIGH). Consider the 3-input domino logic gate shown to the right. If during the evaluation phase signals A and B transition from a LOW->HIGH charge sharing will cause node F to droop.

- a) Given that the VDD=1.8V and that the switch point of the inverter is 1.15V, calculate what the size of capacitor Cx has to be to prevent the output of the inverter from switching.

$$\frac{C_x * 1.8}{C_x + 100} = 1.15$$

$$C_x = \frac{115}{1.8 - 1.15} = 176.92ff$$

- b) By annotating the transistor schematic shown to the right, explain two techniques used in CMOS circuits for solving charge sharing problems. What drawbacks may be associated with those two circuit techniques (if any)?



Bonus Problem: POWER Analysis (25 Points)

An embedded hardware accelerator in a system-on-chip is designed in a 65nm process, and has 1 million logic transistors with an average width of 385nm. The gate capacitance, $C_g = 2.2\text{fF}/\mu\text{m}$. The gates have an switching factor of .2 (20%) and $V_{DD} = 0.9\text{V}$

- (a) What is the maximum clock frequency if the dynamic power should not exceed 20 mW?

$$Power = \frac{1}{2} (C * V^2 * Frequency * Switching_{Factor})$$

$$Capacitance = 1e6 * .385u * 2.2e-15/u = .847e-9$$

$$20mw = \frac{1}{2} (.847nf * .9^2 * .2 * Frequency)$$

$$Frequency = \frac{40mw}{.847nf * .9^2 * .2} = 291.51 \text{ MHz}$$

- (b) If the subthreshold leakage is $20\text{nA}/\mu\text{m}$ and the gate leakage is $2\text{nA}/\mu\text{m}$, and **if half the transistors are off** (on average), what is the leakage power?



$$Leakage = .5e6 * .385u * 22nA/u * .9V = 3.8115 \text{ mw}$$