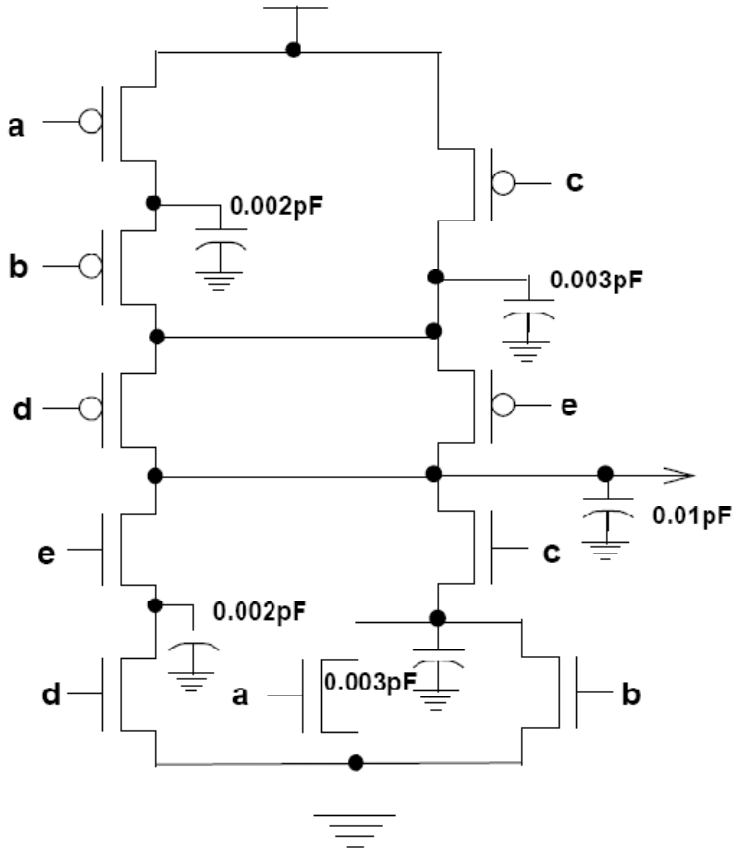
Previous EE360R Final Exam Questions

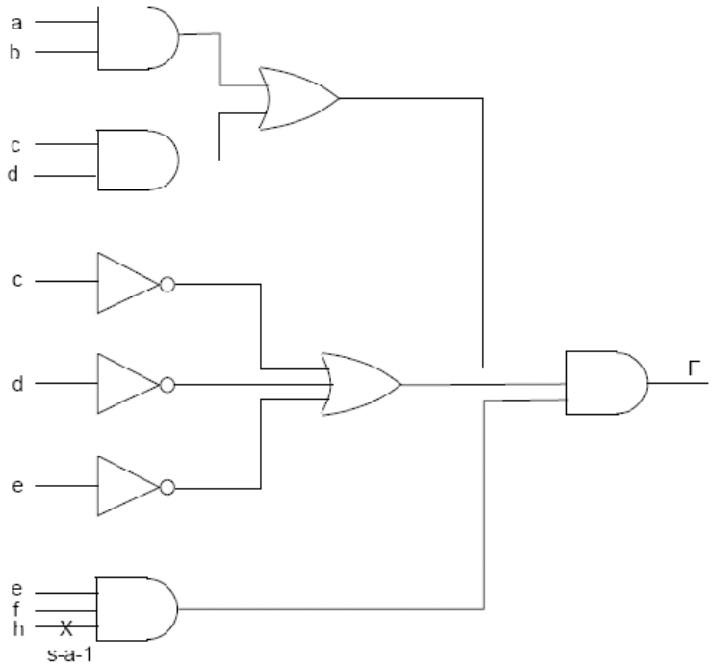
In the static CMOS circuit below, the on-resistance of each n-channel transistor is 5 KOhms and that of a p-channel transistor is 10 KOhms. The gate capacitance of an n-channel transistor is 0.02pF and p-channel transistor is 0.03pF. The source/drain capacitance of an n-channel transistor is 0.001pF and for a p-channel transistor is 0.002pF. The routing capacitances for interconnections are lumped at the nodes as shown.



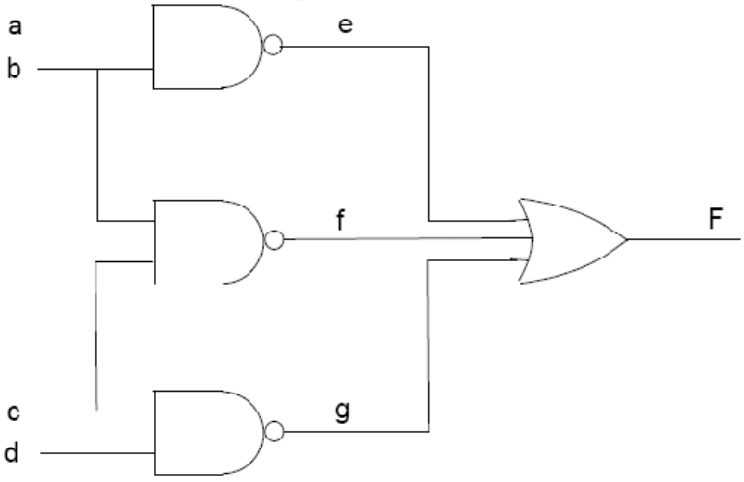
(a) Find the delay when (a b c d e) makes the following transitions:
0 0 0 0 0 ⇒ 0 0 0 1 1 ⇒ 0 0 0 0 1.

Previous EE360R Final Exam Questions

(a) Find a test for the line h stuck-at-1 in the figure below.



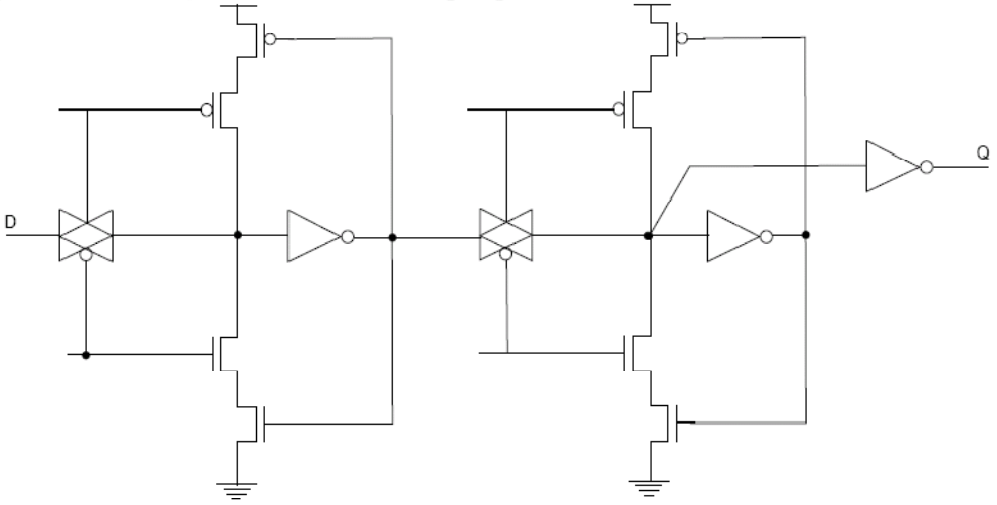
(b) Perform test generation for the following faults and explain the results.



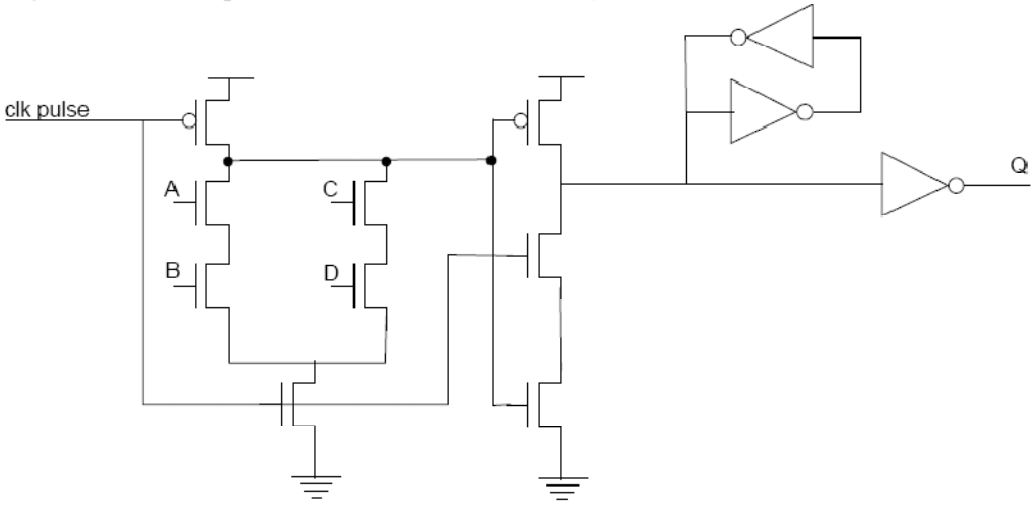
(i) g s-a-0
(ii) e s-a-1
(iii) f s-a-0

Previous EE360R Final Exam Questions

(a) Label the four inputs in the circuit below with the clock symbols CLK and CLKB (complement of CLK) so that the flop latches at the falling edge of the clock.



(b) Analyze the following circuit and write down the equation for its function.



Previous EE360R Final Exam Questions

a) Draw the schematic for a static CMOS network for the following function using the minimum number of transistor. Do NOT assume that the inverted inputs are available.

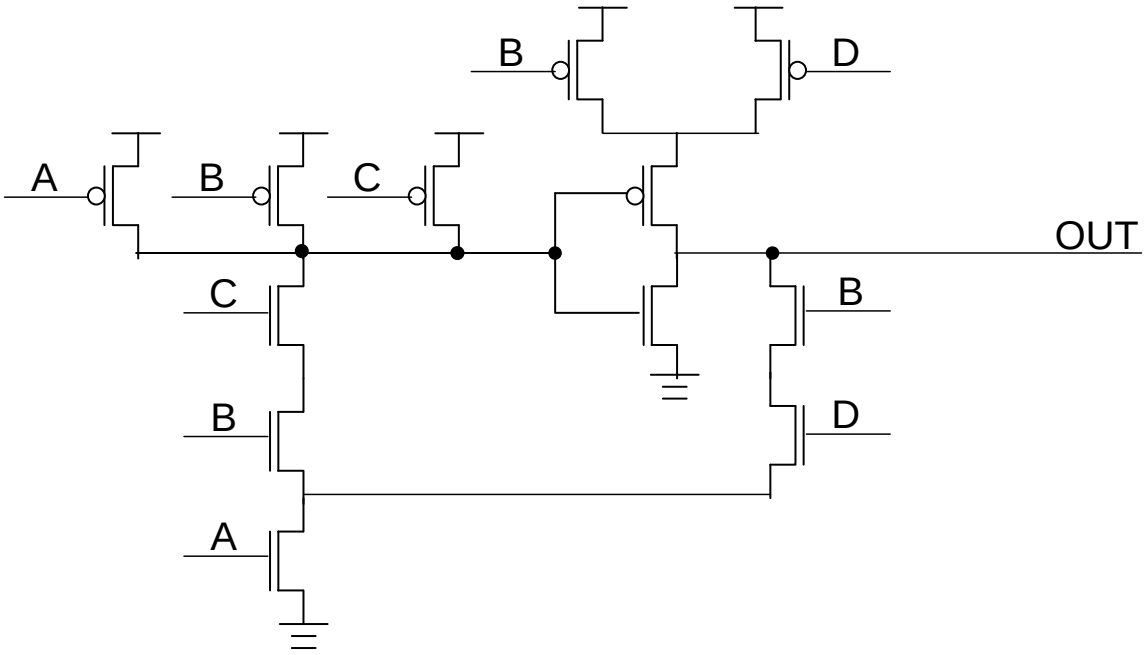
Y = A'B'C' + ABC' + A'B'C + ABC

b) Draw a Domino CMOS schematic (with PMOS precharge and feedback hold device) of the following functions F1 and F2 using the minimal number of transistors.

F1 = (M·N + W) · P · (Q·R + S·T)

F2 = T·S + R·Q

Previous EE360R Final Exam Questions

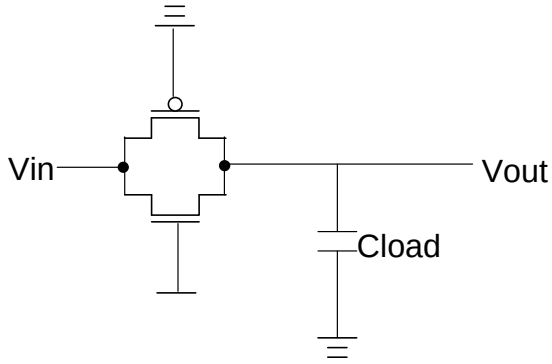


a) Write down the function OUT implemented by the circuit below:
Minimize the number of transistors and draw the new schematic. Do NOT assume that the complementary inputs are available.

Previous EE360R Final Exam Questions

Describe the regions of operation for the NMOS and PMOS device in the transmission gate shown below in terms of linear, saturation and cutoff as the capacitor is charged or discharged:

Vtn = 1.0V Vtp=1.0V



a) Initial conditions: Vin = 5.0V Vout = 0.0V

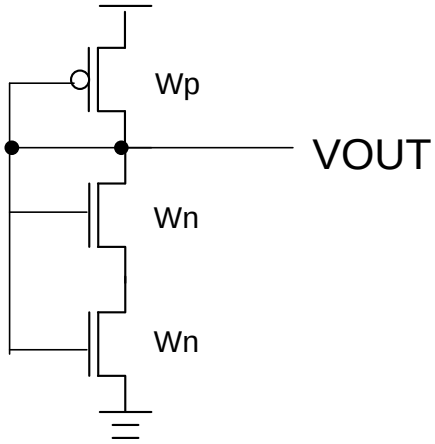
Condition	PMOS Region	NMOS Region
Vin = 5.0V Vout = 0.0V		
Vin = 5.0V Vout = 2.5V		
Vin = 5.0V Vout = 5.0V		

b) Initial conditions: Vin = 0.0V Vout = 5.0V

Condition	PMOS Region	NMOS Region
Vin = 0.0V Vout = 5.0V		
Vin = 0.0V Vout = 2.5V		
Vin = 0.0V Vout = 0.0V		

Previous EE360R Final Exam Questions

a) Determine the voltage on node VOUT.



Assume: $\mu_n = 2 \cdot \mu_p$ Ln = Lp Vtn = Vtp

Both transistors are operating in the saturation region.

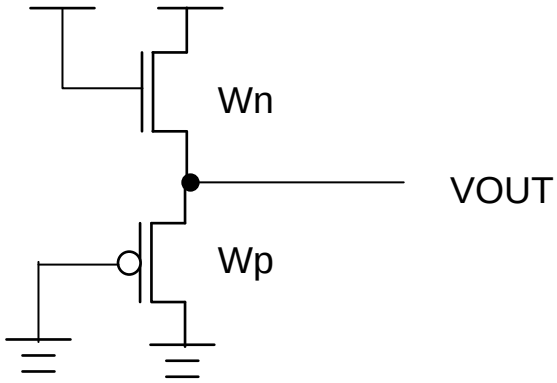
Express value on VOUT as a function of Wn, Wp and VDD

b) Determine the voltage on node VOUT.

Assume $\mu_n = 2 \cdot \mu_p$ Ln = Lp Vtn = 1.0V Vtp = 1.0V

Both transistors are operating in the saturation region.

Express value on VOUT as a function of Wn, Wp and VDD



Previous EE360R Final Exam Questions

a) Explain how the parasitic (field) transistor is formed between two n-channel transistors. How would you reduce the effects of these parasitic transistors?

b) How does a "dummy collector" prevent latch up?

a) Explain how the shape of the input waveform to a CMOS inverter alters the delay through the gate.

b) Explain how you would estimate and plan the clock distribution scheme in a chip. Summarize the parameters that are relevant and explain how your scheme deals with these.

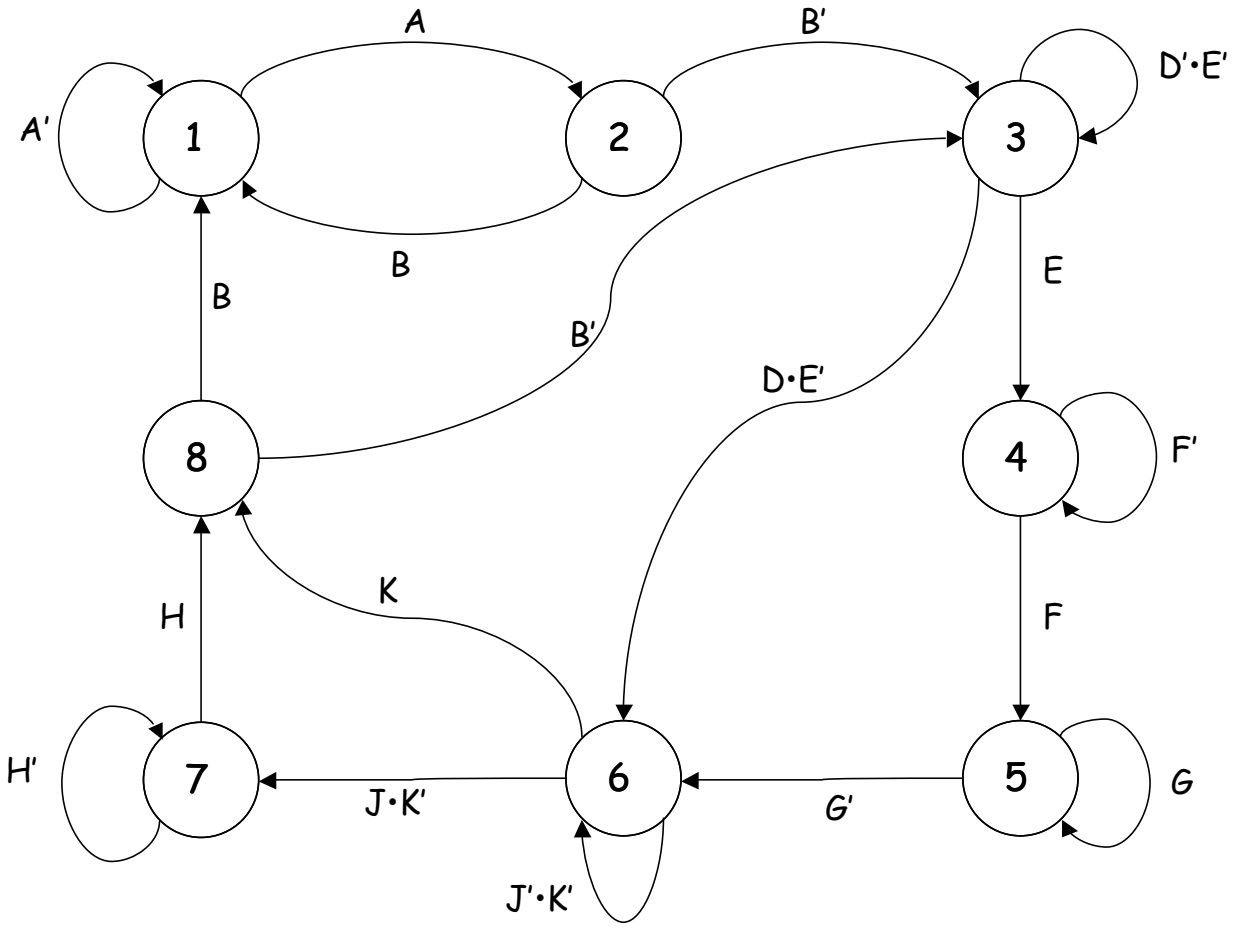
a) What limits the VDD supply voltage in a CMOS technology (i.e., how low or high can you set it)? Explain what you expect the effects of these two voltage extremes to be on the internal circuits. Suggest situations where both of these voltage extremes might be of use.

b) Suggest the approaches you would take to reduce the power dissipation of a CMOS chip.

Previous EE360R Final Exam Questions

a) Complete the following state diagram for arcs: 8->3 6->7 3->6

Confirm that all other arcs are correct. If not, correct the equation(s).



b) How many memory elements (Flip-Flops) are required to implement the state machine for:

One-Hot Encoding:

Fully Encoded:

c) How many inputs are required for the state machine including state inputs for:

One-Hot Encoding:

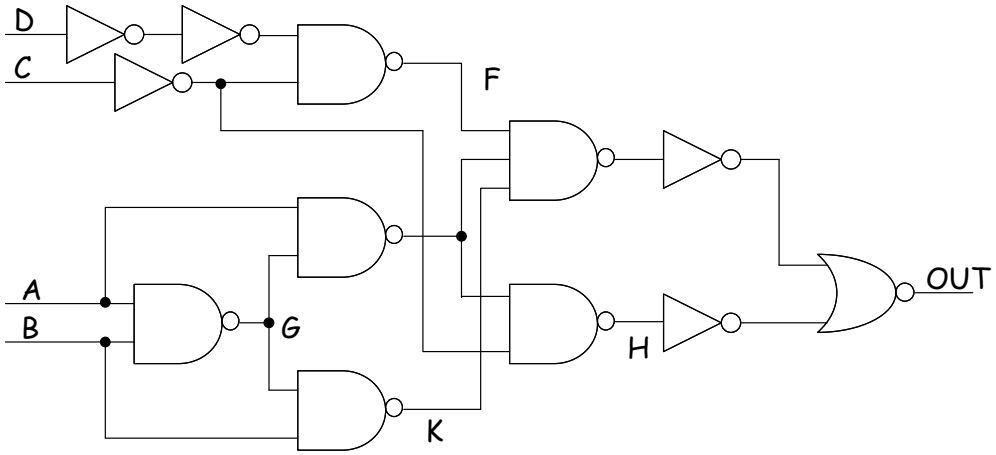
Fully Encoded:

Previous EE360R Final Exam Questions

d) Fill out the following State Table for the state machine described above:

Current State	*A*	B	D	E	F	G	H	J	K		*Next* State
1	0										1
1	1										2
2		1									1
2		0									3
3			0	0							3
3				1							4
3			1	0							6
4					0						4
4					1						5
5						1					5
5						0					6
6								0	0		6
6								1	0		7
6									1		8
7							0				7
7							1				8
8		0									3
8		1									1

Previous EE360R Final Exam Questions



a) Find vector(s) that allow the detection of a SA-1 and SA-0 fault on node F.

SA-1: Cannot detect.

SA-0: ABCD { 001X, 111X } D is a don't care

b) Find vector(s) that allow the detection of a SA-1 and SA-0 fault on node G.

SA-1: ABCD {11XX } C & D are don't care

SA-0: ABCD { 1000, 101X, 011X }

c) Find vector(s) that allow the detection of a SA-1 and SA-0 fault on node H.

SA-1: ABCD { 0101, 0100, 0001, 1101 }

SA-0: ABCD { 011X, 10XX }

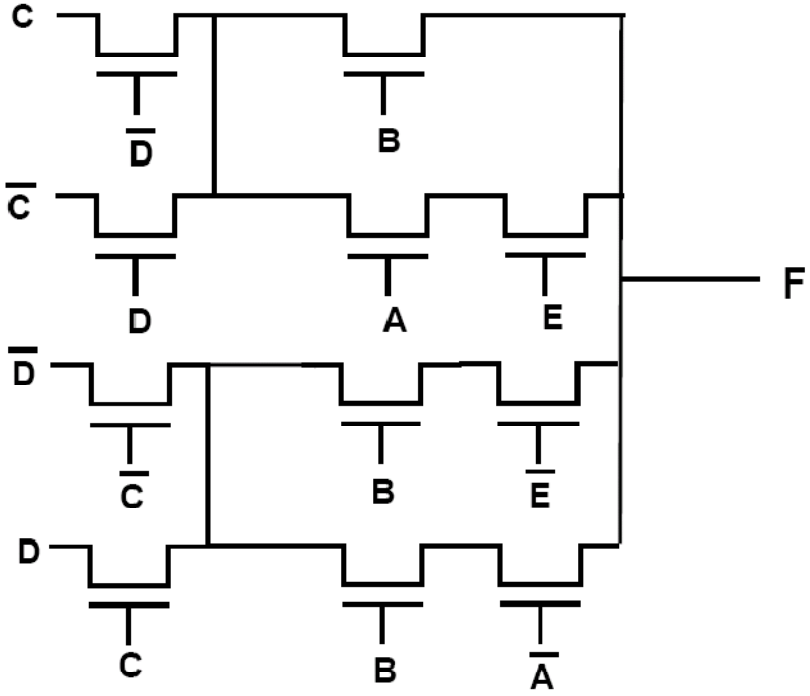
d) Find vector(s) that allow the detection of a SA-1 and SA-0 fault on node K.

SA-1: ABCD {011X }

SA-0: ABCD { 001X, 111X }

Previous EE360R Final Exam Questions

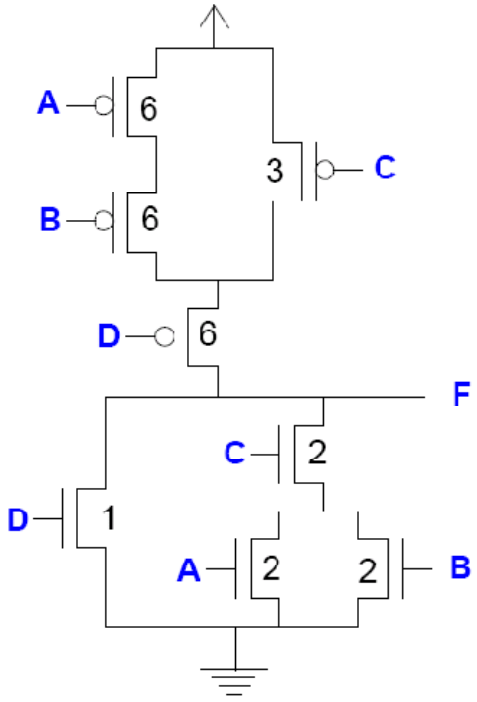
Write down the logic function implemented by the circuit below; use parantheses in the expression to reduce the number of literals.



F =

Previous EE360R Final Exam Questions

Find the largest as well as contimination delays for both 0-1 and 1-0 transitions for the circuit below. The widths of the transistors are given. Assume that a minimum width transistor will have an on-resistance of **R** and a gate capacitance of **C**; the source and drain capacitances are also C, and there is **no** sharing of diffusions. Give the input combinations which produce the respective delays (assuming that the internal nodes are charged or discharged as appropriate).



Input (ABCD) producing the largest rise delay:

Largest rise delay =

Input (ABCD) producing the largest fall delay:

Largest fall delay =

Input (ABCD) producing the smallest rise delay:

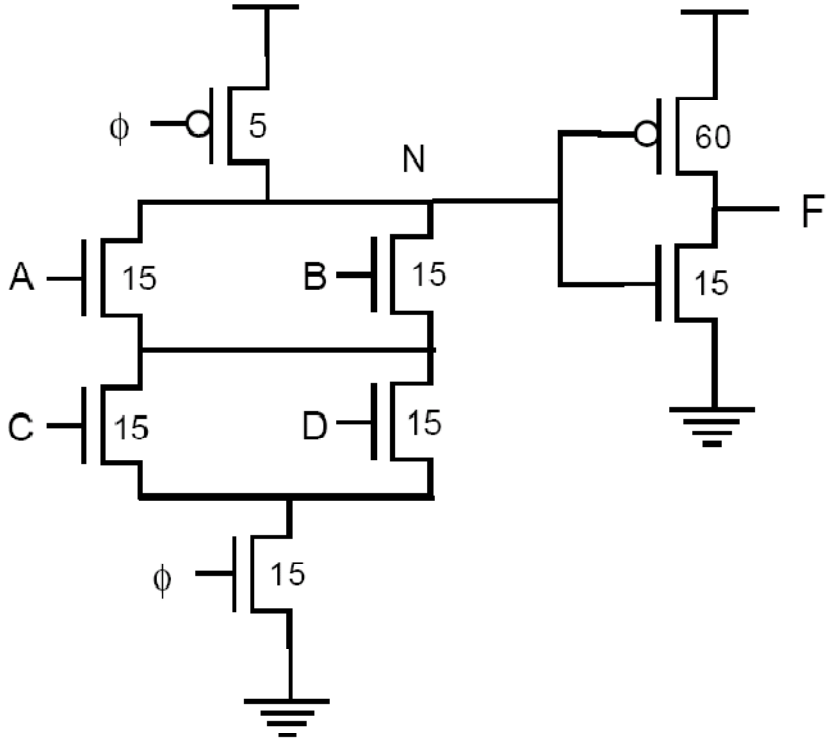
Contamination rise delay =

Input (ABCD) producing the smallest fall delay:

Contamination fall delay =

Previous EE360R Final Exam Questions

The domino circuit has the widths of the transistors shown next to them. Assume that a minimum width transistor has a gate capacitance of C, with the source and drain capacitances also each equal to C. Assume no sharing of diffusion.



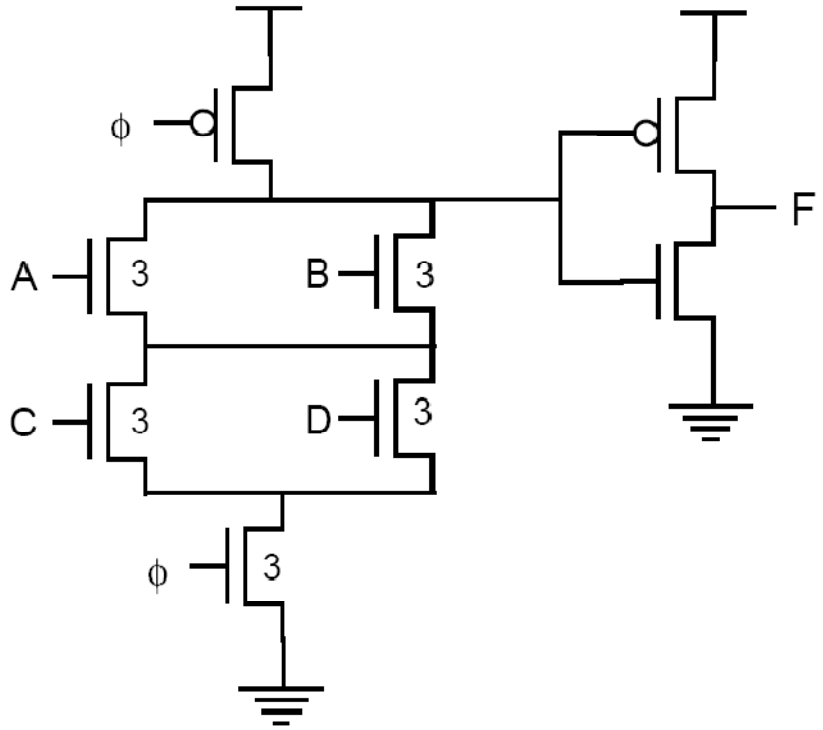
(a) Under the worst-case input sequence, what is the largest voltage drop on the dynamic node, N?

(b) Give a sequence of inputs (ABCD) which will cause the voltage drop on N.

(c) How should the static inverter be sized to cause a voltage drop (noise) of at most 20% on the node N?

Previous EE360R Final Exam Questions

The best stage effort for a domino circuit has been found to be between 2.0 and 2.76 (for unfooted and footed blocks). The circuit below has the transistor widths labeled for the dynamic portion. The static inverter is a standard Hi-Skew with a logical effort of 5/6.



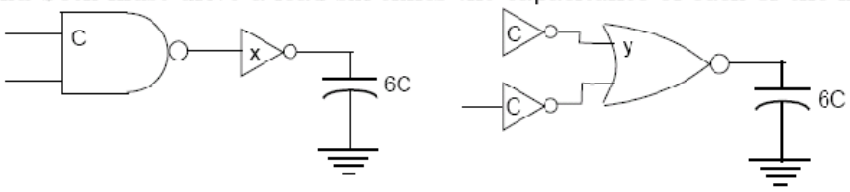
(a) If the stage effort is 2.5, what would be the corresponding path electrical effort, H (using the standard logical effort formulation)?

(b) What would be the delay of the circuit for the design in (a)?

(c) What would be the sizes of the P and N transistors in the static inverter (for the same design)?

Previous EE360R Final Exam Questions

Consider the two different implementations of an AND gate below. Both have an input capacitance of C and both must drive a load six times the capacitance of each of the inputs.



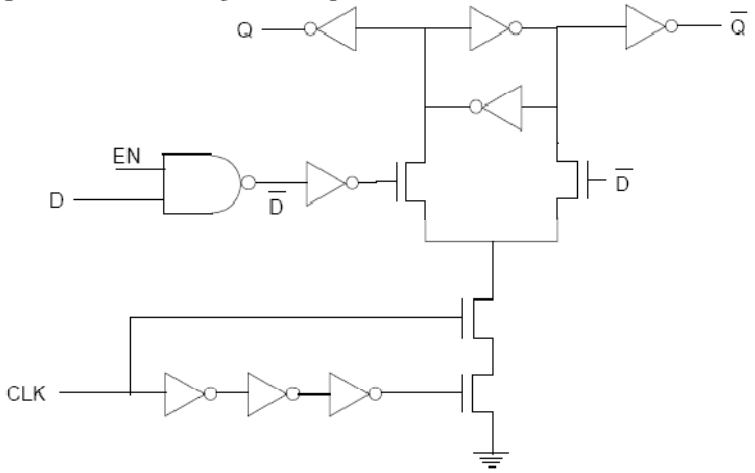
(a) What is the path effort of each design?

(b) Which design will be the fastest? Explain.

(c) Compute the sizes of the logic gates, x and y to achieve the least delay.

Previous EE360R Final Exam Questions

The inverters in the flip-flop below have rise and fall delays of 50 pS. The NAND gate has a rise delay of 100 pS and a fall delay of 150 pS.



Neglecting the delay of the nMOS transistors, what are the parameters of the flip-flop?

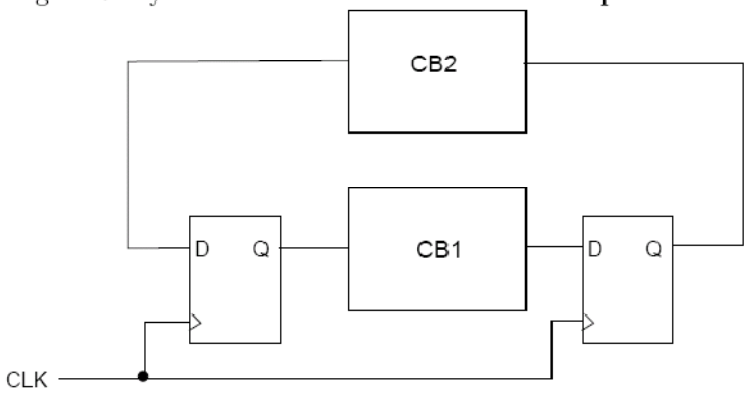
(a) Setup time

(b) Hold time

(c) CLK-Q delay

Previous EE360R Final Exam Questions

The sequential circuit below has two flops and two combinational blocks, CB1 and CB2. The design is made using a library which includes inverters with a 25 pS rise and fall delay.



The parameters of the flops are: $t_{pcq} = 100pS, \quad t_{ccq} = 20pS, \quad t_{setup} = 50pS, \quad t_{hold} = 100ps$

The parameters of the combinational block are as follows.
CB1: $t_{pd} = 250pS, t_{cd} = 100pS$
CB2: $t_{pd} = 350pS, t_{cd} = 50pS$

(a) Will the circuit work correctly? Explain and, if not, suggest a fix which will not affect the maximum frequency at which the circuit can be operated.

(b) If the circuit can be operated correctly, what is the maximum frequency at which it will work correctly?

(c) Suggest a modification to the clock circuitry to increase the frequency found in (b). Explain.

Previous EE360R Final Exam Questions

An embedded hardware accelerator in a system-on-chip is designed in a 1 V, 90 nm process, and has 1 million logic transistors with an average width of 12λ. The gate capacitance, $C_g = 2fF/\mu m$. The gates have an activity factor of 0.2.

(a) What is the maximum clock frequency if the dynamic power should not exceed 20 mW?

(b) If the subthreshold leakage is $20nA/\mu m$ and the gate leakage is $2nA/\mu m$, and if half the transistors are off (on average), what is the leakage power?