	VLSI Design	J. Abraham
Spring 2006	**EXAM. I**	**March 1, 2006**

Name: **Student, A**

Open Book, Open Notes. Time Limit: **75 minutes** (pace yourself). Check for **5 pages in exam.**

Write all your answers in the spaces/boxes provided.

Show any calculations in these pages using the back of the pages if needed. State clearly any assumptions made.

| PROBLEM	MAX	POINTS
1	15	
2	20	
3	20	
4	25	
5	20	
TOTAL	100	

1. (15 points)

Size the transistors in the circuit below so that it has the same drive strength, in the worst case, as an inverter that has **PW = 3** and **NW = 2**. Use the smallest widths possible to achieve this ratio. Write down the size next to each transistor.
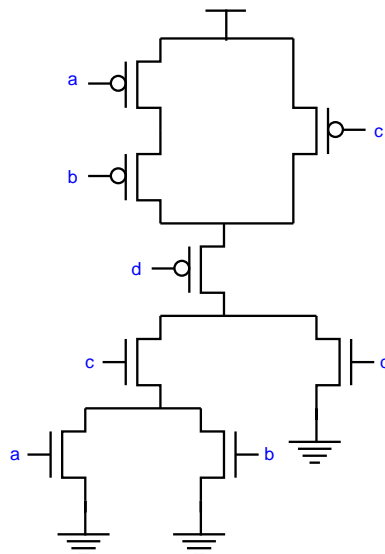
2. (20 points) Find the voltages at each of the nodes, A, B, C, D, E and F below. Use the following circuit parameters:
$V_{dd} = 5V$, $V_{tn} = 0.5V$, $|V_{tp}| = 1.5V$.
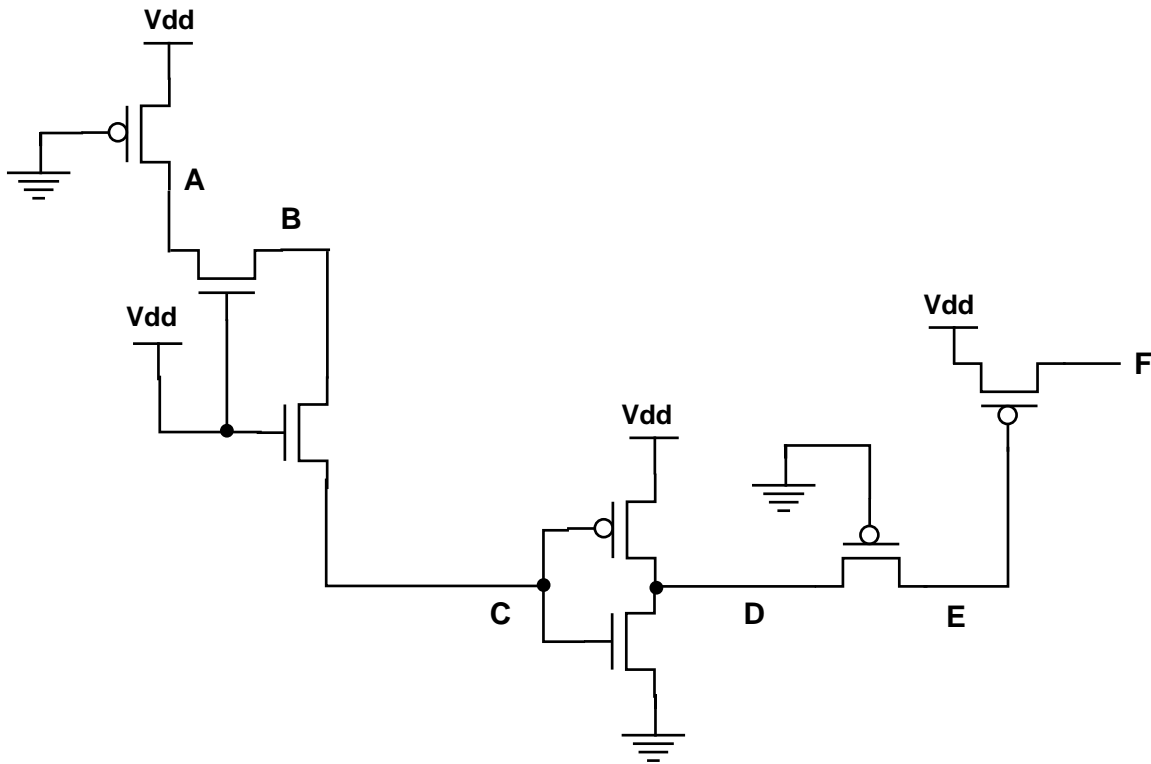
A =

B =

C =

D =

E =

F =

3. (20 points)

Use the Elmore delay approximation to find the worst-case fall delay at output F for the following circuit. The gate sizes of the transistors are shown in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance and that a minimum sized transistor has gate and diffusion capacitance equal to C. The resistance of a nMOS transistor with unit width is R. Also assume NO sharing of diffusion regions.
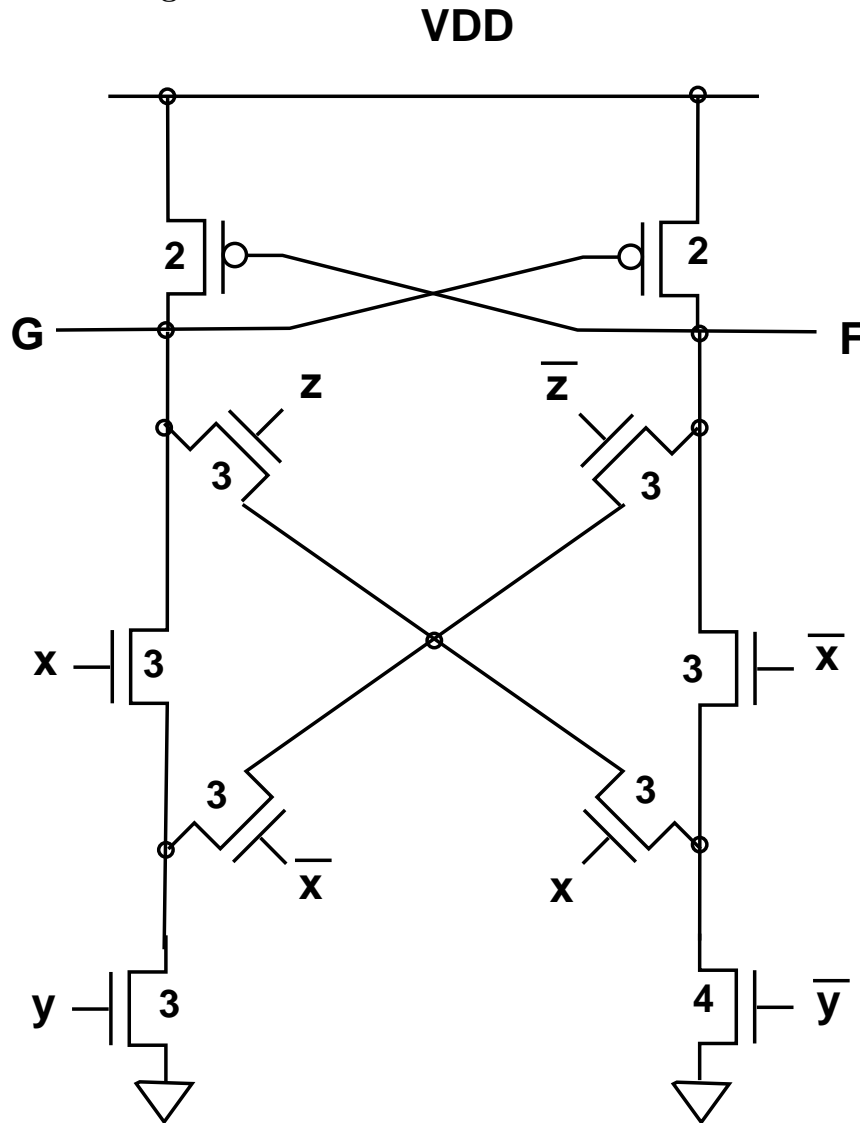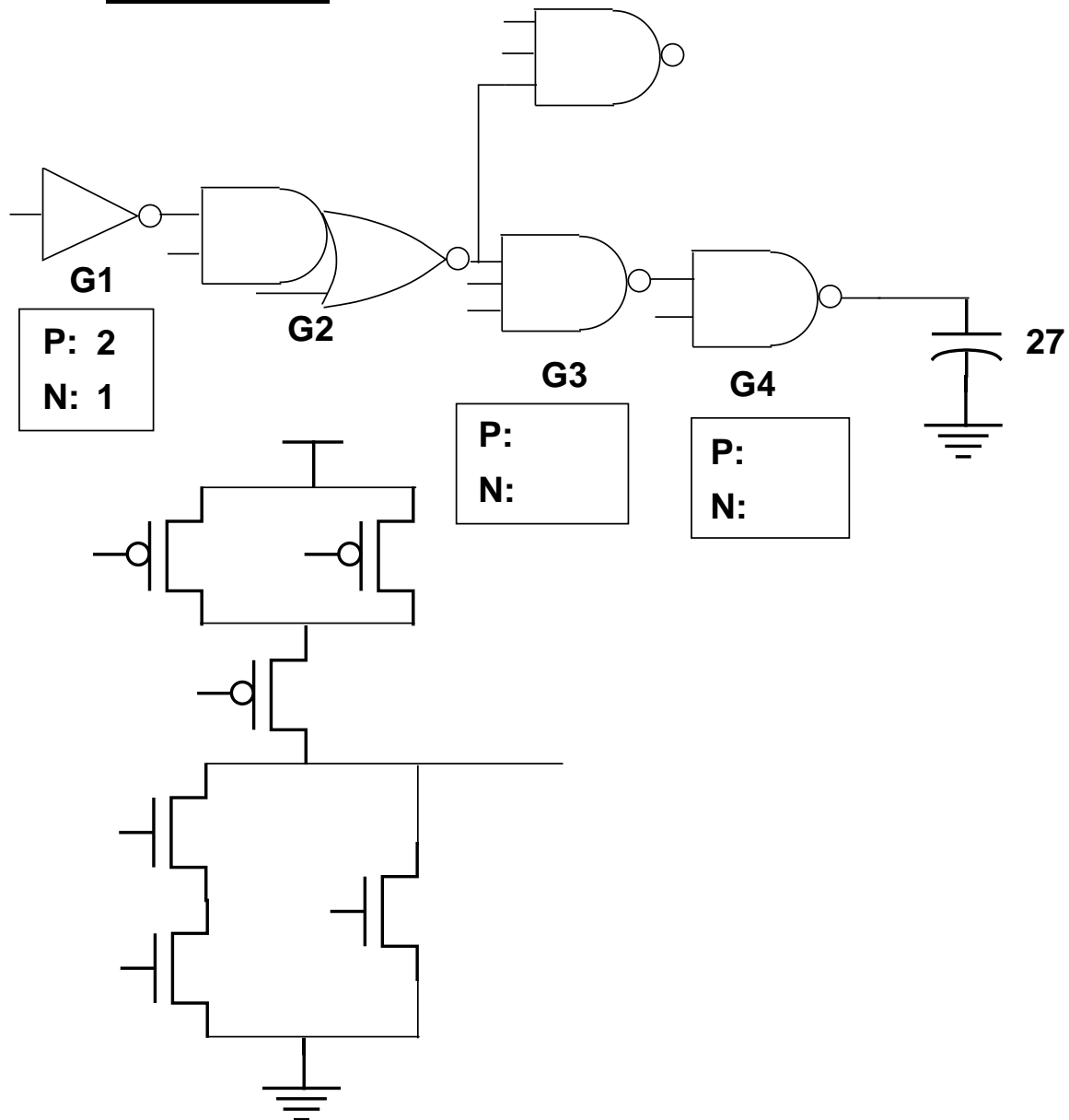

Delay =

4. (25 points)

Find the sizes of the transistors for the circuit below for the least delay from the input to the output. Label the sizes in the boxes for the simple gates and besides the transistors in the figure for the compound AOI21 gate.

Delay =

G1

P: 2

N: 1

G2

G3

P:

N:

G4

P:

N:

27

5. (20 points)

A four-level circuit has been designed to have the least delay, D, from input to output, which can be written as the sum of the path effort delay and the path parasitic delay, $D = D_F + P$.

(a) If the output capacitance is now **2** times the original capacitance, with all other parameters remaining the same, what will be the increase in delay of the circuit as a multiple of the original path effort delay, D_F?

Increase in Delay =

(b) What will be the increase in delay if the output capacitance is the same, but the parasitic delay is now **2** times the original?

Increase in Delay =

(c) If the original circuit is designed using **3-input NAND** gates, what will be the increase in delay, as a fraction of D_F if each gate is replaced with a **3-input NOR** gate (with the output capacitance remaining the same)?

(Delay Increase)/D_F =