1) What are the various regions of operation of MOSFET? How are those regions used?

2) What is threshold voltage?

3) What does it mean, “the channel is pinched off?

4) What is channel-length modulation?

5) Explain depletion region in the channel

6) What is body effect?

7) Give various factors on which threshold voltage depends.

8) Draw the Cross-sectional diagram of the CMOS.

9) Which is better: synchronous reset or asynchronous reset signal?

10) Why is the number of gate inputs to CMOS gates usually limited to four?

11) On what factors does the resistance of metal depend on?

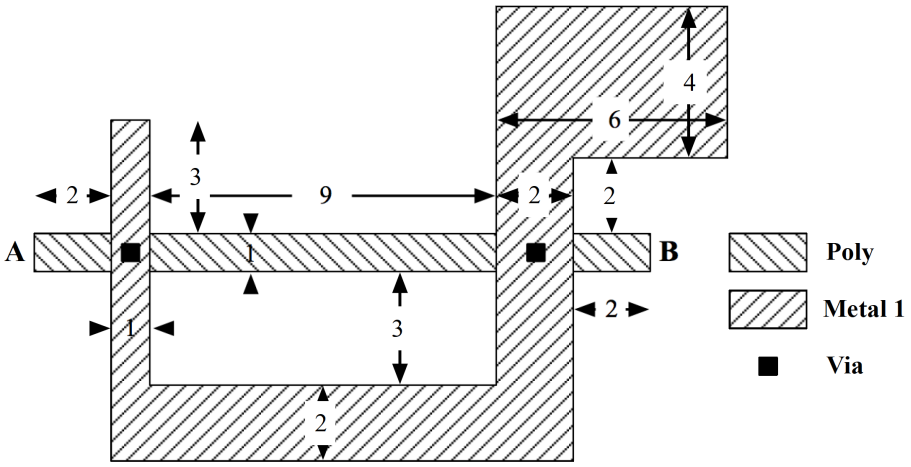
12) What are the 3 areas of VLSI optimization?

13) What are the sources of power dissipation?

14) What is the need for power reduction?

15) How do glitches in logic circuits cause power wastage?

5. (25 points) All dimensions in the figure are in μm. Polysilicon has a resistance of 30 $\Omega/\square$, metal 1 has a resistance of 0.2 $\Omega/\square$, and vias have a resistance of 25 Ω. The capacitance from metal 1 to field, C_{m1f}, is 0.1 fF/μm^2, the capacitance from metal 1 to polysilicon, C_{m1p}, is 0.15 fF/μm^2, and the capacitance from polysilicon to field, C_{pf}, is 0.15 fF/μm^2.

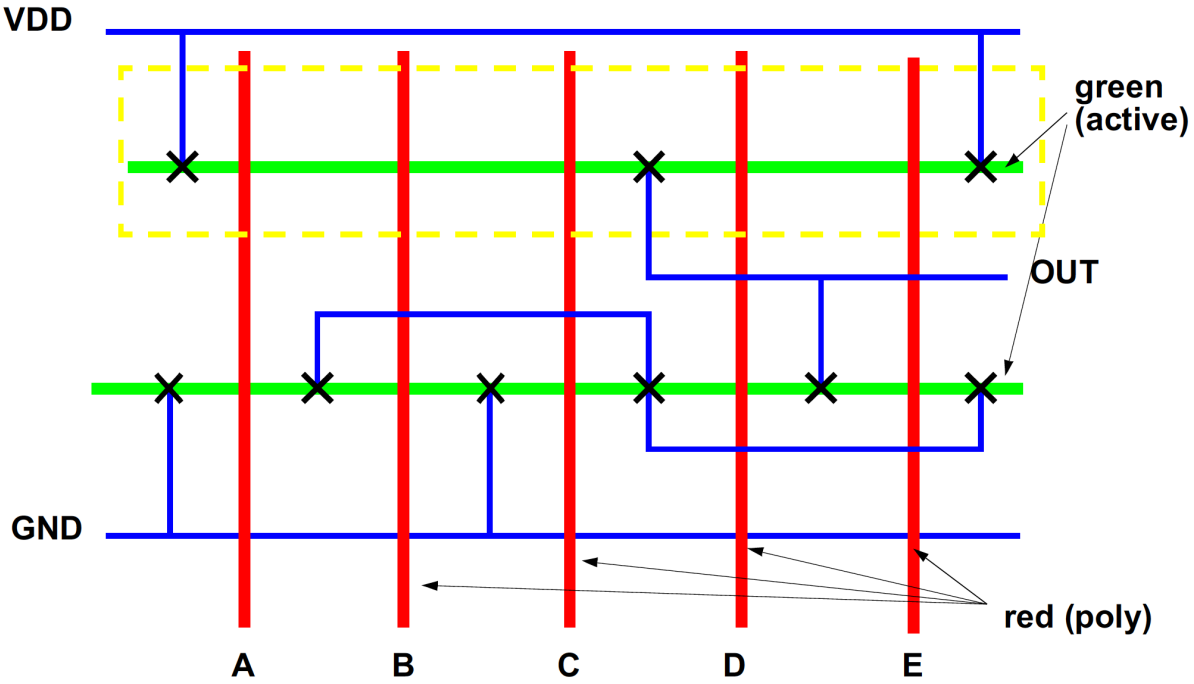


5.1 (10 points) Ignoring resistance, find the total capacitance seen from node A.

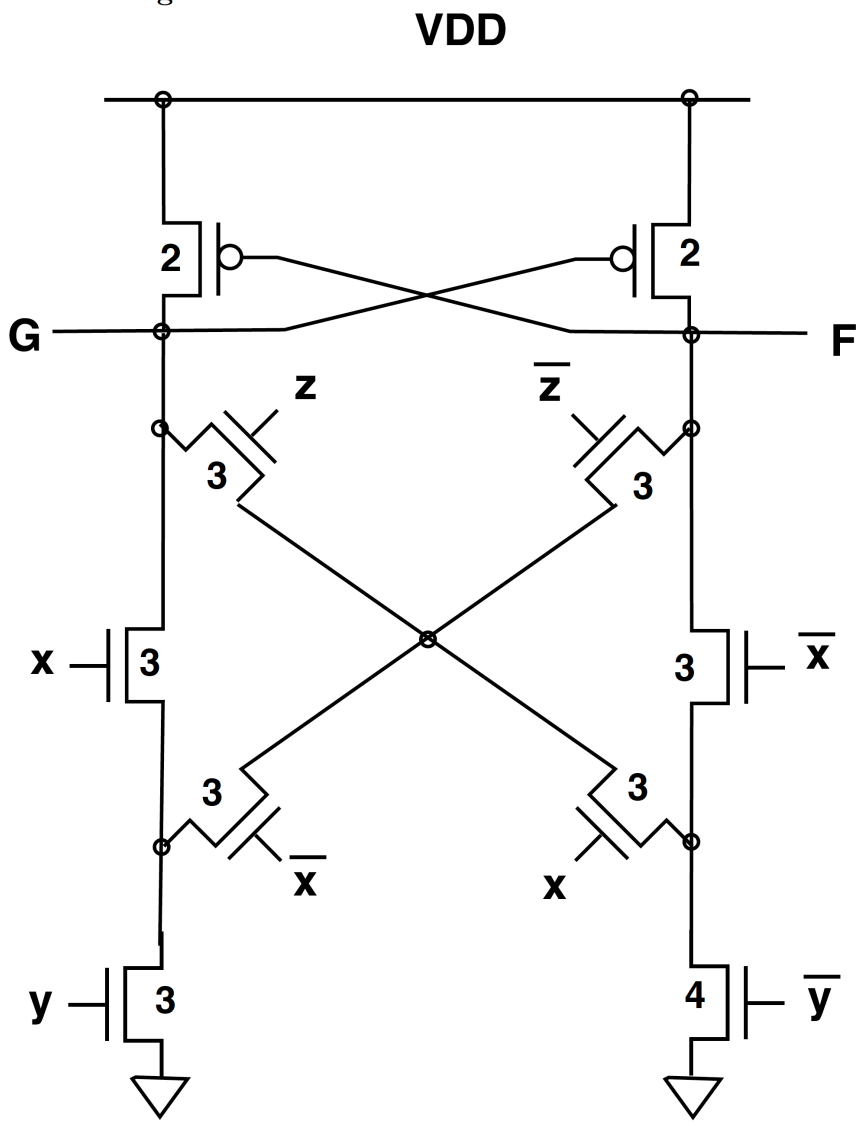
Define $\tau = 2R_N \times C_g$, where R_N and C_g denote the channel resistance and the gate capacitance of a unit NMOS ($W/L = 2\mu m \times 1\mu m$), respectively. R_P, the channel resistance of a unit PMOS, is two times R_N. *i.e.*, $R_P = 2R_N$. The mobility of NMOS, μ_N, is twice as big as the mobility of PMOS, μ_P.

1. (20%) If the Boolean function of a complex gate is $X = \overline{((A+B)\cdot C + D\cdot E\cdot F)(G\cdot H + I)}$, then
(a) (10%) Please show the **schematic** of the CMOS complex gate in terms of PMOS and NMOS **ONLY**.
(b) (10%) If the output of the above complex full-static gate is driving a load of 20Cg units, what will be the **worst-case** rising and falling delay in τ units? In your computation, assume that all NMOS and PMOS transistors are unit transistors ($W/L = 2\mu m \times 1\mu m$), and the internal diffusion capacitances can be ignored.

1. Consider the following stick diagram. Draw the electrically equivalent transistor-level schematic. What logic equation does the circuit implement?



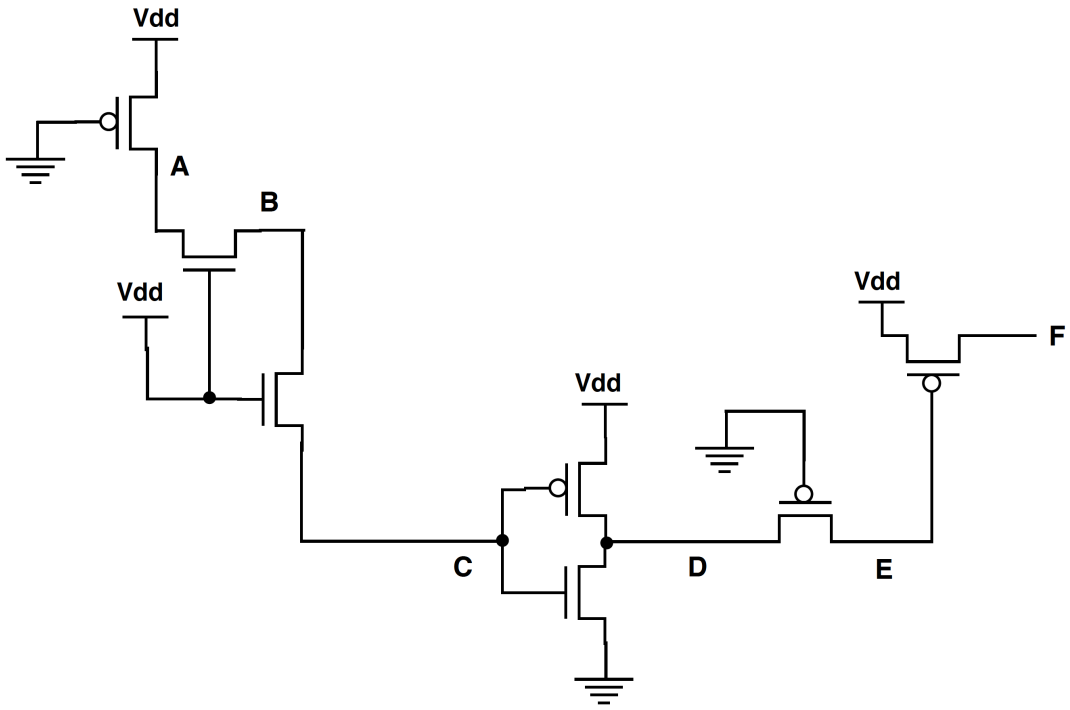
Use the Elmore delay approximation to find the worst-case fall delay at output F for the following circuit. The gate sizes of the transistors are shown in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance and that a minimum sized transistor has gate and diffusion capacitance equal to C. The resistance of a nMOS transistor with unit width is R. Also assume NO sharing of diffusion regions.



Delay = $\boxed{}$

Find the voltages at each of the nodes, A, B, C, D, E and F below. Use the following circuit parameters:

$$V_{dd} = 5V,\ V_{tn} = 0.5V,\ |V_{tp}| = 1.5V$$



$\mathbf{A} =$

$\mathbf{B} =$

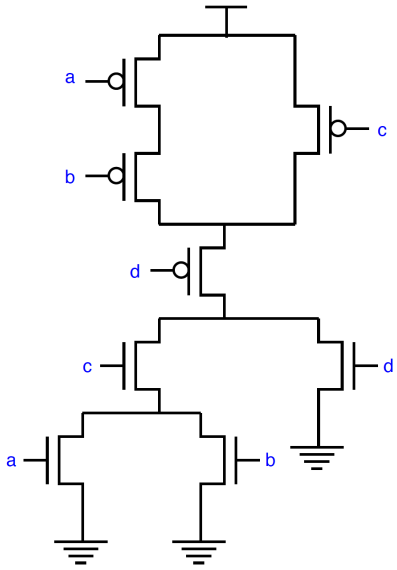
$\mathbf{C} =$

$\mathbf{D} =$

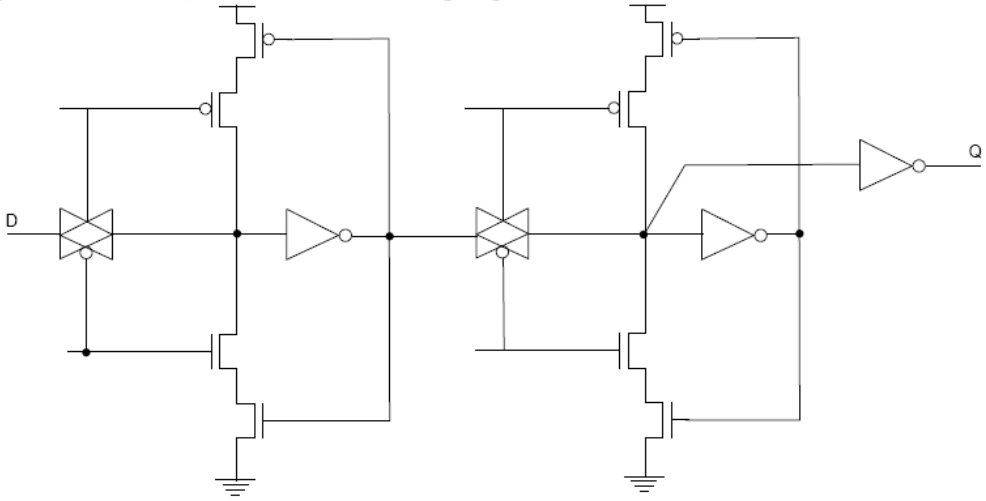
$\mathbf{E} =$

$\mathbf{F} =$

Size the transistors in the circuit below so that it has the same drive strength, in the worst case, as an inverter that has PW = 3 and NW = 2. Use the smallest widths possible to achieve this ratio. Write down the size next to each transistor.



(a) Label the four inputs in the circuit below with the clock symbols CLK and CLKB (complement of CLK) so that the flop latches at the falling edge of the clock.



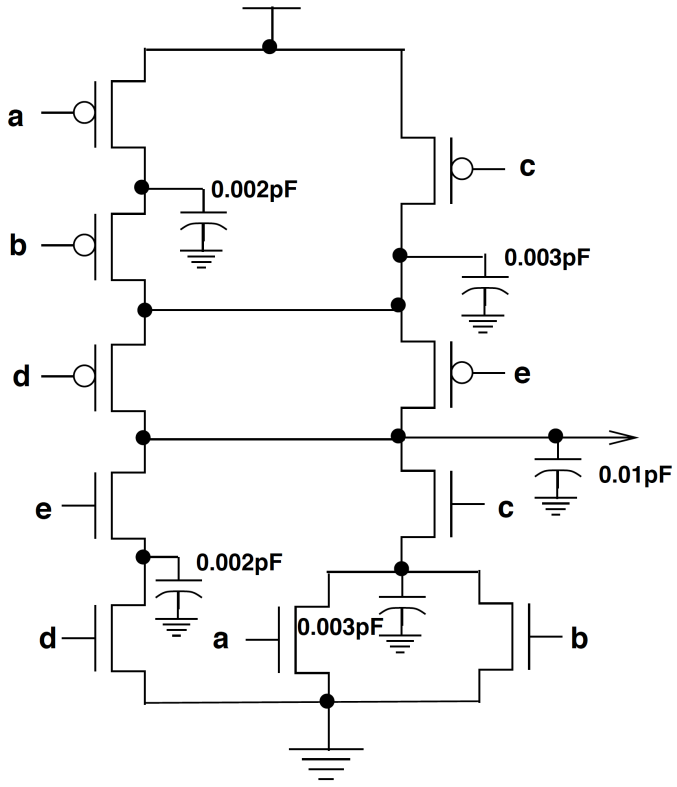
a) Draw the schematic for a static CMOS network for the following function using the minimum number of transistor. Do NOT assume that the inverted inputs are available.

Y = A'B'C' + ABC' + A'B'C + ABC

b) Draw a Domino CMOS schematic (with PMOS precharge and feedback hold device) of the following functions F1 and F2 using the minimal number of transistors.

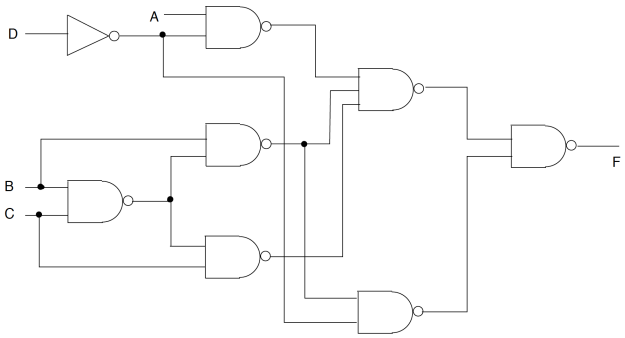
F1 = (M·N + W) · P · (Q·R + S·T)
F2 = T·S + R·Q

In the static CMOS circuit below, the on-resistance of each n-channel transistor is 5 KOhms and that of a p-channel transistor is 10 KOhms. The gate capacitance of an n-channel transistor is 0.02pF and p-channel transistor is 0.03pF. The source/drain capacitance of an n-channel transistor is 0.001pF and for a p-channel transistor is 0.002pF. The routing capacitances for interconnections are lumped at the nodes as shown.



(a) Find the delay when (a b c d e) makes the following transitions:
0 0 0 0 0 $\Rightarrow$ 0 0 0 1 1 $\Rightarrow$ 0 0 0 0 1.

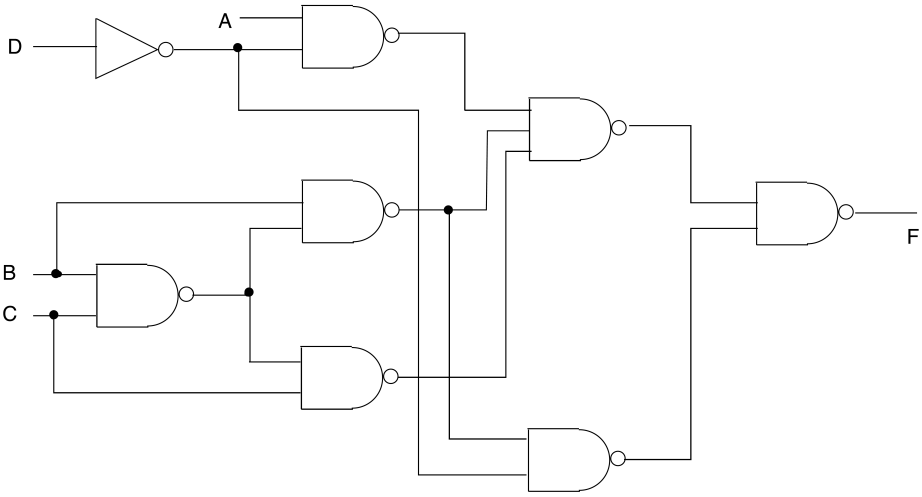
A circuit and the parameters of its library cells are given below.

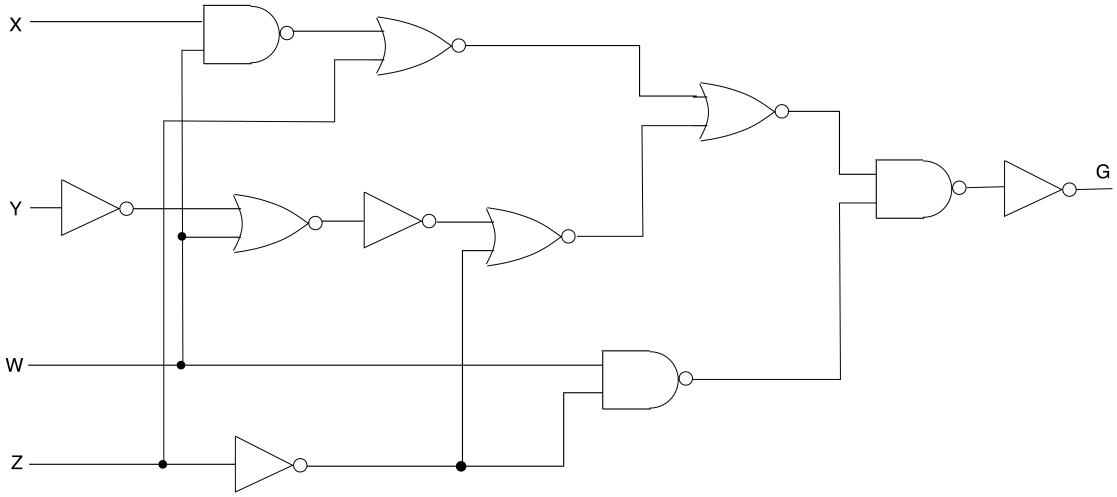


Gate	Fanout	Rise Delay	Fall Delay
Inverter	1	100	80
Inverter	2	120	100
Inverter	3	160	130
Nand	1	140	140
Nand	2	150	160
Nand	3	160	180
Nor	1	220	180
Nor	2	240	200
Nor	3	280	230

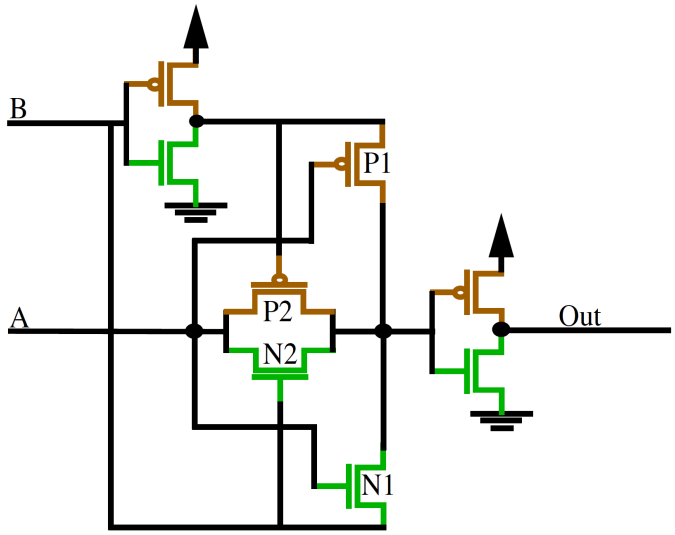
Find the longest functional paths from inputs D and C to F and give the rise and fall delays.

Compare the circuits below and find the input mappings which would make them equivalent.





2) a) (6 pts) Give the truth table for the following transistor level schematic. Explain the source of 'good' logic 0's and 1's (using the labels P1, P2, N1 and N2) under each of the four input combinations.



b)(6 pts) Give the minimum CMOS realization of an XNOR ($f = \overline{a \oplus b} = ab + \bar{a}\bar{b}$). Assume the **un**complemented inputs ***a*** and ***b*** are available. Show your work.