

Fall 2006

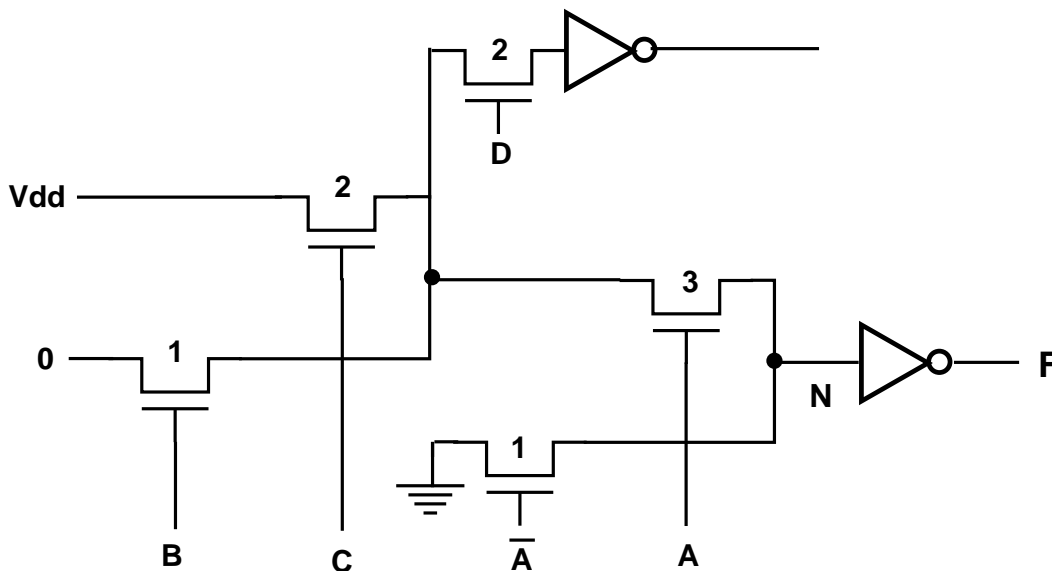
VLSI Design  
EXAM. IIJ. Abraham  
November 20, 2006

Name: Exam, No. 2

- Open Book, Open Notes.
- Time Limit: 75 minutes (pace yourself).
- Check for 6 pages in exam.
- Write all your answers in the spaces/boxes provided.
- Show any calculations in these pages using the back of the pages if needed.
- State clearly any assumptions made.

1. (20 points)

The inverters in the circuit below have minimum-sized transistors and the widths of the pass transistors are shown in the figure. Assume that the diffusion capacitance of a transistor is equal to its gate capacitance, and that a minimum sized transistor has gate and diffusion capacitance equal to  $C$ . In addition,  $V_{dd} = 2V$ ,  $V_{tn} = 0.3V$  and  $|V_{tp}| = 0.4V$ .



The sequence  $ABCD = (0011, 1001)$  is given as input to the circuit. Write down the voltage on node N just after the sequence is applied.

Voltage on Node N =

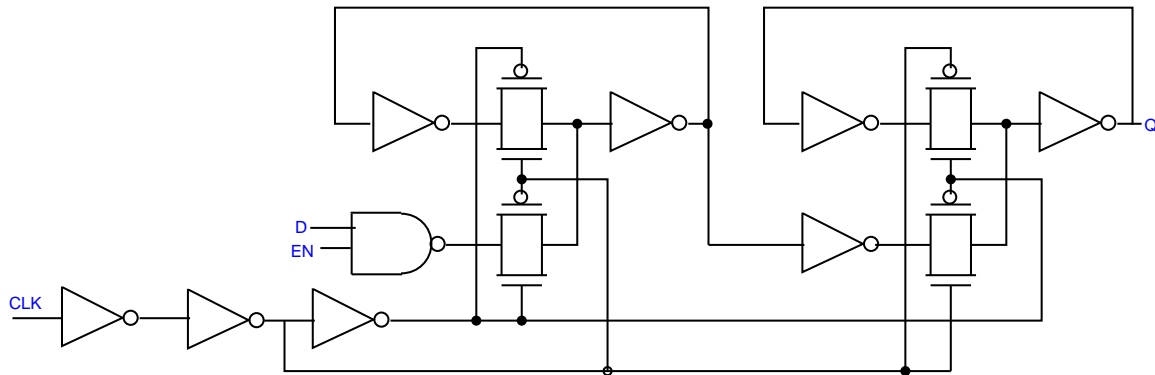
2. (20 points)

The components of the flip-flop below have the following rise/fall delays (in picoseconds).

Nand gate: 75/125

Transmission gate: 75/75

Inverter: 50/50



What are the values of the following flip-flop parameters (which a designer needs to use to calculate the performance of a system)?

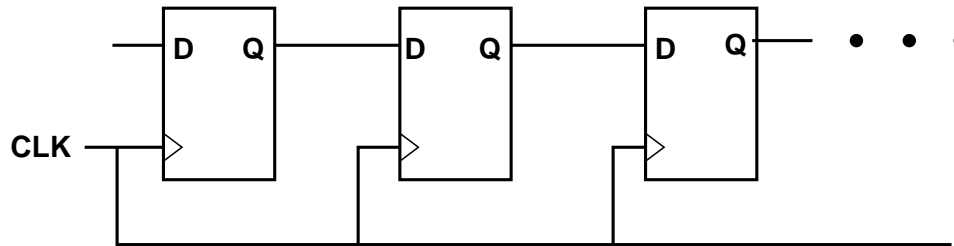
(a) Setup time =  ps

(b) Hold time =  ps

(c) Clock-to-Q delay =  ps

4. (20 points)

The flops used in the shift register below have a setup time of 100 ps, a maximum clock-Q delay of 150 ps, and a minimum clock-Q delay of 100 ps.



(a) How fast can this circuit be clocked?

Clock frequency =  MHz

(b) What is the limit on the hold time of the flops at this frequency?

Hold time <  ps

(c) What is the limit on the hold time of the flops at a frequency of 1 GHz?

Hold time <  ps

(d) What is the limit on the hold time of the flops if the circuit is clocked at a frequency of 100 MHz?

Hold time <  ps

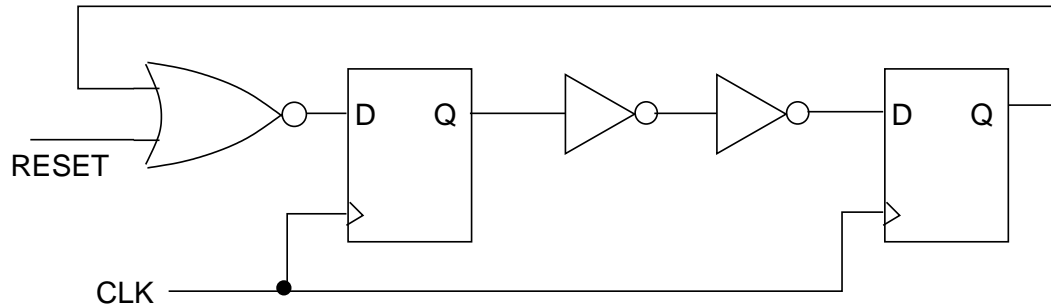
3. (20 points)

(a) What is the highest frequency at which the following circuit can be operated correctly? The parameters of the components are as follows.

Inverter:  $t_{pd} = 200ps$ ,  $t_{cd} = 100ps$

2-input NOR:  $t_{pd} = 200ps$ ,  $t_{cd} = 150ps$

D-flop:  $t_{pd} = 200ps$ ,  $t_{cd} = 0ps$ , Setup time = 300 ps, Hold time = 100 ps.



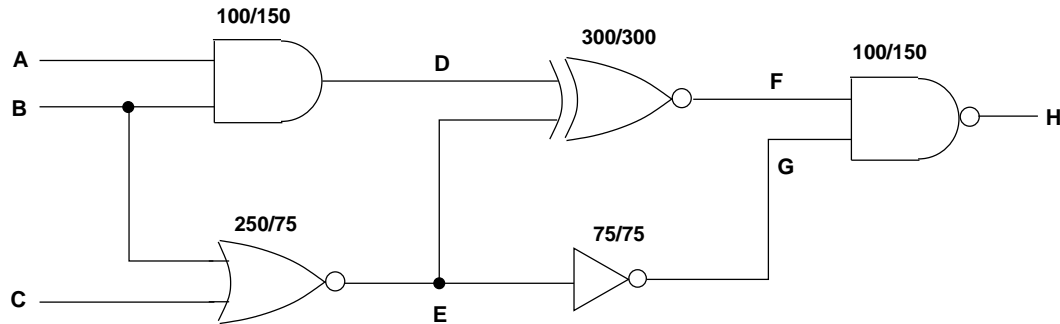
Maximum Clock frequency =  MHz

(b) If the two inverters are removed (the Q of the first flop is connected to the D of the second), what will be the highest frequency at which the circuit can be operated. Explain your answer.

Maximum Clock frequency =  MHz

5. (20 points)

(a) Write down all the paths from input B to the output and the worst-case and lowest delays for each path in the circuit below. The rise and fall times (in picoseconds) for each gate are shown over the gate symbol as risetime/falltime.



For example, the paths from input A to the output, and the delays are:

Path	Worst-case delay	Lowest delay
ADFH	600 ps	500 ps

(b) Give the test sequences for the following cases:

(i) Rising input on B, path BDFH

(i) Falling input on B, path BEFH

(ii) Rising input on B, path BEFH