EE 382M-8 VLSI-II Spring 2011 -- HW #1

Assigned: Jan. 24, 2011 Due: Feb. 14, 2011

Problem 1.1 (40 points) Max Frequency

Use HSPICE to determine the maximum frequency and the average power dissipation of a pre-designed static CMOS logic circuit, including interconnects and master-slave flip-flops (MSFFs). You will be given a complete netlist and schematic for the circuit in a **65nm** technology that features copper interconnects. The circuit is an actual 2-stage pipeline slice from an advanced microprocessor structured data-path (see lecture slides).

Collateral you will need to complete Problem 1.1:

Copy the following files from:

http://users.ece.utexas.edu/~mcdermot/vlsi/main/hw/hw1/

to your HSPICE simulation directory:

hw1_schematic.pdf – schematic needed for this problem

hw1p1.sp - top-level HSPICE netlist & simulation deck for the circuit

65nm_NMOS_bulk_TT.txt – NMOS MOSFET models for a 65nm semiconductor technology

65nm_PMOS_bulk_TT.txt – PMOS MOSFET models for a 65nm semiconductor technology

library-65nm.txt - library of circuit elements (logic gates, transmission gates, tristate inverters, MSFF, and interconnect elements)

block1-65nm.txt - logic for the first pipeline stage

block2-65nm.txt - logic for the second pipeline stage

Procedure

Characterize the given circuit for maximum functional frequency (F_{max}) over 6 PVT corners (Process, Voltage and Temperature design simulation corners). Modify hw1p1.sp, as needed, without changing the given circuit. Use the given 65nm models, a range of V_{dd} (1.1, 1.0, 0.9 V) and two temperatures (25, 125 ºC) (for a total of 6 separate corners). The nominal V_{dd} is 1.0V.

To determine the max operating frequency (F_{max}) of the circuit, find the maximum clock rate, with a resolution of 100 MHz, at which the circuit will correctly operate. For the purposes of this assignment, the maximum operating frequency is defined as the highest clock frequency for which the total latency of the circuit (time from the first clock edge after the data input transition to the transition of the final output) is no greater than 2.2 * the clock period. When determining the maximum operating frequency, be sure to apply a worst-case input transition. When you report a maximum operating frequency, this means that the circuit is guaranteed to work at that frequency no matter what inputs are applied to the A0_IN and B0_IN signals. (The pipeline slice is a 2-stage pipeline, so it takes 2 cycles for the data to propagate from the input

of the 1st stage to the output of the 2nd stage. The extra 0.2 cycle accounts for the clock-to-output delay of the last MSFF in the pipeline.)

To determine F_{max}, be sure to apply a worst-case input transition. The circuit must be shown to work at F_{max} with all possible A0_IN and B0_IN inputs (00, 01, 10, 11).

Use $V_{dd}/2$ to $V_{dd}/2$ when measuring the delay from one signal transition to another signal transition (including the clock).

Use a 50% duty cycle for the clock signal. This means that the clock should be above $V_{dd}/2$ for 50% of the time, and below $V_{dd}/2$ for 50% of the time.

Use 50ps for the input rise and fall times for all signals (data and clock) in the HSPICE stimulus code. Remember that rise and fall times in HSPICE stimulus code are 0-100%.

Notice that the MSFF elements are inverting – a logical inversion is performed between the D input and Q output of the MSFF (MSFF schematics included in the Flip Flop Lecture Notes).

Suggestion: Use a transient analysis in HSPICE to sweep the clock frequency. Keep the inputs steady and run the clock for a few cycles to ensure that the circuit stabilizes to a steady state. Apply an input transition with enough setup time to the next rising edge of the clock (try 100ps). Measure and record the fastest clock frequency at which the circuit functions properly. Begin with 1.0 GHz and increment up in steps of 100 MHz until circuit functionality failure.

Hint – some possible ways to sweep over 10 points in a transient analysis:

tran tstep tstop tstart SWEEP sweepvar sweepstart sweepstop sweepstep

tran tstep tstop tstart SWEEP sweepvar LIN 10 sweepstart tsweepstop

tran tstep tstop tstart SWEEP sweepvar POI 10 p0 p1 p2 p3 p4 p5 p6 p7 p8 p9

What To Submit

Your submission for this problem consists of (1) a paper report and (2) an electronic submission of your HSPICE files.

1. Report:

- Plot F_{max} vs V_{dd} (1.1V, 1.0V, 0.9V) for 25 and 125 ºC (in the same panel) – expect to see 2 lines.
- Plot Power (mW) vs V_{dd} (1.1V, 1.0V, 0.9V) for 25 and 125 ºC (in the same panel) – expect to see 2 curves. $I_{Vdd} * V_{dd}$.
- Does the power verses V_{dd} follow a $P=CV^2f$ relationship – do you expect it to? How does the temperature affect this relationship? Remember that F_{max} is changing for each (V_{dd} -Temperature pair) datapoint on the graph.

(2) Electronic submission of your HSPICE files:

Submit any HSPICE files that you created or modified to do this problem. (Don't submit files that you did not change or did not create.) Send these files via email to TAs with a subject line of "HW1 Problem 1". (Your email must be sent by 6:00 p.m. on the day this assignment is due.)

Problem 1.2 (40 points) Scaling

Using constant field scaling, shrink problem 1.1's 65nm circuit to 45nm technology; estimate the new Fmax and power, again using constant field scaling; the following guidelines should apply:

- MOSFET channel lengths will decrease from 65nm to 45nm (a scale of 0.7x).
- Assume that MOSFET widths, clock-to-output delay of MSFF's, logic delay of static CMOS gates, and the length of interconnect runs will scale by a factor of 0.7 (this is a simplifying assumption).
- The nominal V_{dd} of the circuit in 45nm technology will be 0.8 V. The nominal V_{dd} of the circuit in 65nm technology will be 1.0 V.
- Interconnect capacitance per unit length does not scale and remains at 1.0x; do note that routing distances do scale by 0.7X. Interconnect resistance per unit length increases by 2x.
- Assume that the input setup time of the MSFFs will NOT scale (keep it constant when scaling from 65nm to 45nm.)

Before you do the scaling, you may need to look back at the Problem1.1 HSPICE simulations. Find the delays for each gate in the given network.

After estimating the new R and C for each interconnect element in the 45nm technology, predict the new delay of each interconnect by using the formula 0.5*R*C (the metal interconnect elements are netlisted as "iconn" elements). The "C" in the estimation formula here is the total capacitance of the interconnect. To compute the total capacitance seen in the interconnect, you will need to sum up the capacitances at each end of the interconnect resistance, including the capacitance of the gate at the receiving end of the interconnect element, before using the estimation formula.

Power dissipation depends on three primary factors: interconnect capacitance, transient power dissipated due to switching, and transistor leakage current (assume leakage is minimal in this exercise). Remember that power is proportional to CV^2f (where C is the switching capacitance, V is V_{dd}, and f is the switching frequency).

What To Submit

For the scaled circuit operating at 0.8V, 25 ºC, predict the following:

- The estimated maximum operating frequency of the 45nm circuit **(30)**
- The power that the circuit will consume during 2 clock cycles of useful work **(10)**

Show all the steps and work you used in the process of arriving at your predictions.

Suggested Procedure for Problem 1.2:

The steps to predicting the maximum operating frequency:

1. Run the 65nm circuit for the worst case input transition using HSPICE. This was done as part of Problem 1.1

2. Determine the delays of each of the individual simple/complex gates. To do this, measure the time between the Vdd/2 of the input transition of a gate to the Vdd/2 of the output transition of that gate.

3. Once you have got these delay numbers for the gates, scale them to 45nm. The problem clearly states how the delay scales.

4. Next, characterize the flops for optimal setup and clock-to-Q. Note that all the flops in the given circuit are instances of the same macro. Therefore, if you do it for one of them, you have done them all.

5. To simulate a flop, sweep the input setup time from a large value to a small value (start with 100ps). Measure the delay between Vdd/2 of the clock and Vdd/2 of the flop output transition. This is Clk-to-Q. You will notice that the clk-to-Q remains nearly constant for large setup times and then starts to increase. The optimal setup time will be that setup time at which the FLOP clk-to-Q is 10% higher than its value at a setup time of 100ps.

6. So now, you have the setup time and the clk-to-Q of the flop. From the problem statement, you know how these values will scale. Simply use the scaling factor to estimate 45nm data.

7. Now comes the interconnect delay. Use 0.5*R*C. You know the new values of R & C for the 45nm circuit, because you are given the scaling factors for the interconnect cap and resistance.

8. Now that you have all the data necessary,

   clock_period_per_stage = scaled clk-to-Q (of the input flop)
   + scaled delays of individual gates (in that pipe-line stage)
   + scaled interconnect delays
   + optimal setup (for the output flop)

   Determine in which stage the required clock period is the max (stage1 or stage2 delay?).
   $1/Delay_{max,\ stage} = F_{max,clk}$

9. Now for the power dissipated: get the total capacitance of the ckt (after accounting for scaling) and then use the all too familiar formula. You may also use the power (from HW1.2) and scale it for 45nm.

Problem 1.3 (40) Max Frequency

Use HSPICE to determine the maximum frequency of a pre-designed static CMOS logic circuit, including interconnects and master-slave flip-flops (MSFFs), and Local Clock Buffers (LCBs). You will be given a complete netlist and schematic for the circuit in a 65nm technology that features copper interconnects.

The circuit is the same as the one used for Problem 1.1, except that it has been modified to add a realistic clock distribution network (see Lecture foils). This network consists of a global clock node routed to 3 local clock buffer (LCB) units. Each LCB provides a local clock signal that is used to drive the clock input of a nearby MSFF unit.

The distribution network is not uniformly loaded: it is heavily loaded at the input MSFF stage in the pipeline, and lightly loaded at the intermediate MSFF and output MSFF. The load has been modeled using NMOS gate capacitance connected to the local clock node.

Collateral you'll need to complete this assignment

Copy the following file from:

http://www.ece.utexas.edu/~mcdermot/vlsi/main/hw/hw1/

hw1p3.sp - top-level HSPICE netlist for the circuit, using local clock buffering

For the remaining files, use the files that you used in Problem 1.1

hw1_schematic.pdf – schematic needed for this problem

65nm_NMOS_bulk_TT.txt – NMOS MOSFET models for a 65nm semiconductor technology

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Procedure

Simulate the given circuit (over the same 6 PVT corners used in Problem 1.1) to determine the maximum frequency (of the global clock) for each corner.

What To Submit

- Plots (as in Problem 1.2):

  - The maximum operating frequency (Fmax) of the circuit (to the nearest 100 MHz) vs. Vdd (1.1V, 1.0V, 0.9V) for 25C and 125C. **(25)**

  (Note: you need not report the amount of power consumed by the circuit)

- Answer the following questions:
  - Measure the clock slew rate at the clock inputs of all FFs (4 total). How does this slew rate compare to the ideal 50ps used in Problem 1.2? Use 20-80% for the risetime. **(5)**
  - Why did the max frequency of the circuit change when the LCBs were used to distribute the clock to the MSFFs? What impact would this have in a real design? **(5)**
  - What factors would you consider in determining where to place (and load) the LCBs in the floor plan of a chip and how many LCBs to place? **(5)**