EE 382M VLSI-II Fall 2011 -- HW #2 Assignment

Assigned: Sep. 16th, 2011 Due: Oct. 15, 2011

Part 2.1: (20 points) Area Estimation for EDP

a) **Register File area estimation (10) in 130nm CMOS:** Assume word-lines are routed in M3 with a pitch of 0.6um. Local bit-lines are routed in M2 with a pitch of 0.6um and global bit-lines and data-lines are routed in M4 with a pitch of 0.8um. Assume word-lines and global bit-lines are half-shielded.

Estimate the area of a 128 entry, 32bits/entry, 5R/3W array. Assume 16 cells per local bit-line and each local bit-line receiver and write data driver is the same area as one cell. Assume decoders make up 20% of the total array area.

b) **Small signal array area estimation (10) in 130nm CMOS**: Assumptions to estimate a 4KB data cache:

- The area of a high performance 6T bitcell in a 130nm CMOS technology is 2.6 μm^2.
- The bitcell sub-array is comprised of 256 columns and 128 rows (32,768 bits).
- Each word is 32b wide (Din and Dout is 32b wide).
- Assume an array efficiency of 50%.

Answer the following questions:

1. How many sense-amps are required?
2. How wide are the column decoders?
3. How many address lines are required?
4. What is the area of this 4KB data cache?

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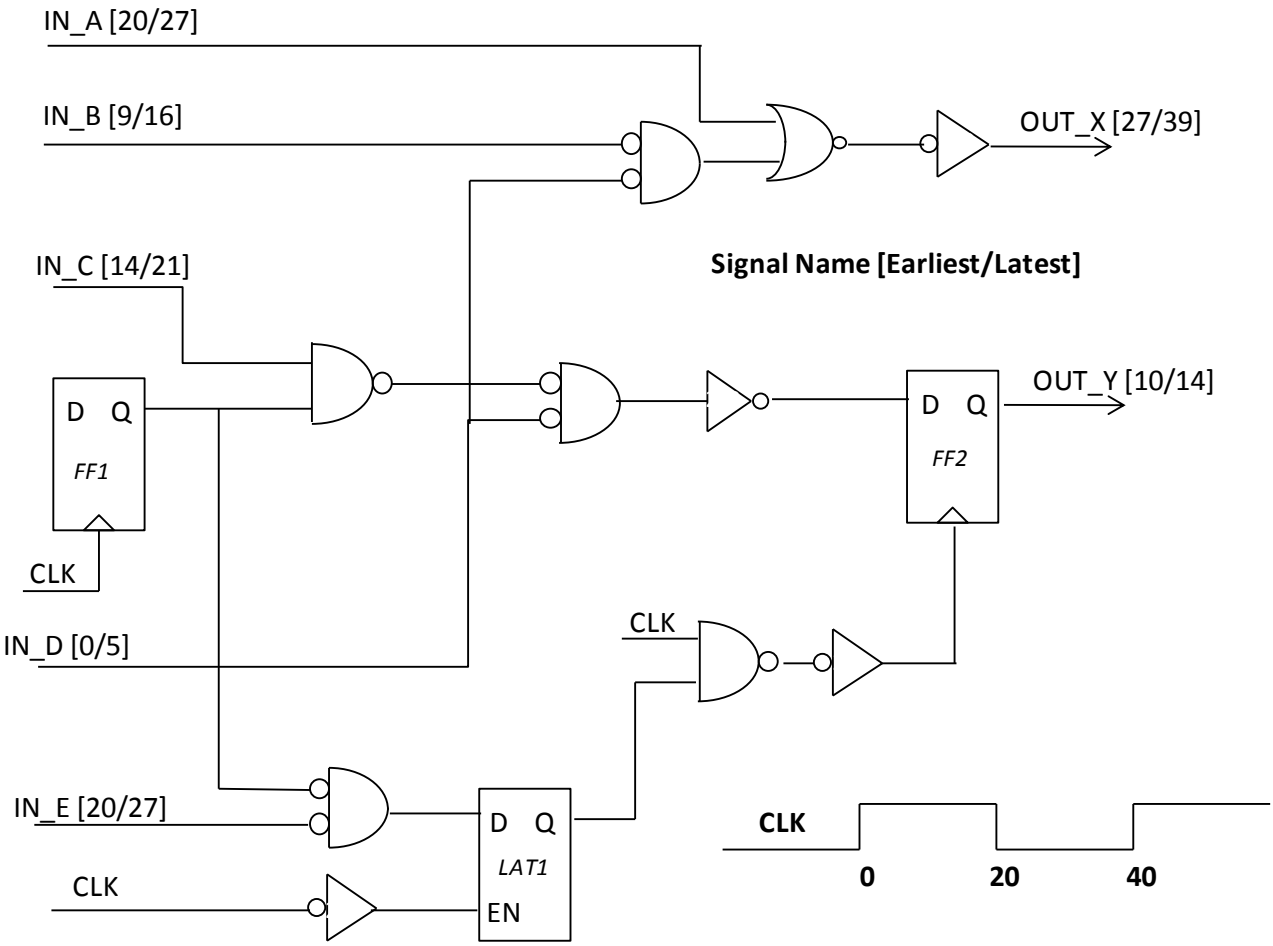
Problem 2.2 (30 points): Timing

The I/O timing constraints for this circuit are annotated on the schematic below. The first number is for "Min Mode" timing and the second number is for "Max Mode" timing. Your task is to a) identify the critical min and max paths to the primary outputs OUT_X and OUT_Y and b) to find the min and max slack for this circuit.

Note that the timing delays for each combinational logic gate type are given below. The clock period is 40 units. For robustness the integration team has determined that there is a restriction that the setup time to a clock gater will be [1/1] i.e., 1 unit for "Min-Mode and 1 unit for "Max-Mode".



GATE Type [Fastest/Slowest]		
2-NAND [3/5]	DFF Setup [8/12]	Latch D-Q [5/7]
2-NOR [4/6]	DFF Hold [8/12]	Latch C-Q [6/8]
INV [2/3]	DFF C-Q [5/7]	Latch Hold [0/1]

HINT: Don't forget about cycle-adjust requirements for some paths.

a) What are the critical "Max" paths in this circuit?
b) What are the critical "Min" paths in this circuit?
c) What are the Max-Mode slacks for LAT1 & FF2?
d) What are the Min-Mode slacks for LAT1 & FF2?

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Problem 2.3 (20 points): Power Estimation & Reduction in CMOS circuits

In a 0.18um technology, a processor design has an area of 100mm^2 and runs at 1 GHz at a typical voltage of 1.8V. Assume that at any given time, approximately half the transistors in the processor are on and half are off; also assume that the Stack Effect = 0.5 and the switching activity factor (AF) = 0.5.

a. Estimate total processor power assuming:

   Cswitch-den = 120pF/mm^2
   Transistor Density = 60K/mm^2
   Wavg = 3um
   Isubthreshold = 200nA/um
   Igate = 50nA/um

b. In a 130nm technology with a typical voltage of 1.5V, the same processor design runs at 1.4GHz. Assume an $I_{subthreshold}$ of 500nA/um and Igate of 250nA/um and all linear dimensions scale by 0.7. Calculate total power.

c. List (in priority) all sources of power (both dynamic and leakage) that any CMOS circuit (with a ***Ceff*** capacitance) dissipates when powered by a ***VDD*** power rail and operated at ***F*** frequency.

d. Describe 3 methods to reduce ***leakage*** power ***without*** adversely affecting gate performance or overall block performance (something to keep in mind: typically, a small number of paths in a block or CPU set the maximum frequency of operation).

e. What is the difference between ***active*** leakage power and ***stand-by*** leakage power?

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Part 2.4: (30 points) 65nm FLOP characterization

For both Din transitions (0->1 and 1->0), determine the input setup (Tsu), input hold (Th), and clock to out (Tcq) for the following 3 FLIP FLOPS (a, b, c). Use 50ps slew rate (full rail) for Din and clock; use the 65 nm CMOS transistor models. For the Tcq measurement, use a Din Tsu. These designs are all driving a 4.2/2.1 inverter.

Show ALL your work; also answer the following questions pertaining to each design:

a) List 3 deficiencies with this design. Hint: look at b, c designs.

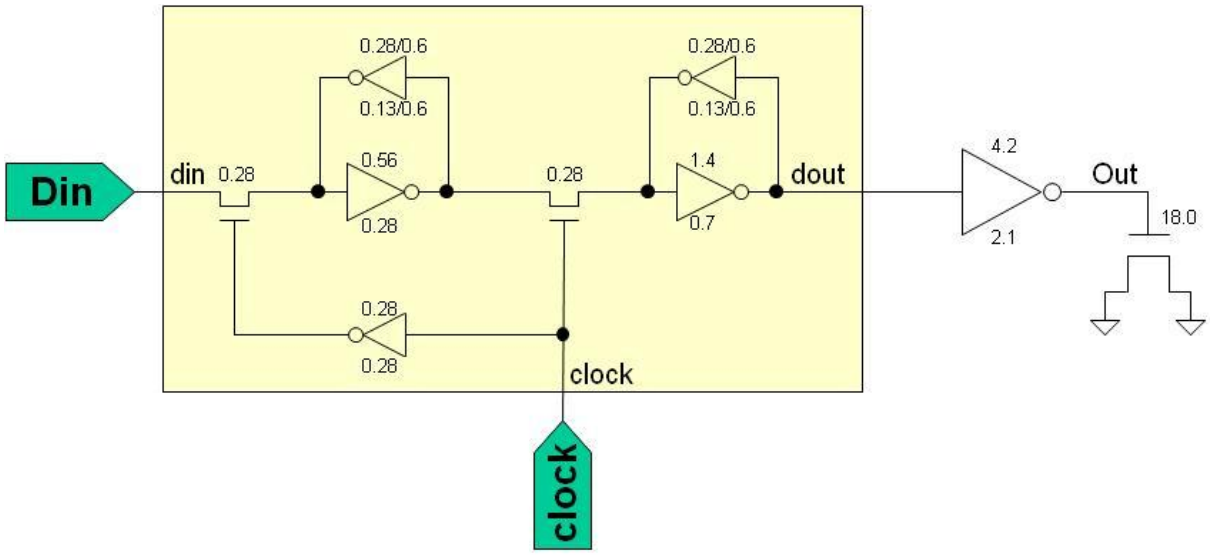
b) Is the Din input capacitance lower than design a? What about the clock capacitance?

c) What are the benefits of placing the slave latch off to the side? Is this a time-borrowing FLOP? Is the clock capacitance lower than design b? Any benefit in clocking the master LATCH feedback?

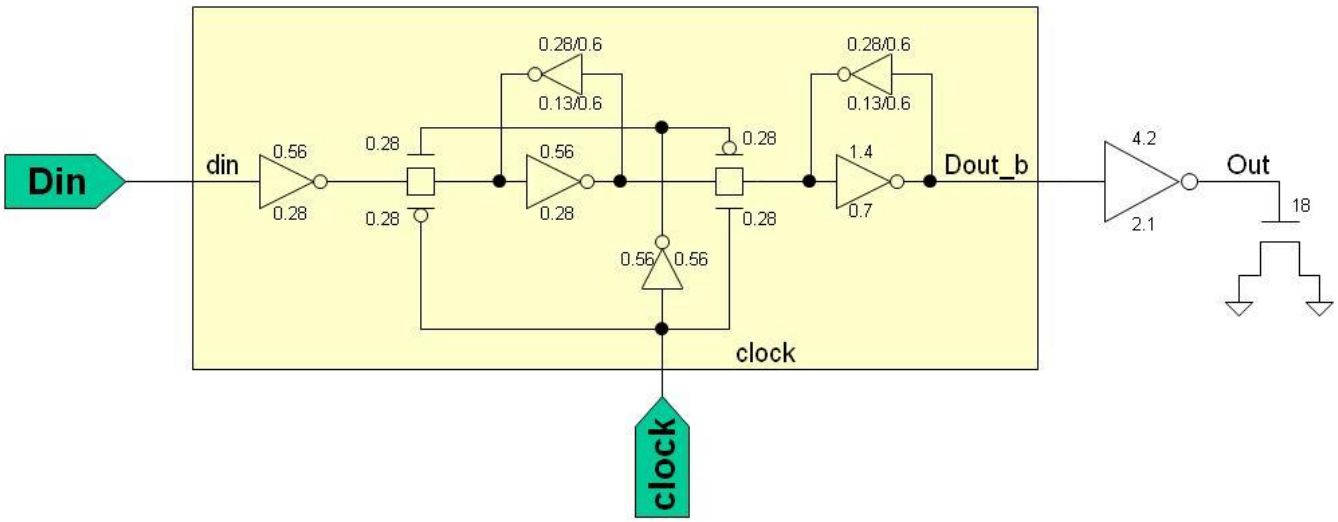
Simulation Tips:

- Use a TEMP=90C, VDD=1.5V, TYPICAL transistor models.
- Use HSPICE ic statements to properly initialize these sequential circuits.
- Use a Din-to-clock step-size of 10ps to search for Tsu, Th and Tcq.
- If a channel length is not specified, then use nominal 45nm transistor length.
- Netlists are located here: http://users.ece.utexas.edu/~mcdermot/vlsi/main/hw/hw3/

a) FLOP for part a).



b) FLOP for part b)



c) FLOP for part c)