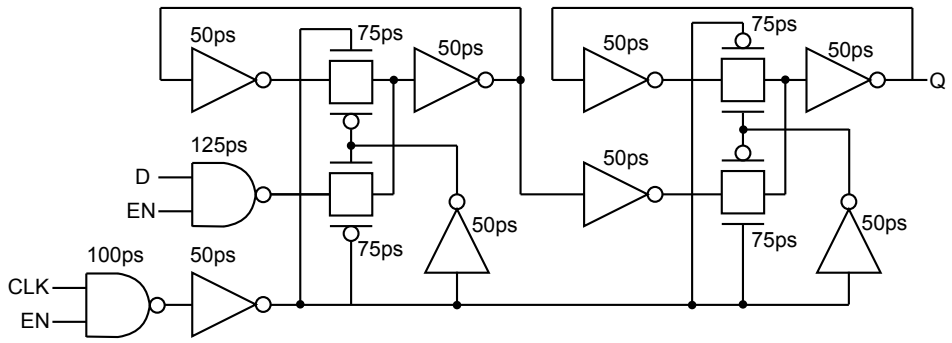
VLSI Design, Fall 2017

J. A. Abraham

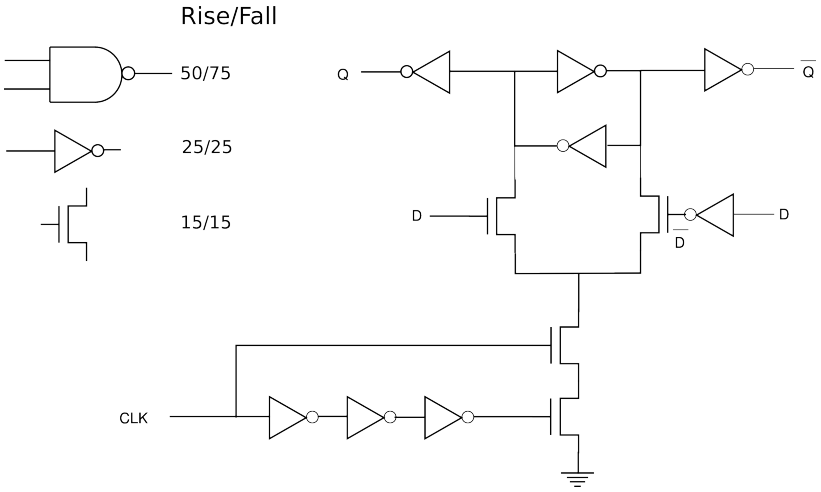
Homework No. 5

Assigned October 16, 2017, due October 23, 2017

1. Find the setup, hold and clock-to-Q times of the flip-flop below; the delays of each component are indicated on the schematic.



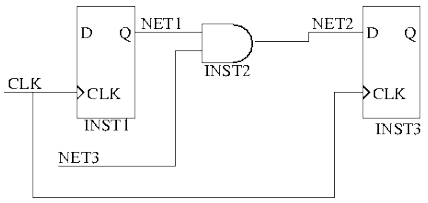
2. (a) Find the setup time, hold time and clock-to-Q delay of the pulse-flip-flop below.

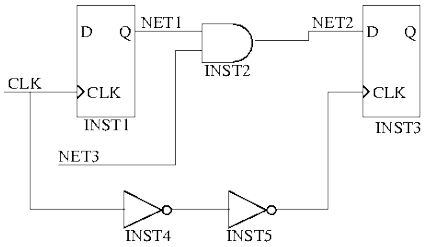


(b) Add one (or more) of the cells shown on the left of the flip-flop in (a) to reduce the setup time to 0 (or less), without changing the circuitry already in place.

(c) Add one (or more) of the cells shown on the left of the flip-flop in (a) to reduce the hold time to 0 (or less), without changing the circuitry already in place.

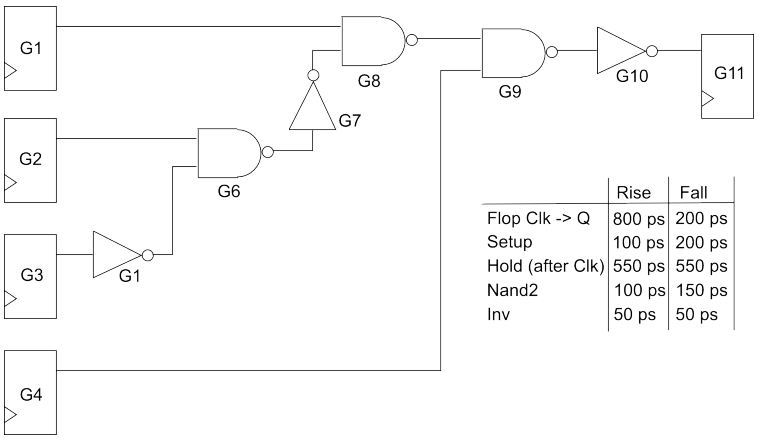
3. Identify if there are any hold time problems from INST1 to INST3 in the two circuits below If there are any, indicate by how much the hold time is violated. Indicate a solution to any hold-time violation.





	Rise	Fall
CLK → Q	500ps	500ps
Flop Hold Time	750ps	750ps
AND gate	300ps	200ps
Inverter	50ps	20ps

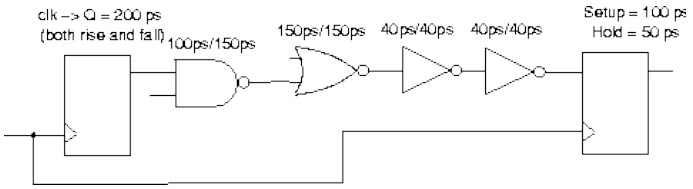
4. (a) Identify if there are any hold time problems from the source flops (G1, G2, G3 and G4) to G11 in the circuit below. If there are any, indicate by how much the hold time is violated and suggest a fix which minimizes the impact on the delay of the circuit. Use the delays from the table below.



	Rise	Fall
Flop Clk -> Q	800 ps	200 ps
Setup	100 ps	200 ps
Hold (after Clk)	550 ps	550 ps
Nand2	100 ps	150 ps
Inv	50 ps	50 ps

(b) What is the maximum frequency of operation after fixing any hold-time violation?

5. (a) What is the maximum frequency at which the following design can operate?



(b) What is the maximum frequency at which the following design can operate?