VLSI Design, Fall 2017

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Homework No. 6

Assigned October 23, 2015, due October 30, 2017

1. Problem 9.31 from the Exercises for Chapter 9 (page 373).

2. Problem 9.32 from the Exercises for Chapter 9 (page 373).

3. Problem 9.33 from the Exercises for Chapter 9 (page 373).

4. Problem 9.35 from the Exercises for Chapter 9 (page 373).

5. Problem 9.37 from the Exercises for Chapter 9 (page 373).

6. Design the carry function for a full adder (C = AB + AC + BC) using standard Domino CMOS Logic, with the restriction that there are only three transistors (including clocking transistors) from any output node to ground.

7. Design a transistor level circuit realization of the following function using N-P Dynamic Logic. Assume you have two non-overlapping clocks ϕ and $\overline{\phi}$ and the restriction that you cannot use more than four transistors in series (including clocking transistors) in any path from an internal node to power or ground. You have only the uncomplemented inputs A, B, C, D, E, F, G, H available.

$Z = (A \cdot B + C \cdot D) \cdot (E \cdot F \cdot G + H)$

HINT: Realize two sub-functions using N-networks and feed the outputs of these sub-functions as inputs to a P-network.