Lecture 19:
Circuit Pitfalls, Tip & Tricks

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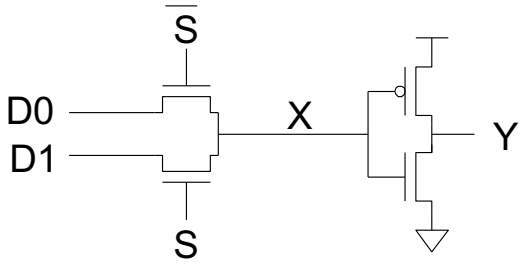
Agenda

- Circuit Pitfalls
- Circuit Tips & Tricks
- Circuit Robustness
  - Noise
  - Reliability

Bad Circuit 1

- **Circuit**
  - 2:1 multiplexer



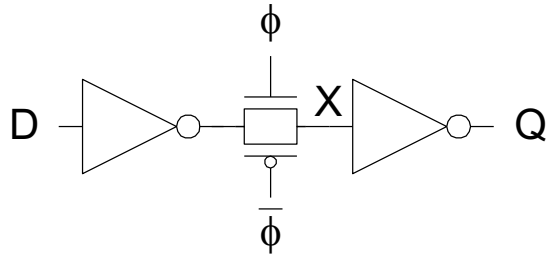
- **Principle: Threshold drop**
  - X never rises above VDD-Vt
  - Vt is raised by the body effect
  - The threshold drop is most serious as Vt becomes a greater fraction of VDD

- **Solution: Use transmission gates, not pass transistors**

- **Symptom**
  - Mux works when selected D is 0 but not 1
  - Or fails at low VDD
  - Or fails in SFSF corner

Bad Circuit 2

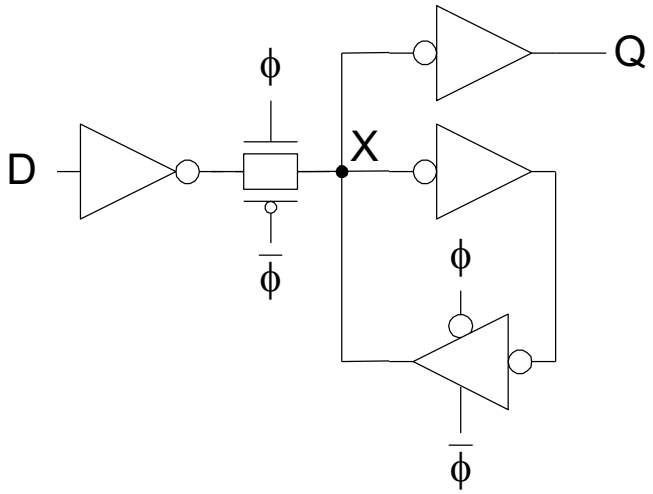
- **Circuit**
  - Latch



- **Symptom**
  - Load a 0 into Q
  - Set f = 0
  - Eventually Q spontaneously flips to 1

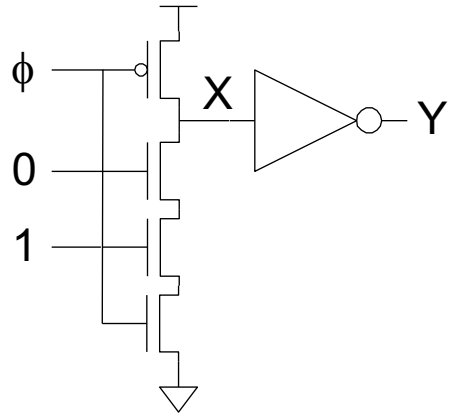
- **Principle: Leakage**
  - X is a dynamic node holding value as charge on the node
  - Eventually subthreshold leakage may disturb charge

- **Solution: Refresh node with feedback**
  - Or periodically refresh node (requires fast clock, not practical processes with big leakage)



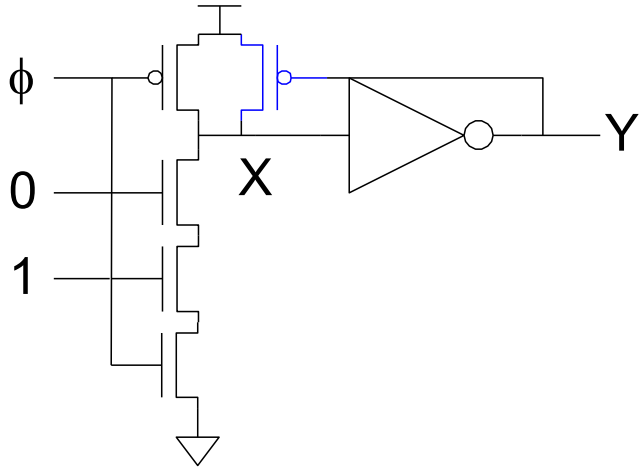
Bad Circuit 3

- **Circuit**
  - Domino AND gate



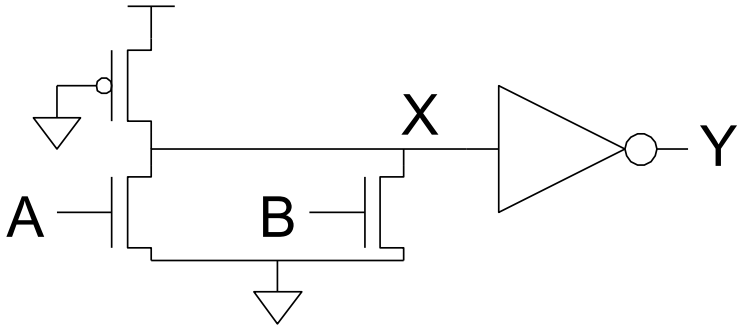
- **Symptom**
  - Precharge gate (Y=0)
  - Then evaluate
  - Eventually Y spontaneously flips to 1

- **Principle: Leakage**
  - X is a dynamic node holding value as charge on the node
  - Eventually subthreshold leakage may disturb charge
- **Solution: Keeper**



Bad Circuit 4

- **Circuit**
  - Pseudo-nMOS OR



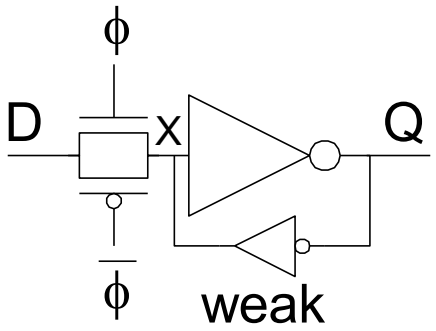
- **Principle: Ratio Failure**
  - nMOS and pMOS fight each other.
  - If the pMOS is too strong, nMOS cannot pull X low enough.

- **Solution: Check that ratio is satisfied in all corners**

- **Symptom**
  - When only one input is true, Y = 0
  - Perhaps only happens in SF corner

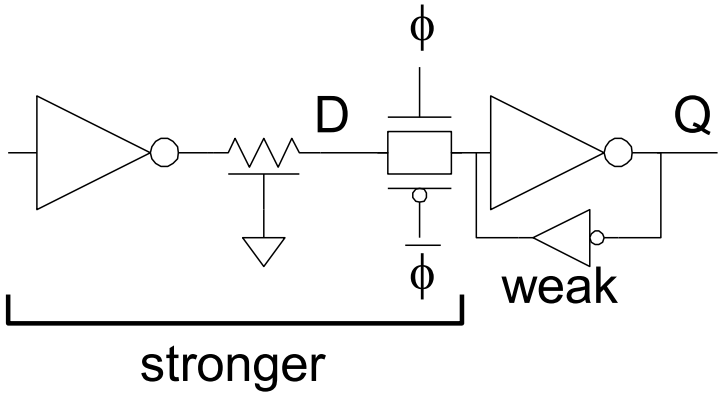
Bad Circuit 5

- **Circuit**
  - Latch



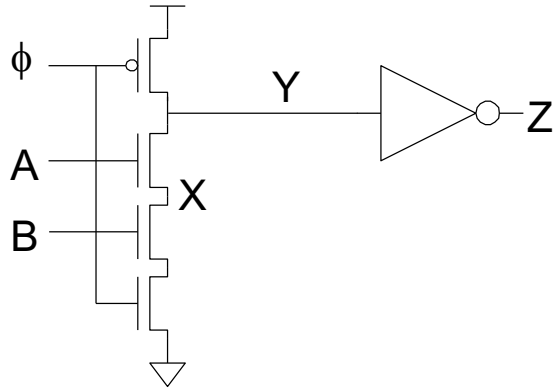
- **Symptom**
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.

- **Principle: Ratio Failure (again)**
  - Series resistance of D driver, wire resistance, and pass-gate must be much less than weak feedback inverter.
- **Solutions: Check relative strengths**
  - Avoid un-buffered diffusion inputs where driver is unknown



Bad Circuit 6

- **Circuit**
  - Domino AND gate



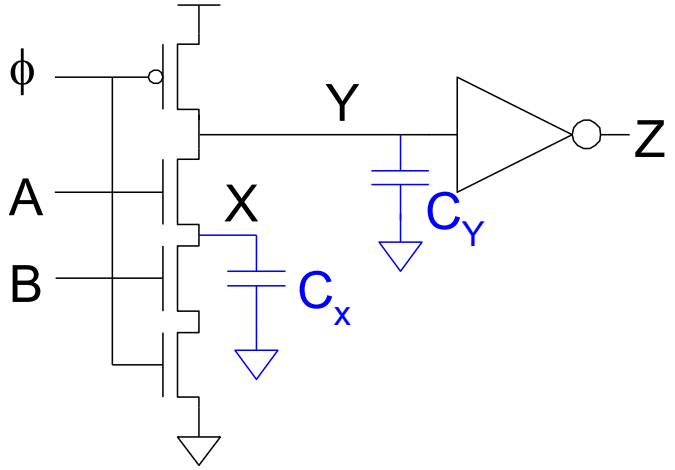
- **Principle: Charge Sharing**
  - If X was low, it shares charge with Y

- **Solutions: Limit charge sharing**
  - Safe if CY >> CX

$$V_x = V_Y = \frac{C_Y}{C_x + C_Y} V_{DD}$$

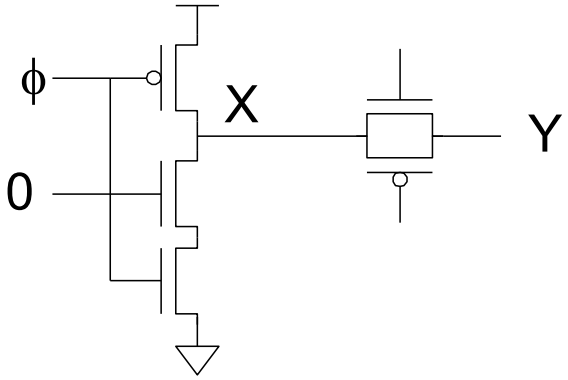
  - Or precharge node X too

- **Symptom**
  - Precharge gate while
  - A = B = 0, so Z = 0
  - Set f = 1
  - A rises
  - Z is observed to sometimes rise



Bad Circuit 7

- **Circuit**
  - Dynamic gate + latch



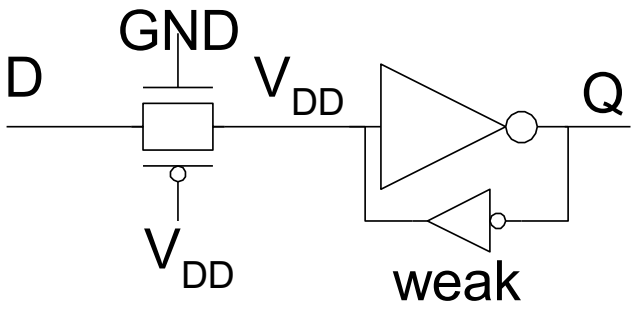
- **Principle: Charge Sharing**
  - If Y was low, it shares charge with X

- **Solution: Buffer dynamic nodes before**
  - driving transmission gate

- **Symptom**
  - Precharge gate while transmission gate latch is opaque
  - Evaluate
  - When latch becomes transparent, X falls

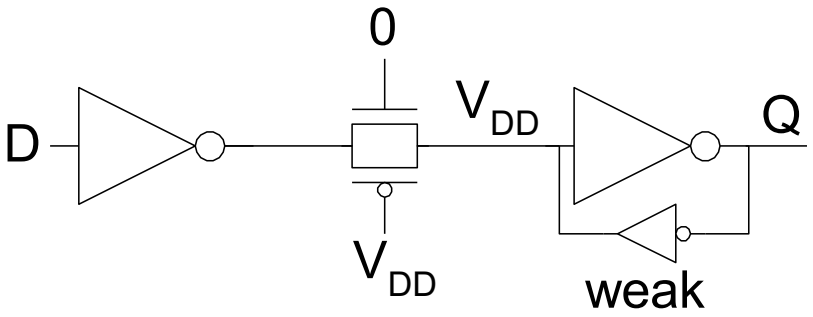
Bad Circuit 8

- **Circuit**
  - Latch



- **Symptom**
  - Q changes while latch is opaque
  - Especially if D comes from a far-away driver

- **Principle: Diffusion Input Noise Sensitivity**
  - If D < -Vt, transmission gate turns on
  - Most likely because of power supply noise or coupling on D

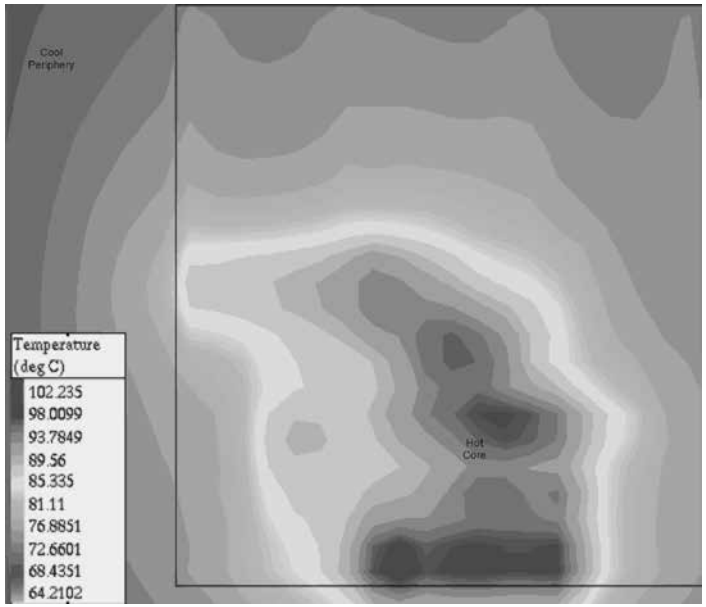


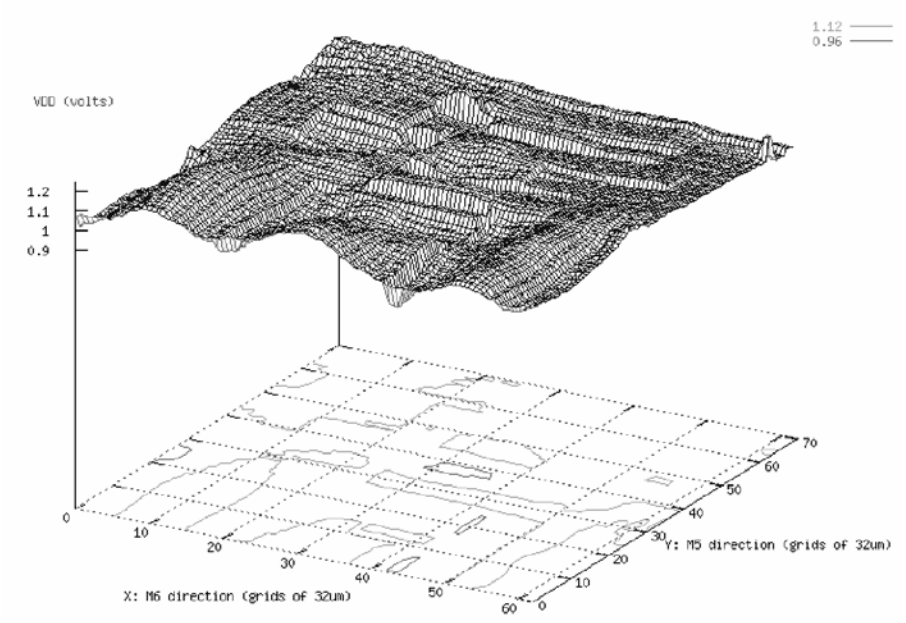
- **Solution: Buffer D locally**

Bad Circuit 9

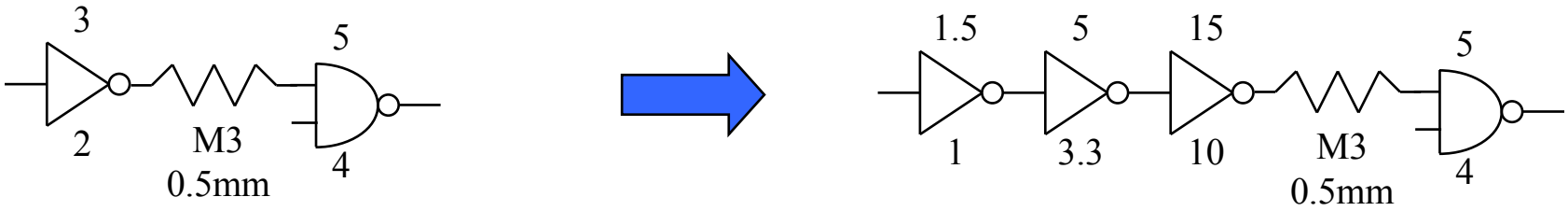
- **Circuit**
  - Anything
- **Symptom**
  - Some gates are slower than expected

Principle: Hot Spots and Power Supply Noise



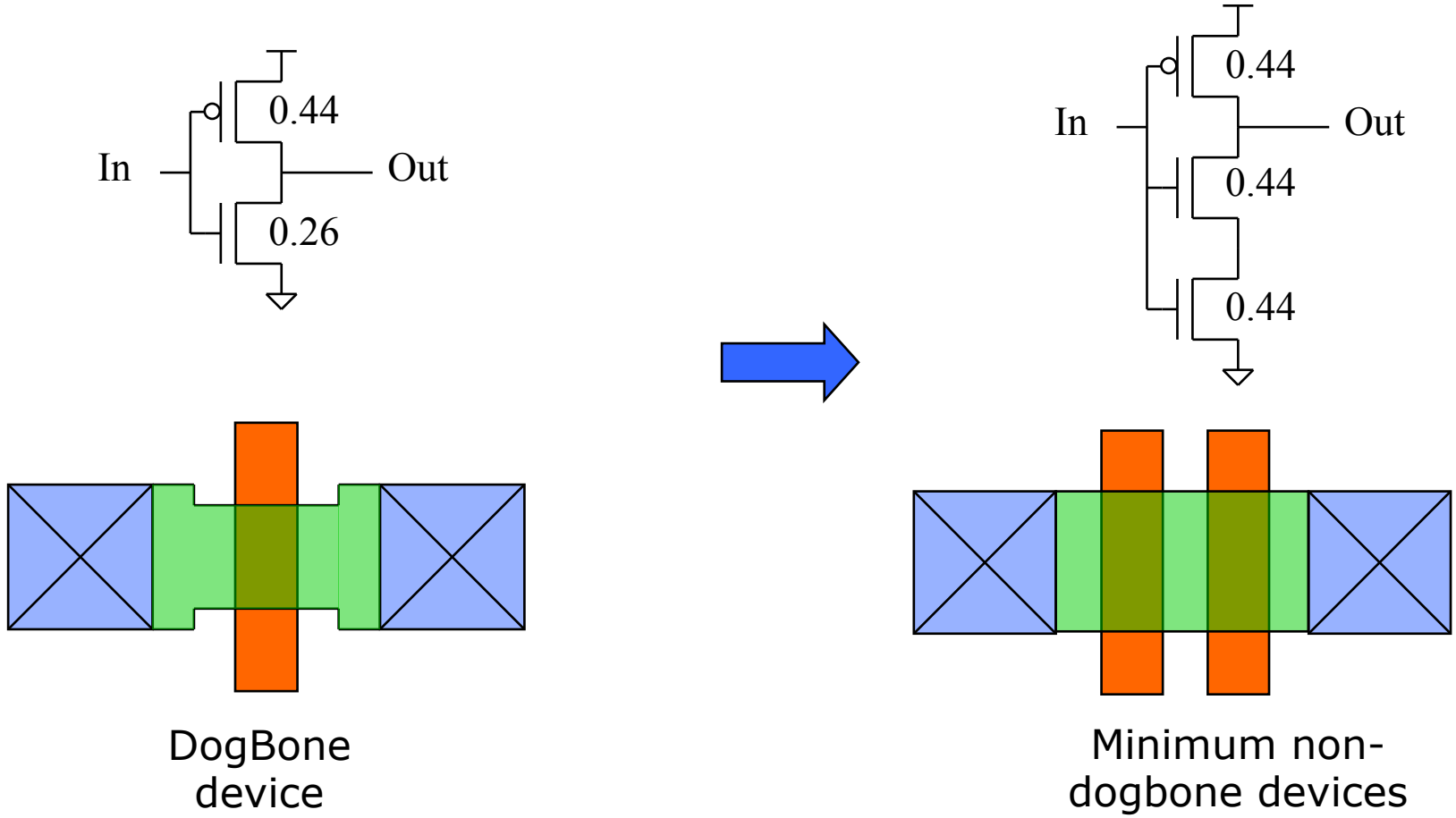


Bad Circuit 10: Extremely Large Gate Delays



Node with very large gate delays are susceptible to noise.

Bad Circuit 11: DogBone Devices in Forward Path

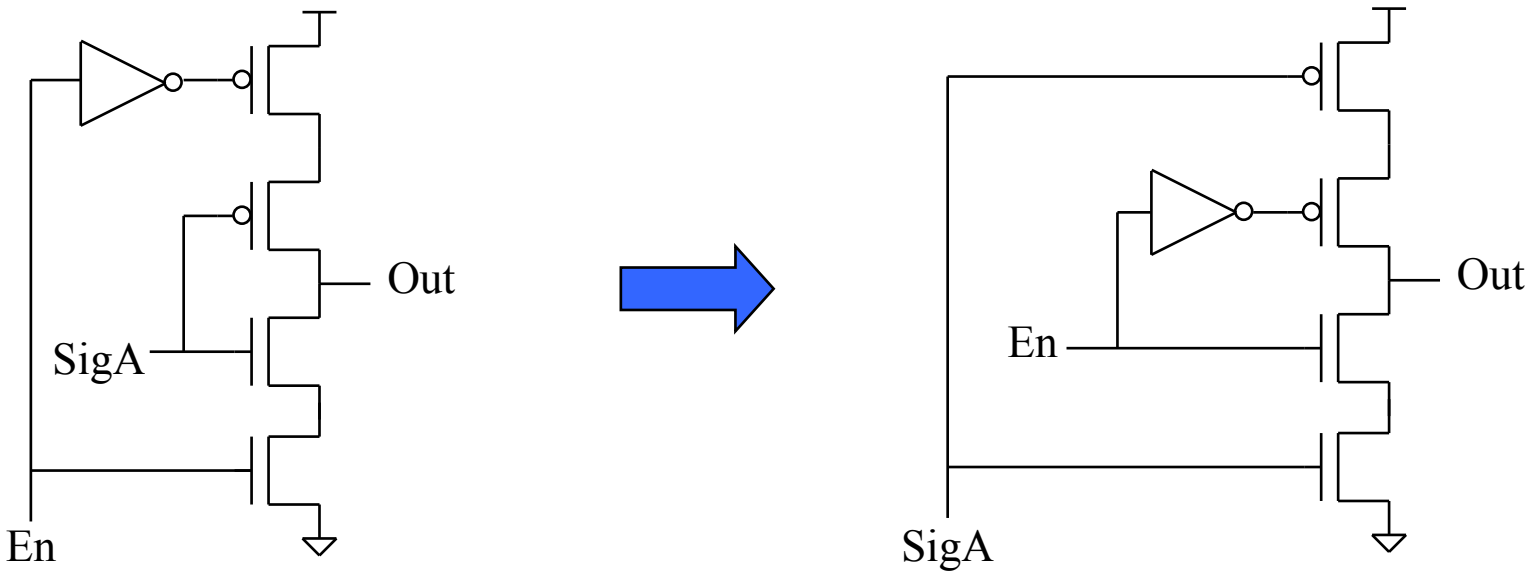


DogBone device

Minimum non-dogbone devices

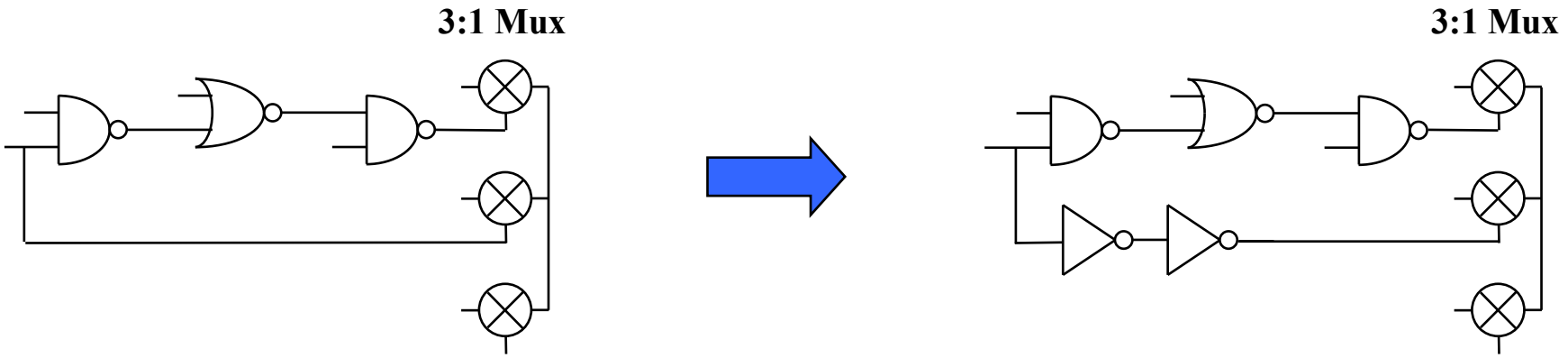
Dog-Bone devices and non-minimum length devices have very large variations in their delay and should only be used for keepers.

Bad Circuit 12: Charge Sharing Tristates



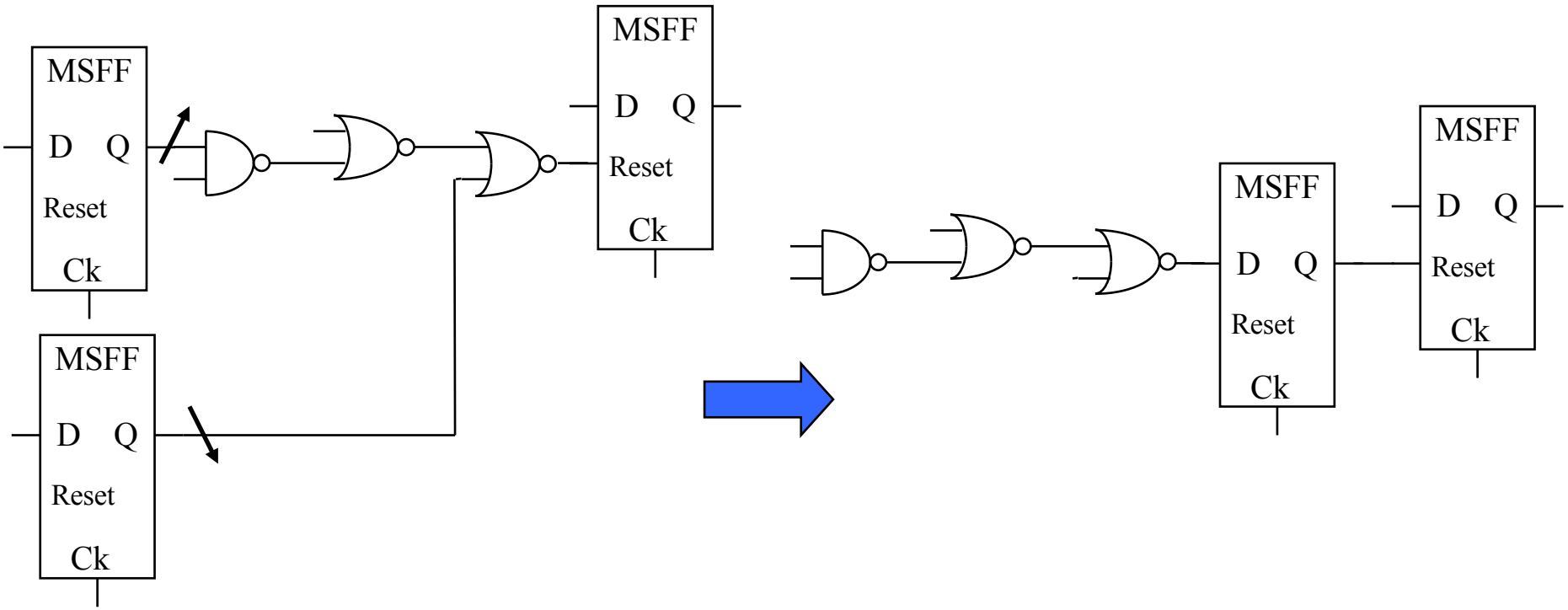
Placing data on the inside of a tristate allows charge sharing as well as extra capacitance on the output.

Bad Circuit 13: Contending Pass Gate Mux Selects



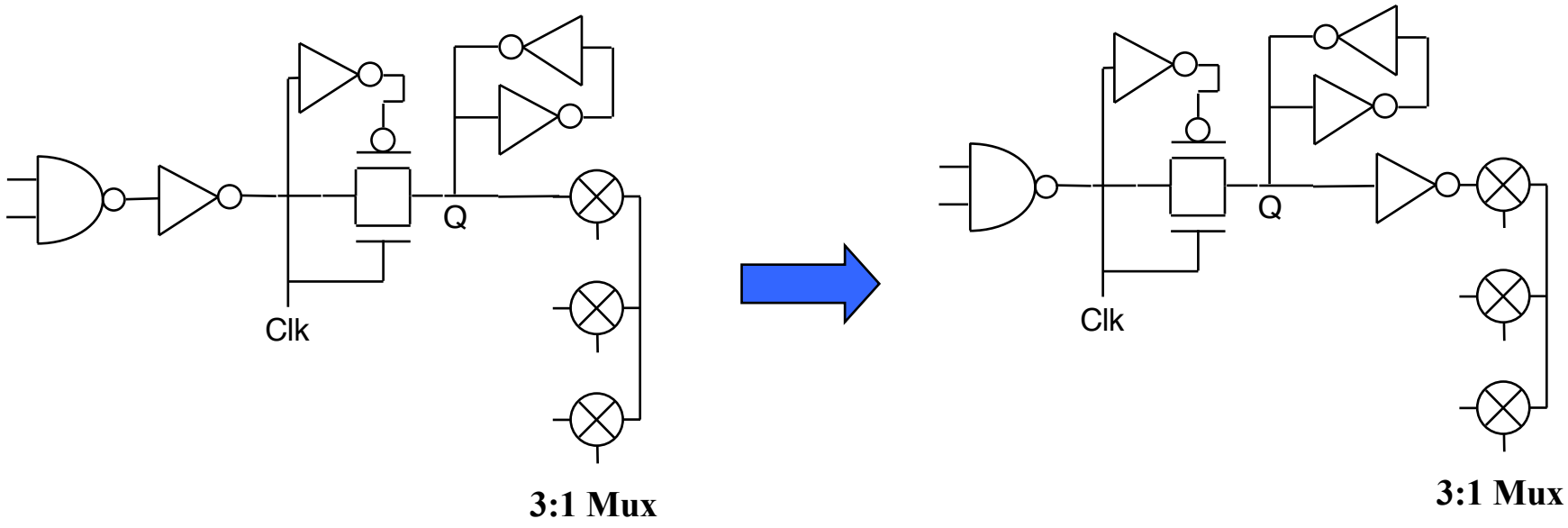
Pass gate mux selects should be designed to all switch at approximately the same time to minimize possible contention.

Bad Circuit 14: Asynchronous Signals Driven from Logic



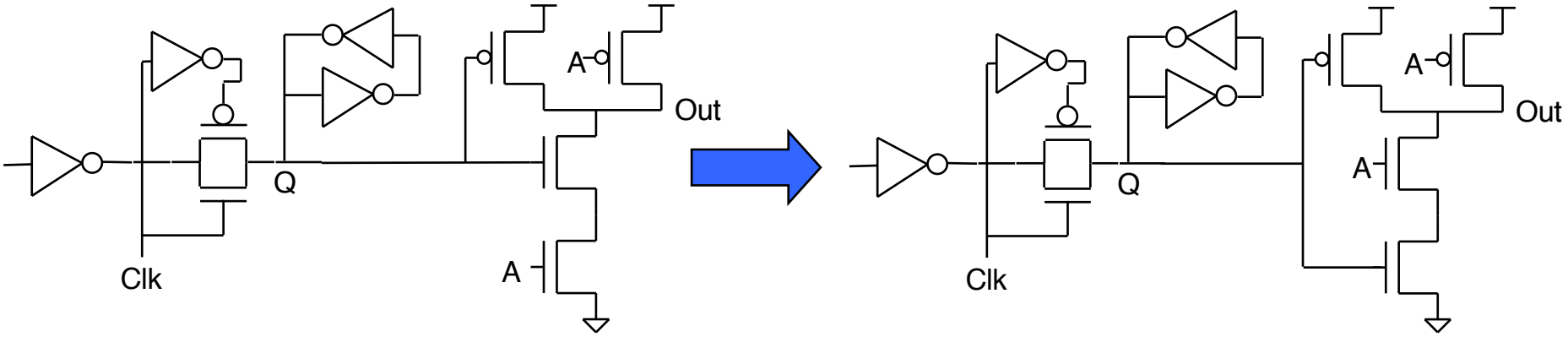
Logic glitches can trigger asynchronous resets improperly.

Bad Circuit 15: Back-writing



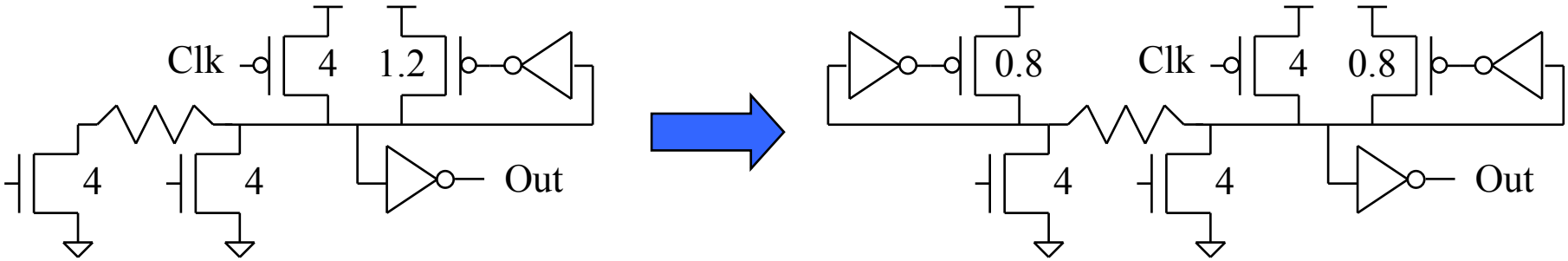
Weakly held nodes driving directly into pass gates can have their data accidentally overwritten.

Bad Circuit 16: Gate-to-Drain Coupling into Weakly Held Node



Weakly held nodes can be disturbed by gate to drain capacitance dramatically increasing gate delay.

Bad Circuit 17: Oversized Keeper in Distributed Domino Gate



Significant RC between the pulldowns can prevent the keeper from being easily overcome.

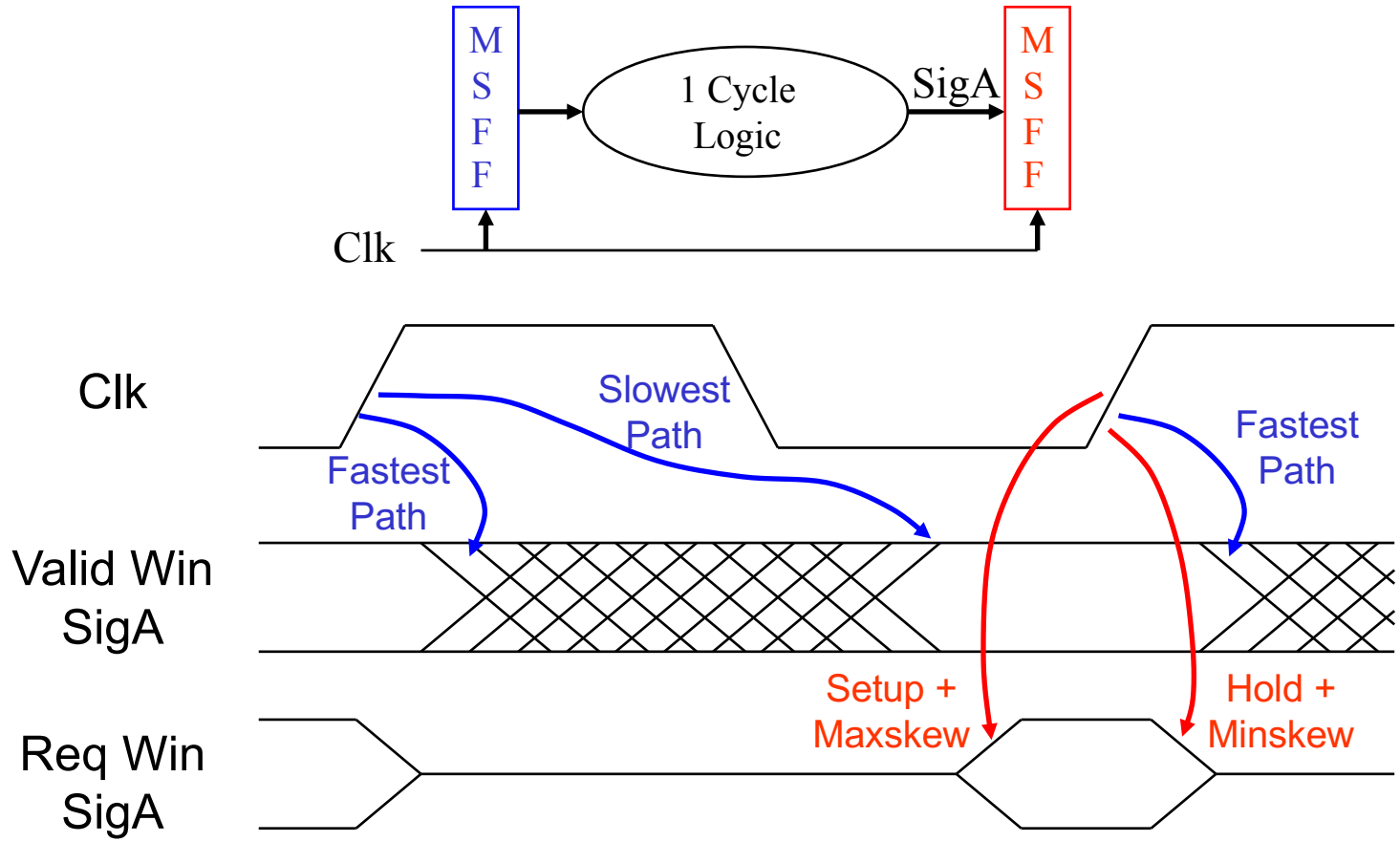
Distributing multiple keepers with the pulldowns can allow for better noise immunity and delay.

Circuit Tips & Tricks

Outline

- **MaxDelay Solutions**
  - Every path has a maximum delay to be captured properly when running at frequency
  - Most MaxDelay solutions make MinDelay worse
- **MinDelay Solutions**
  - Every path has a minimum delay to avoid false capture.
  - Most MinDelay solutions make MaxDelay worse
- **Circuit Pitfalls**
  - Circuits topologies which can cause unexpected failures

Review: Max-Delay & Min-Delay



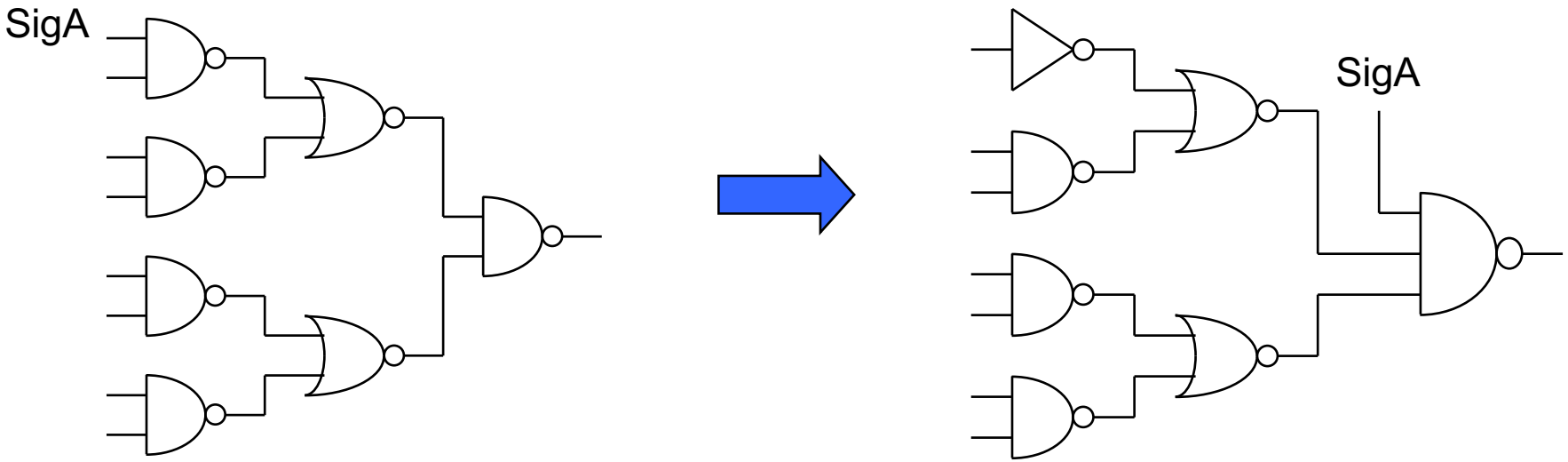
MAXDELAY: **Tmax < Tcycle - Tsetup - Tmaxskew**

MINDELAY: **Tmin > Thold + Tminskew**

Max-Delay Solutions

Use Late Signals Last

Assume the SigA is the critical path

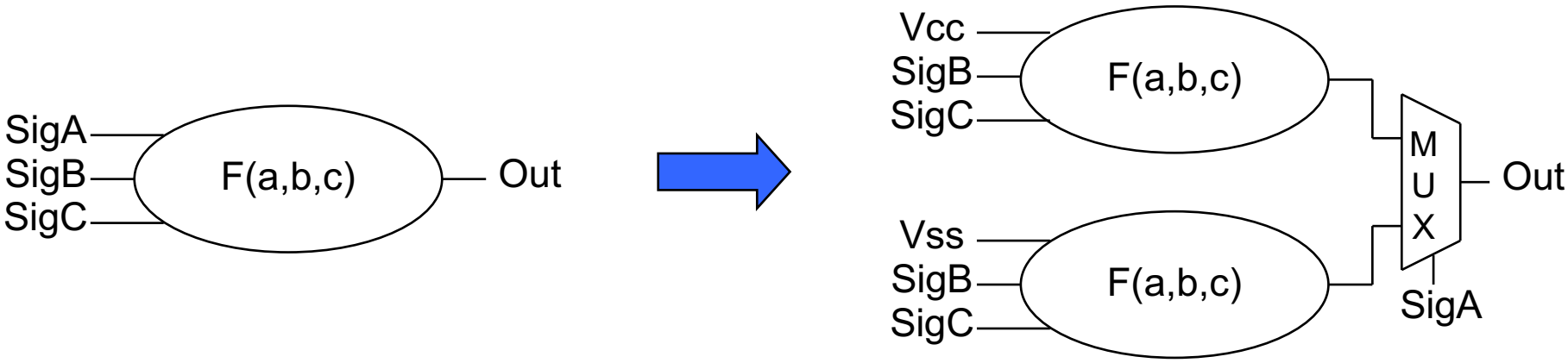


Latest signals should be used in the last stages of logic.

Con: Slows down other paths

Use Late Signals Last (II)

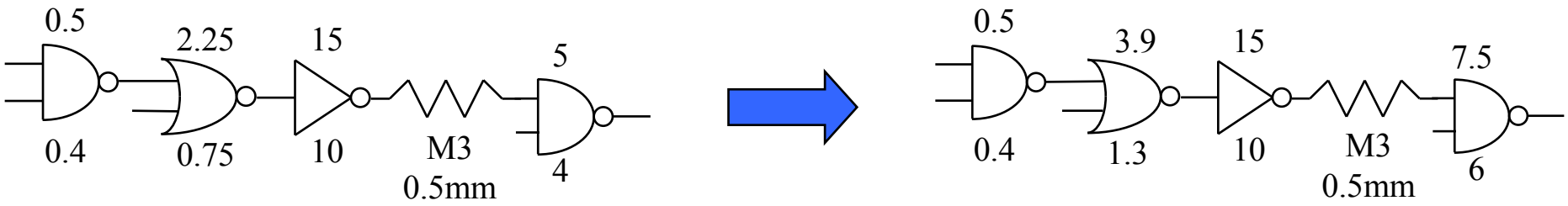
Shannon's Theorem: F(a,b,c) = (a# & F(0,b,c)) | (a & F(1,b,c))



Shannon's theorem allows any logic function to be rewritten to favor a late arriving input.

Con: Slows down other paths
Can dramatically increase area

Size Up Gates

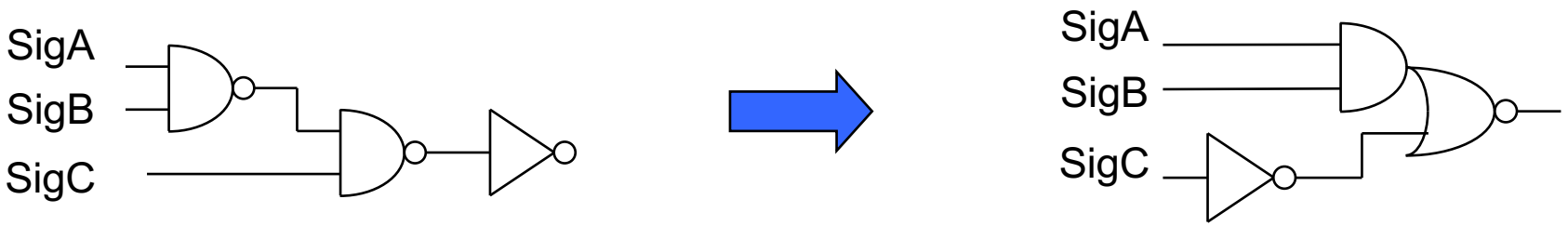


Best gates to size up are those in the critical path having the largest delays and those after long wires.

Con: Increases area
Increases power

Combine Gates

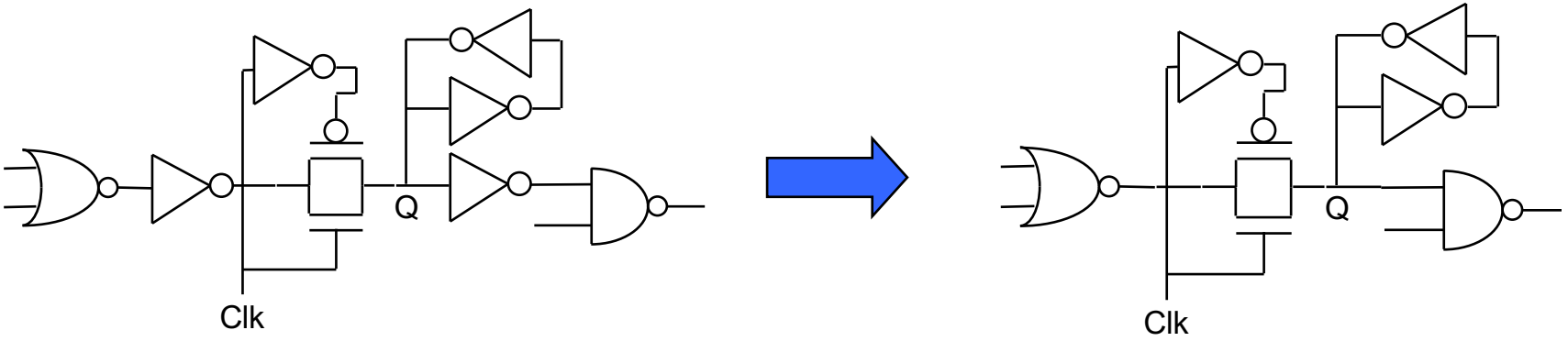
Assume the SigA is the critical path



AOI gates are slow but faster than multiple gates.

Con: Slows down other paths

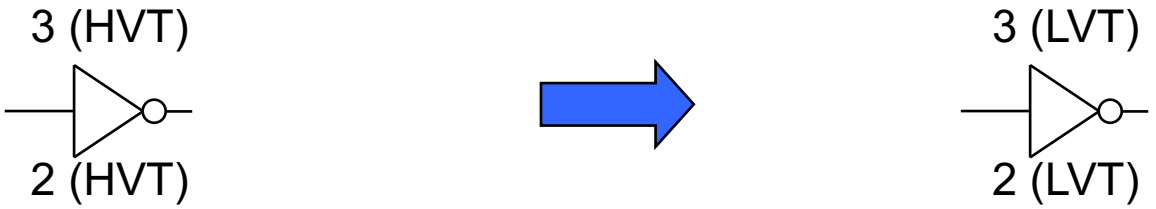
Embed Logic in Latches



Logic gates can be used to drive or receive state nodes.

Con: Increases clock load
Library characterization difficult

Use Low Vt Devices

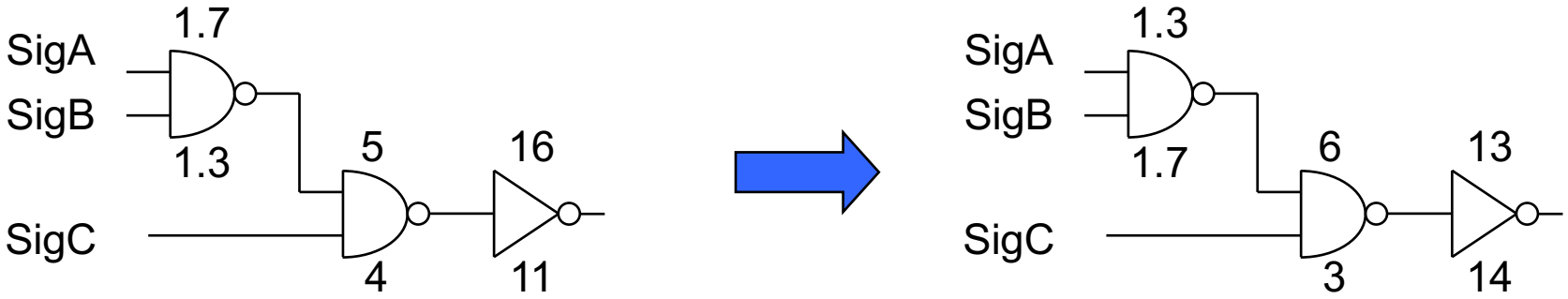


Low threshold devices turn on at lower voltages and provide more current when on.

Con: Increased power due to leakage

Skew P/N Ratio

Assume rise of SigA is the critical path

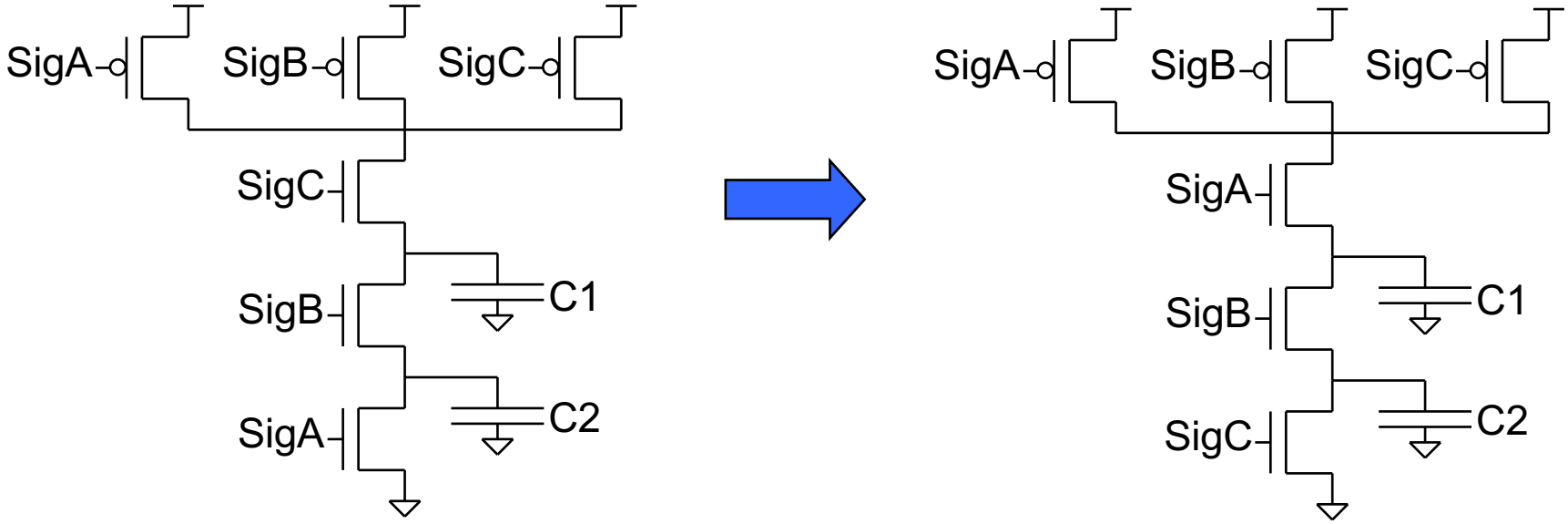


Gate delay can be reduced by 15-25% by skewing P/N ratio

Con: Slows down opposite transition
Reduces noise margins

Late Signals Closest to Output

Assume the SigA is the critical path

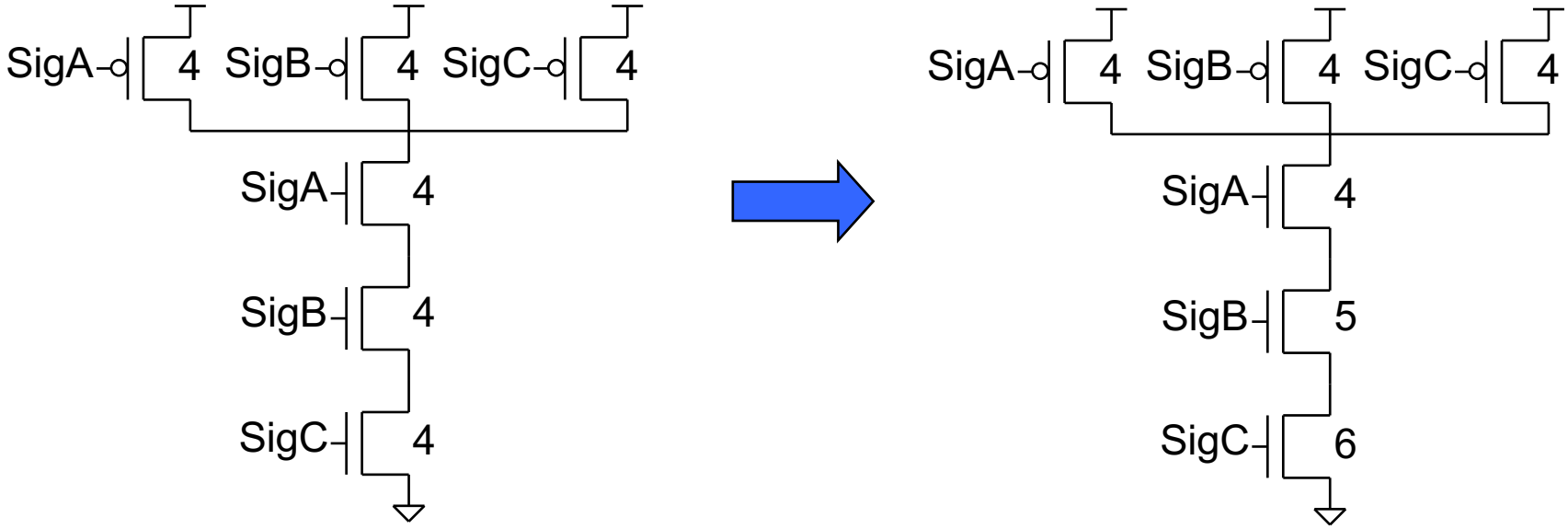


Placing critical path signal at the top of a series stack allows intermediate capacitances to switch early.

Con: Slows down other paths

Taper Series Stacks

Assume rise of SigA is the critical path

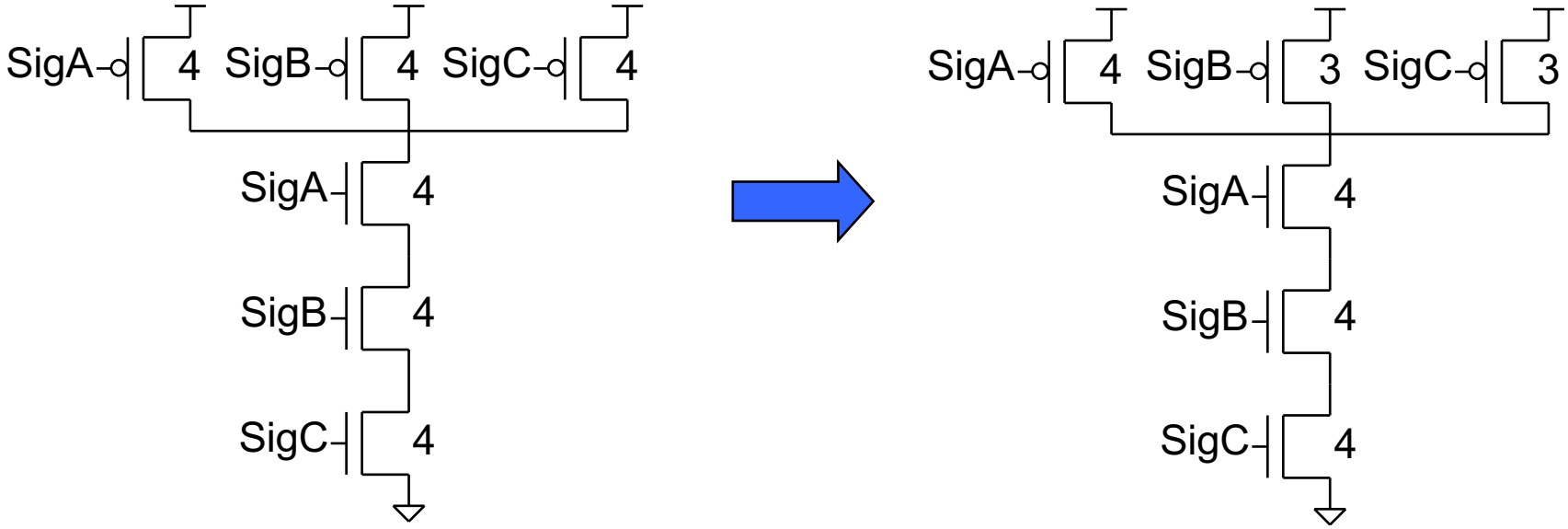


Larger devices at bottom of stack allow more current through top device.

Con: Slows down other paths
Less regular layout

Size Down Parallel Devices

Assume fall of SigA is the critical path

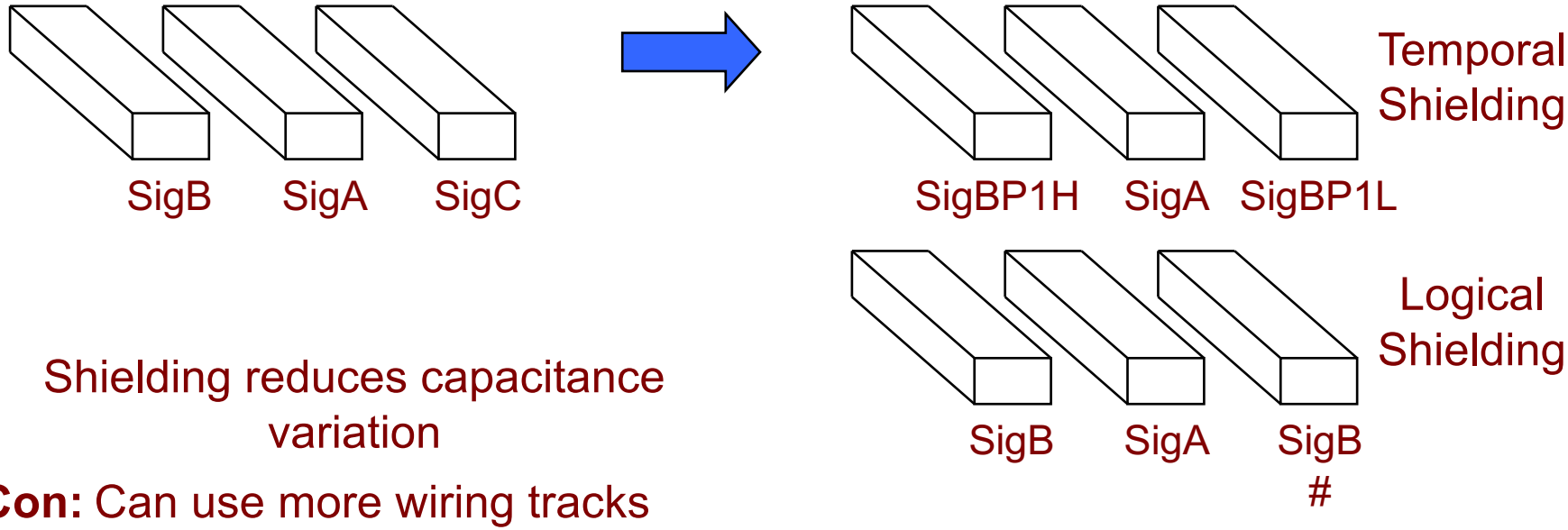


Larger devices at bottom of stack allow more current through top device.

Con: Slows down other paths
Less regular layout

Shield Critical Signals

Assume the SigA is the critical path



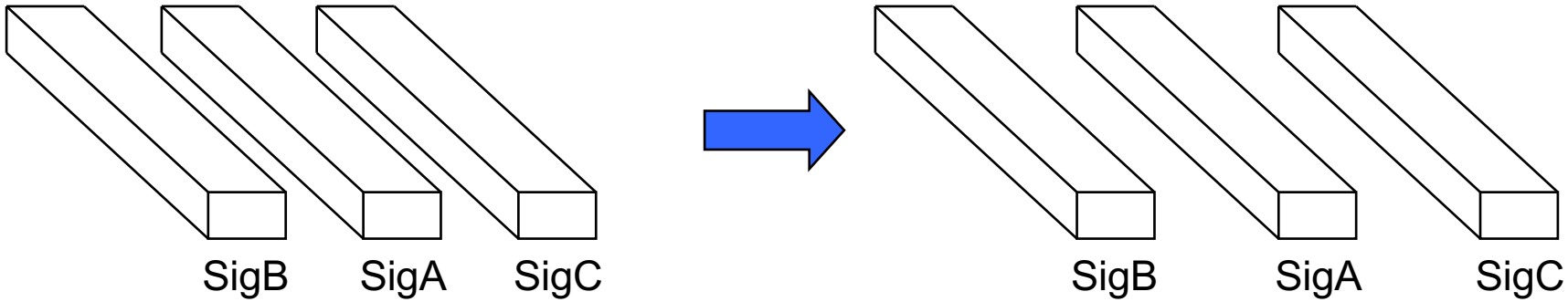
Shielding reduces capacitance variation

Con: Can use more wiring tracks

Shielding simultaneously improves maxdelay and mindelay.

Increase Wire Spacing

Assume the SigA is the critical path

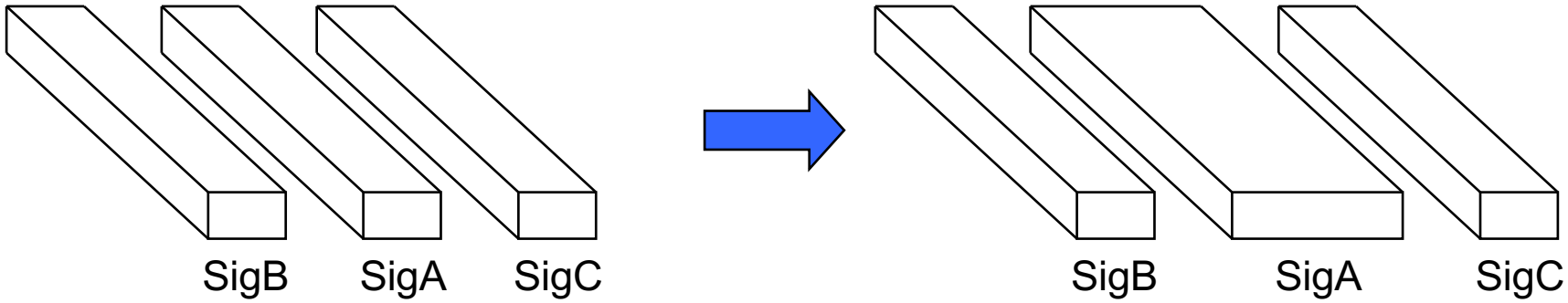


Increased wire spacing reduces total wire capacitance.

Con: Uses more wiring tracks

Increase Wire Width

Assume the SigA is the critical path



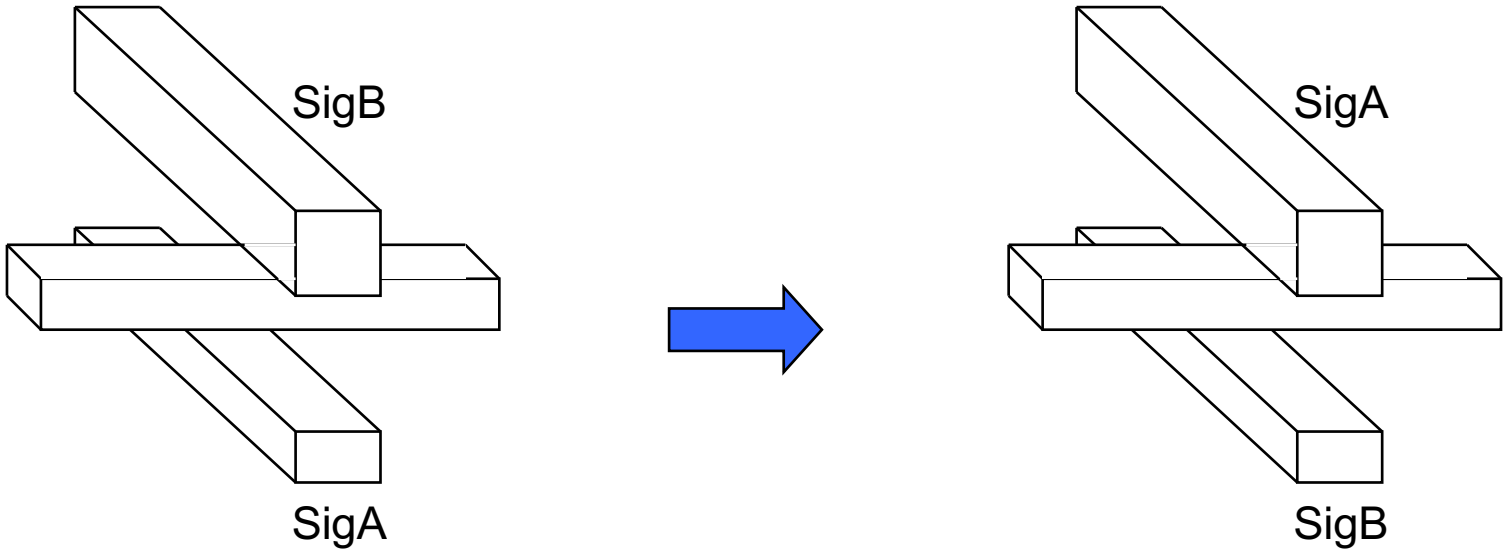
When wire RC is significant, increasing wire width can reduce delay.

Con: Uses more wiring tracks
Increases wire capacitance

A tapered wire may give the best delay but is a nuisance to layout.

Use Higher Metal Layer

Assume the SigA is the critical path

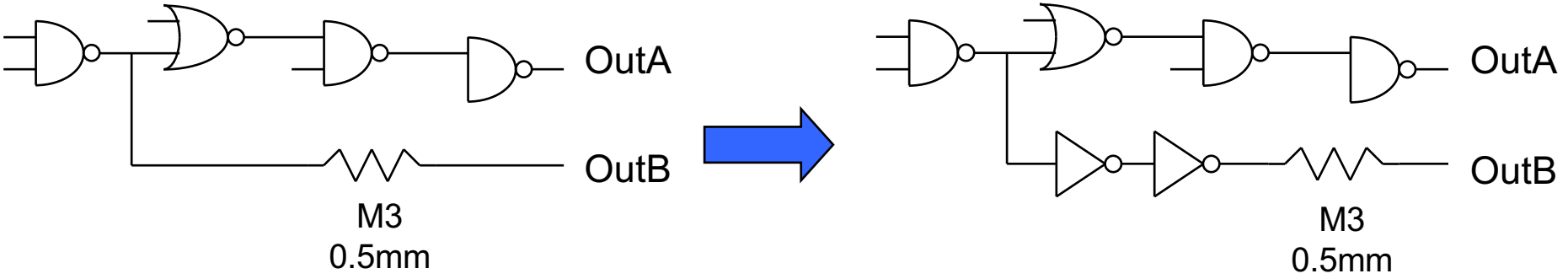


Because higher level metals are thicker they have less resistance even at the same width.

Con: Takes tracks from global routes

Buffer Side Loads

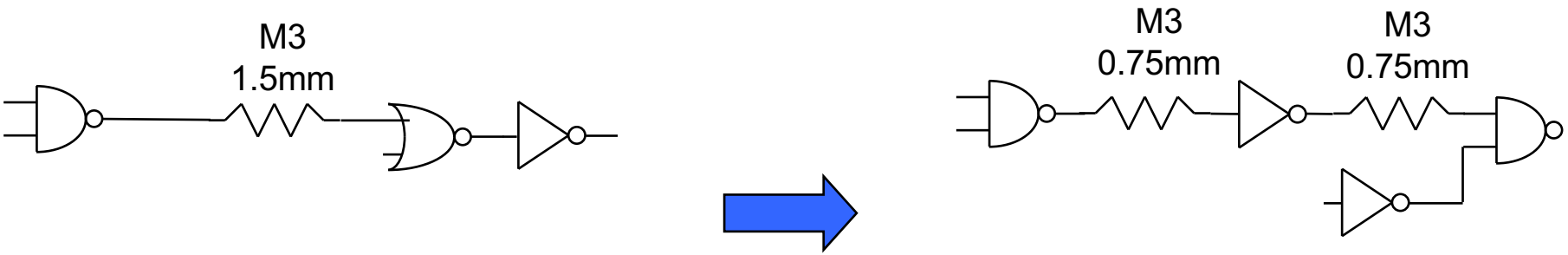
Assume OutB is not on critical path



Prevent the critical path from being slowed by large loads not on the critical path.

Con: Slows down other paths
Increases area

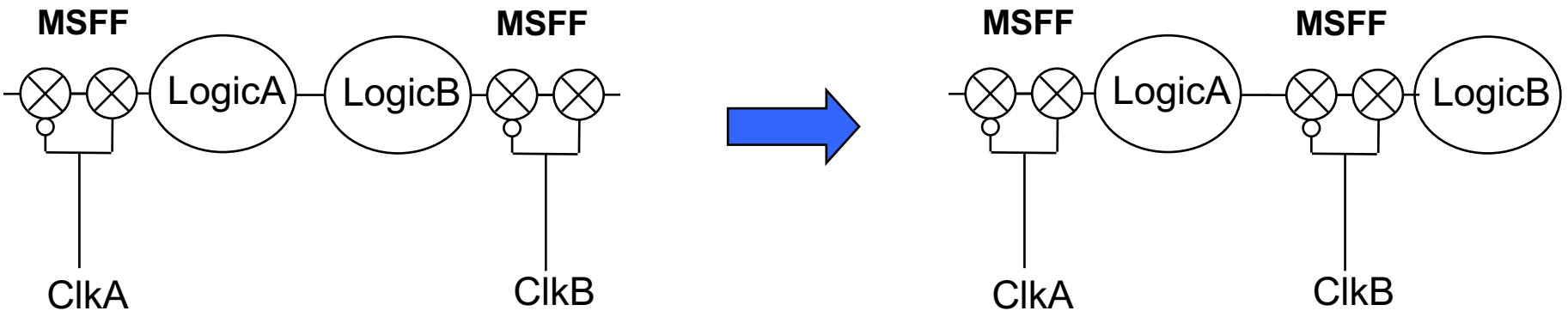
Add Repeaters



For routes longer than 1mm a repeater than reduce the total delay.

Con: Increases area

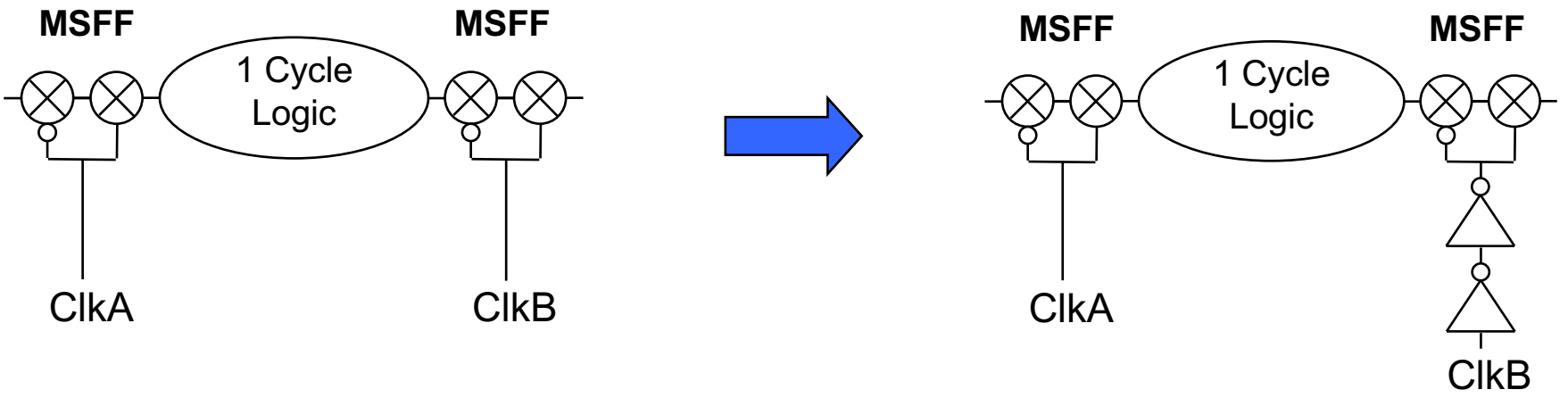
Move Logic Across Sequentials



Cycles with maxdelay margin can be used to improve help other cycles

Con: Increases delay in other cycle
May increase clock load

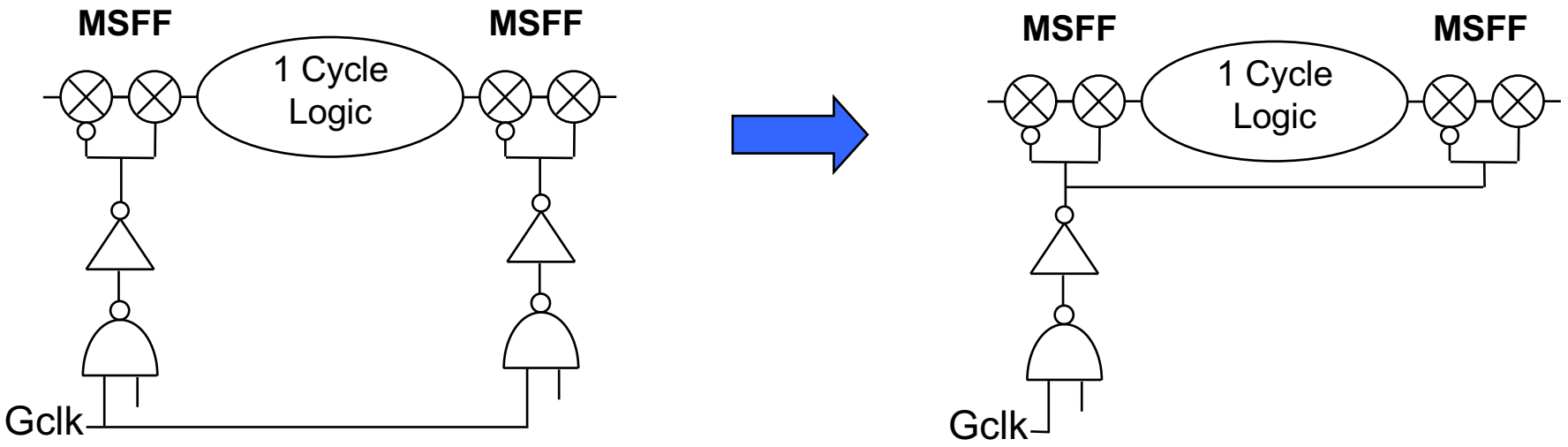
Delay Receiver Clock



Delayed clocks allow logic to be divided into unequal pipestages.

Con: Mindelay significantly worse
Reduces time in next pipestage
Increases clock skew

Closer Common Point for Clocks

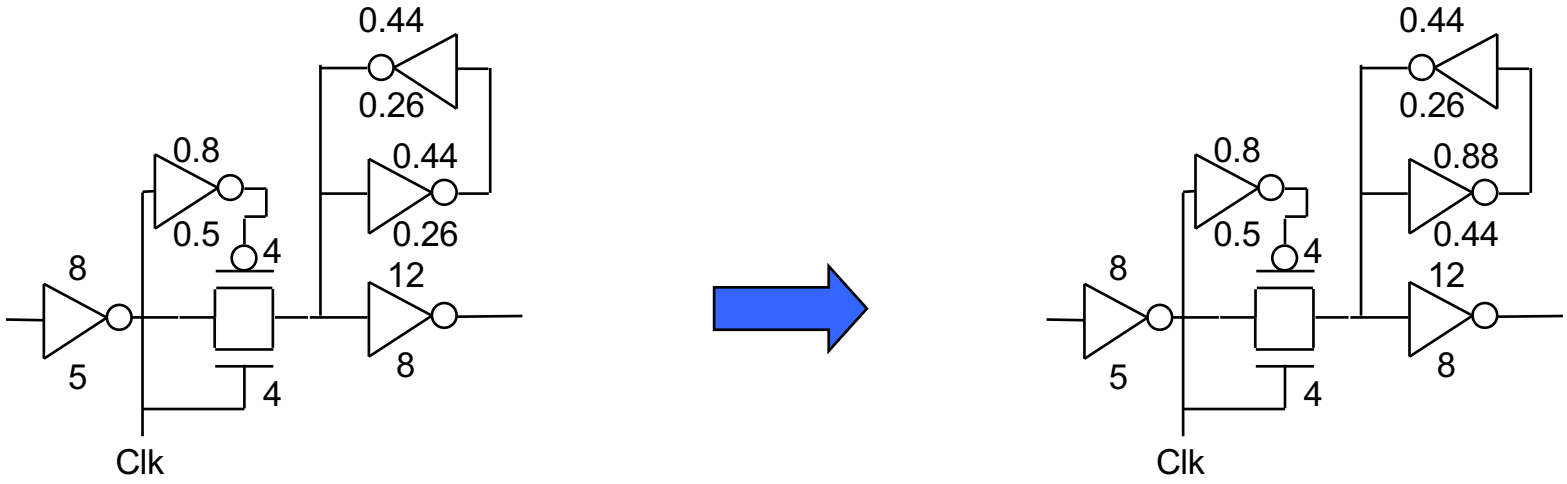


A closer common point reduces clock skew.

Con: Reduces opportunities for clock gating
May increase global clock load

Reduced clock skew improves maxdelay and mindelay.

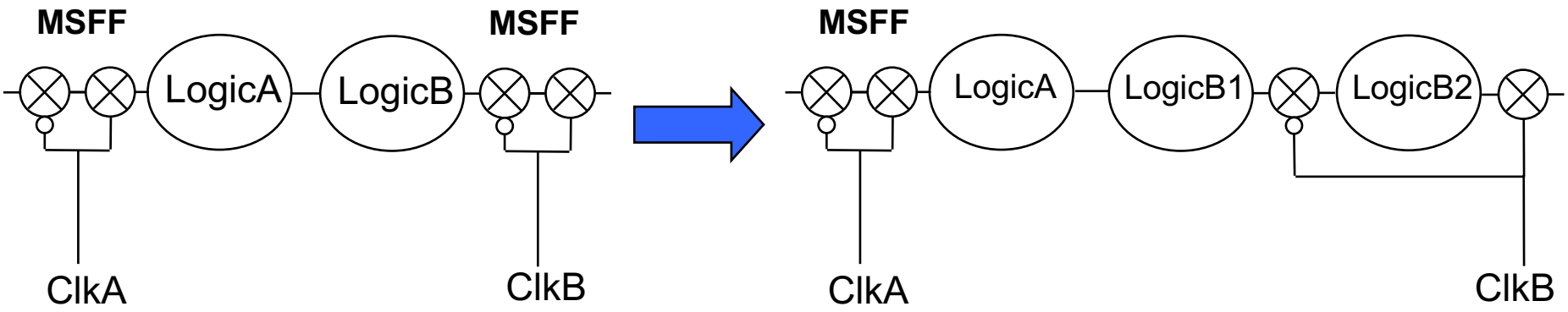
Speed Up Latch Feedback



Faster inverter in feedback loop can reduce latch setup time.

Con: Very small improvement
Eventually start to slow latch node

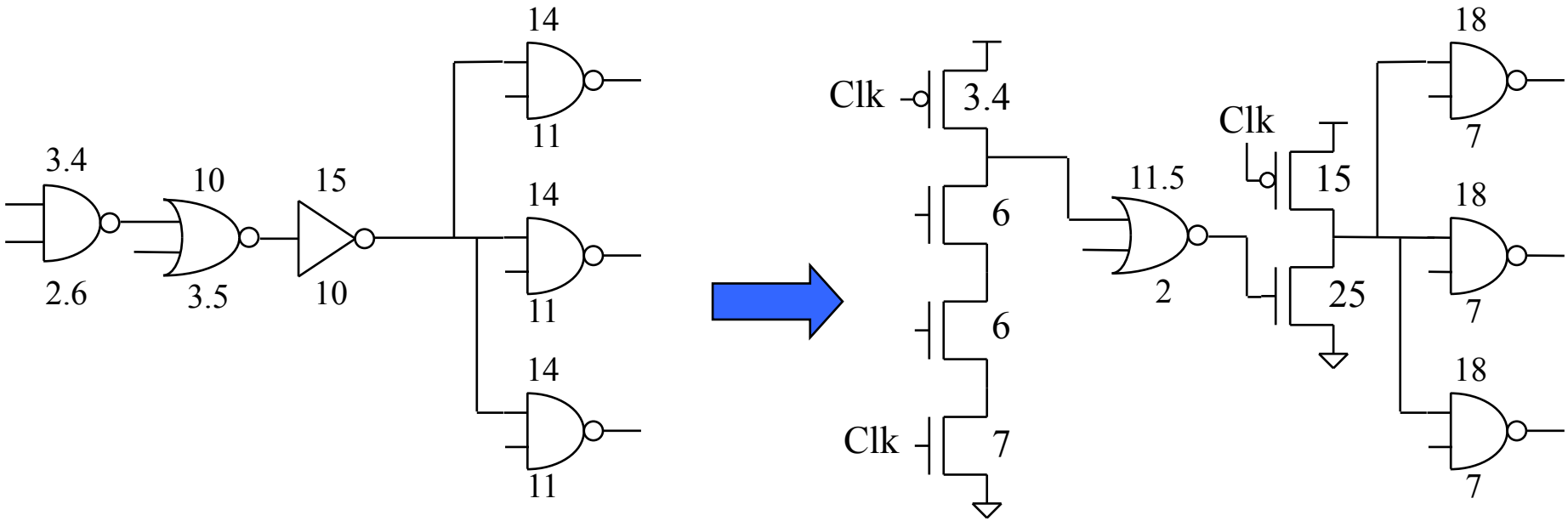
Design for Time Borrowing



Transparent sequentials can allow skew penalties to be avoided by allowing time borrowing.

Con: May increase clock load
More difficult timing analysis

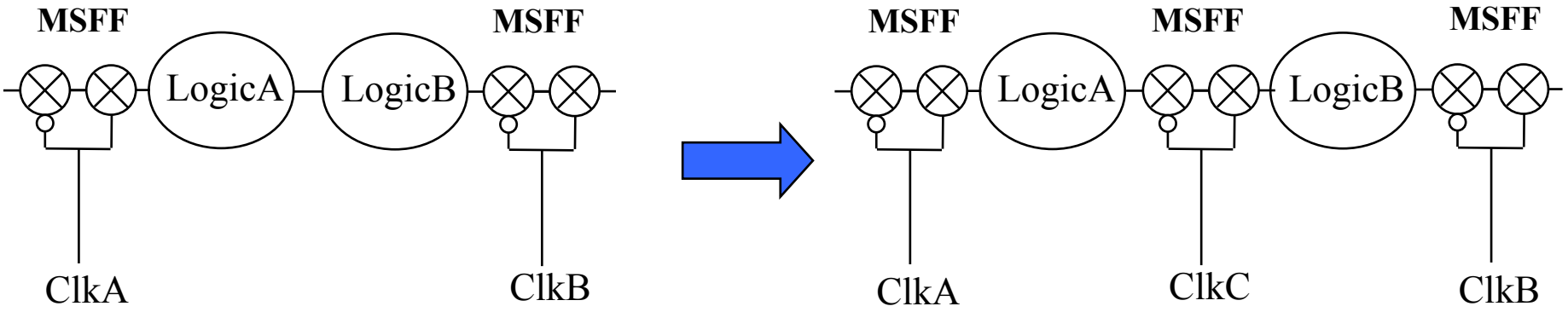
Convert Static Logic to Domino



Domino speeds one transition by skewing the P/N ratio and adds precharge devices to keep the other transition from becoming the critical path.

Con: More design time
More clock load
More power
More sensitive to noise

Add Pipestages

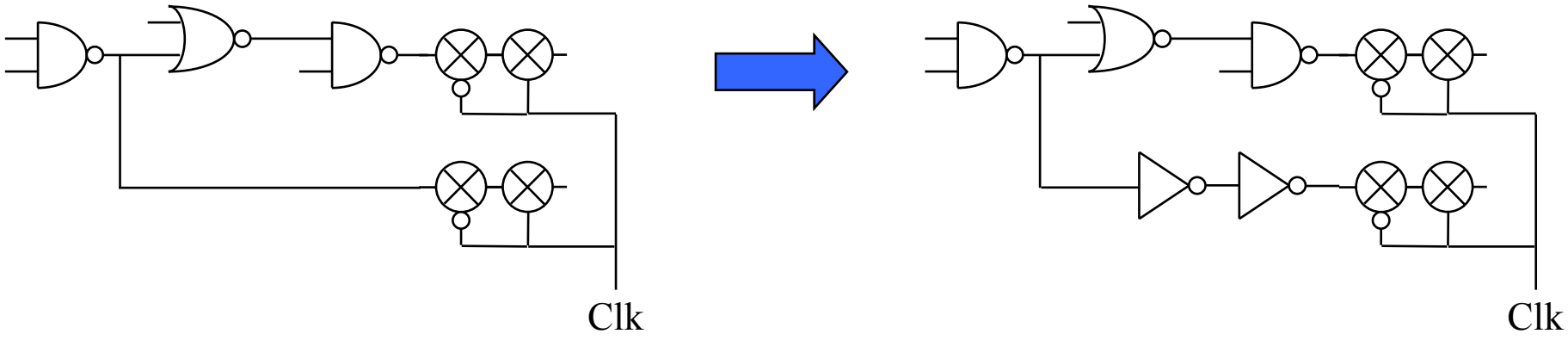


Any path can have its frequency increased by adding pipestages.

Con: Reduces IPC
Increases clock load
Increases area

Min-Delay Solutions

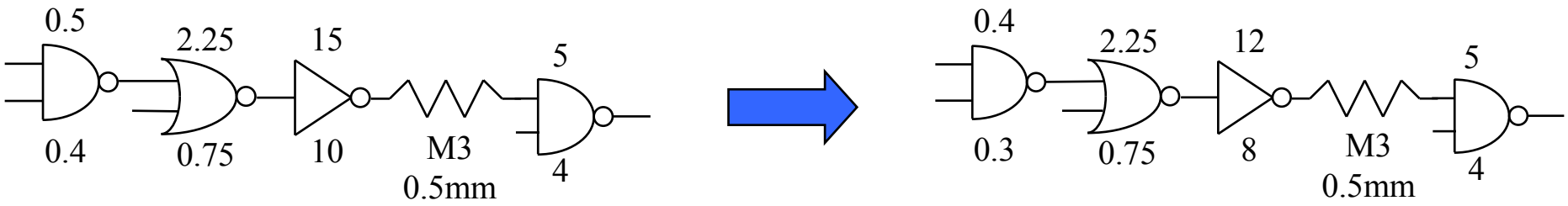
Add Buffers



Shortest paths between sequentials can be made longer by adding buffers.

Con: Increases area

Size Down Gates

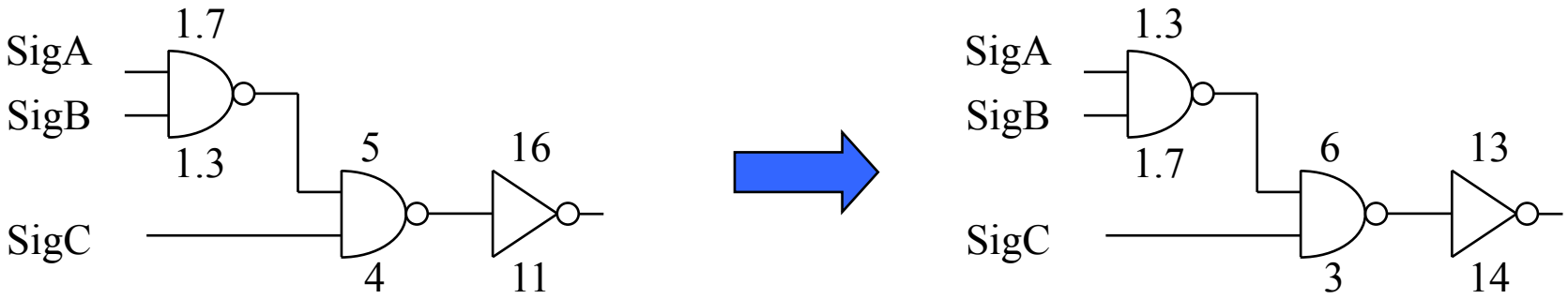


Best gates to size down are those in having the smallest delays and those driving long wires.

Con: Long routes more susceptible to coupling

Skew P/N Ratio

Assume fall of SigA is critical race

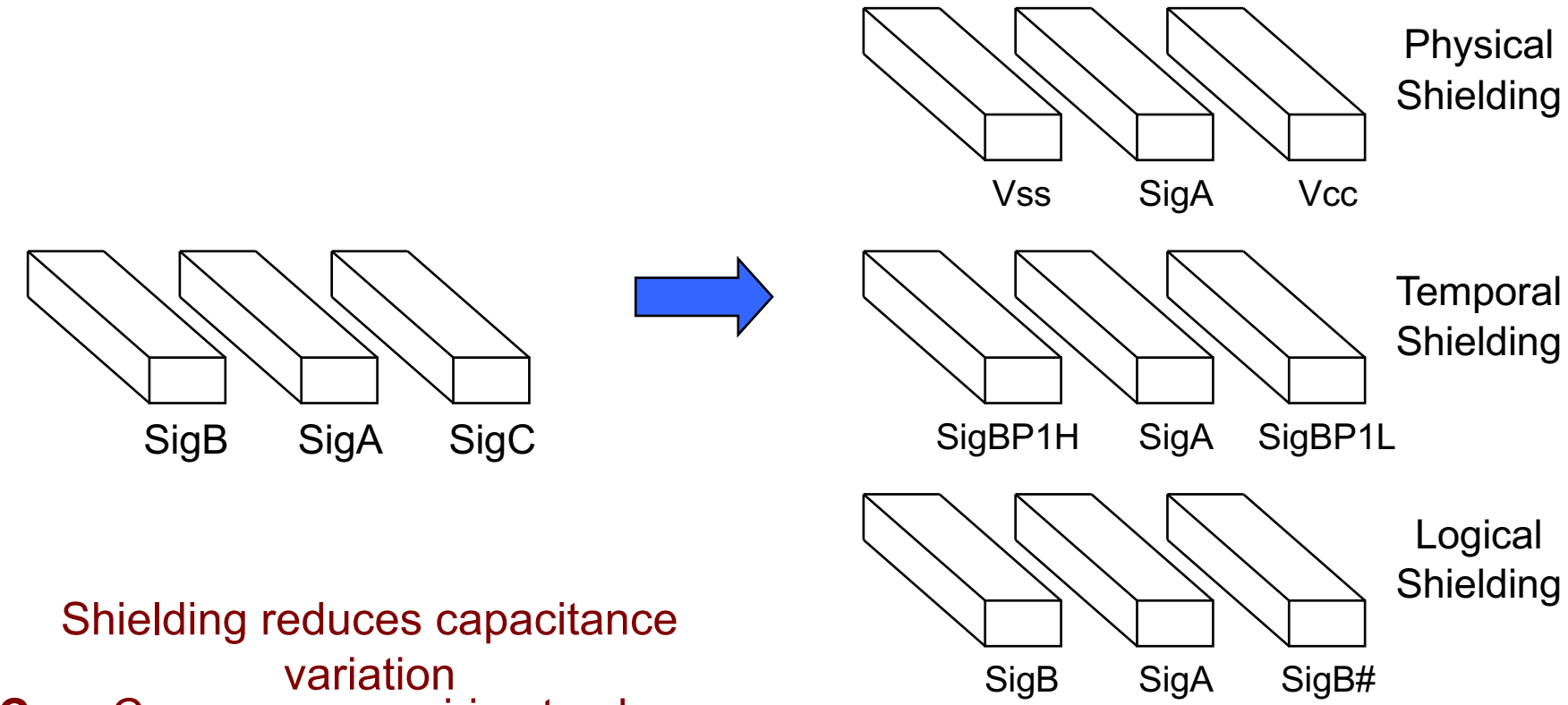


Allows races to be improved for one particular transition.

Con: Reduces noise margin
Speeds up other transition

Shield Critical Signals

Assume the SigA is the critical race

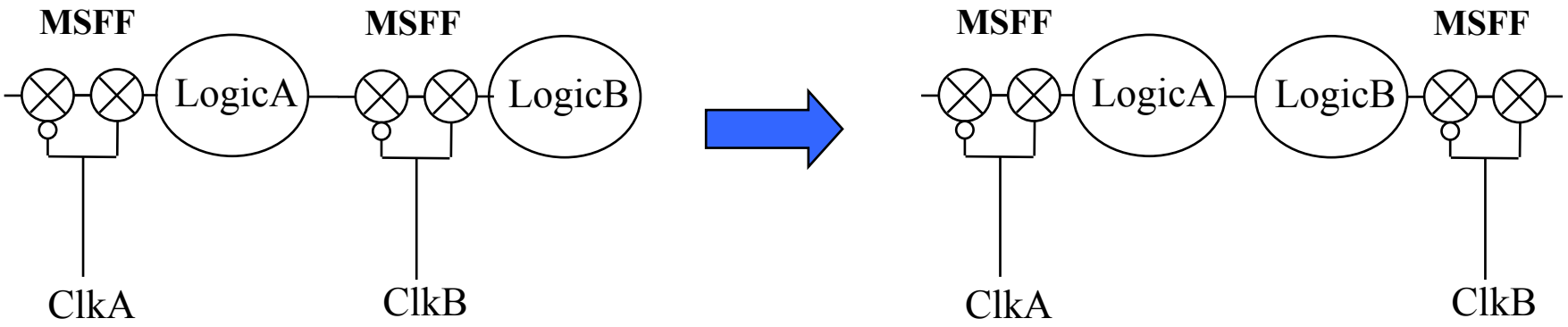


Shielding reduces capacitance variation

Con: Can use more wiring tracks

Shielding simultaneously improves maxdelay and mindelay.

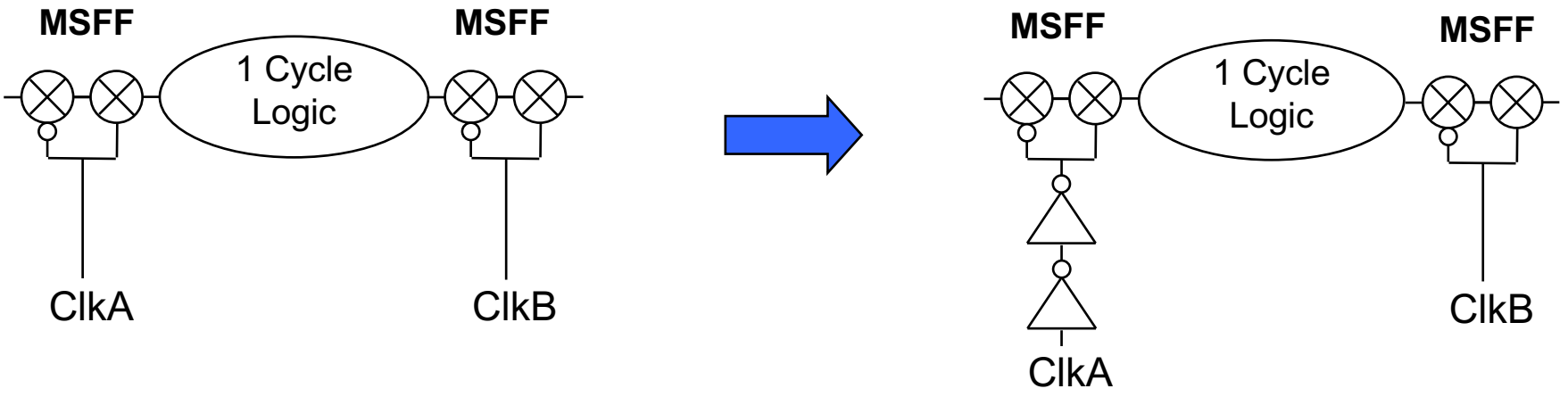
Move Logic Across Sequentials



Careful partitioning of logic between cycles can fix maxdelay and mindelay failures.

Con: May increase clock load

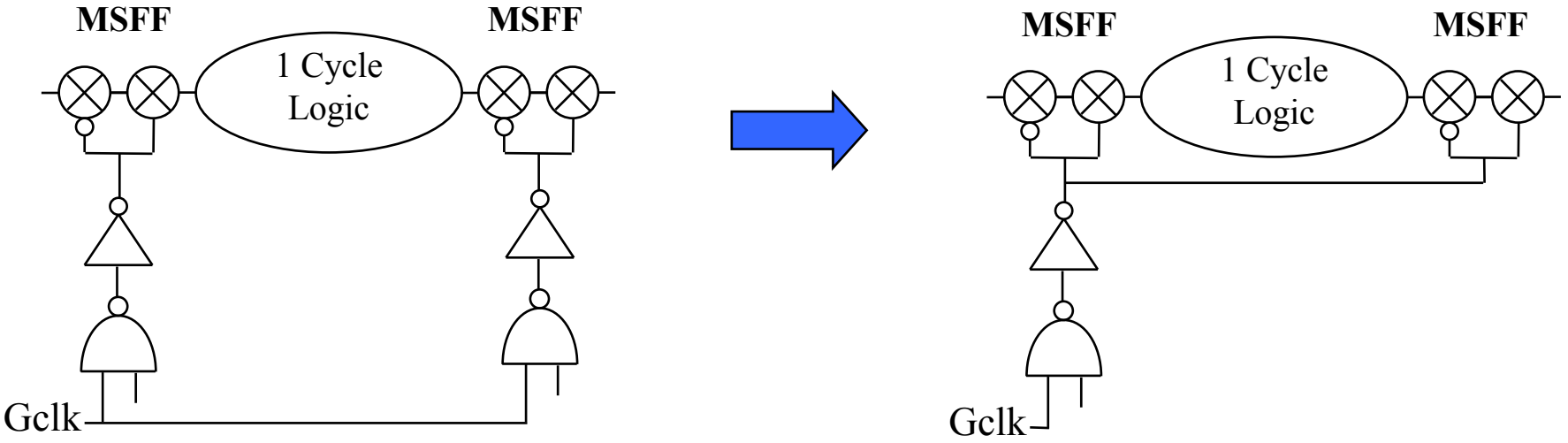
Delay Driver Clock



Delayed clocks allow logic to be divided into unequal pipestages.

Con: Reduces time in this pipestage
Increases clock skew

Closer Common Point for Clocks

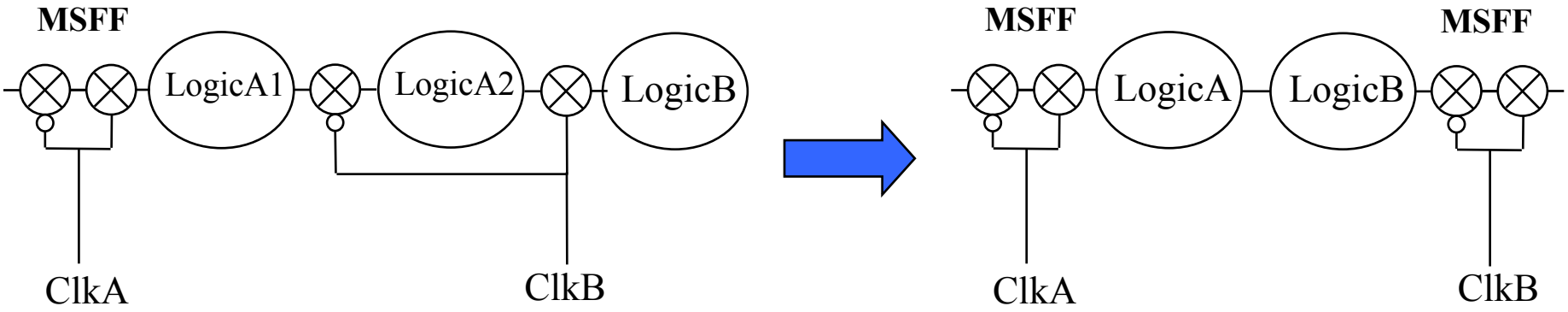


A closer common point reduces clock skew.

Con: Reduces opportunities for clock gating
May increase global clock load

Reduced clock skew improves maxdelay and mindelay.

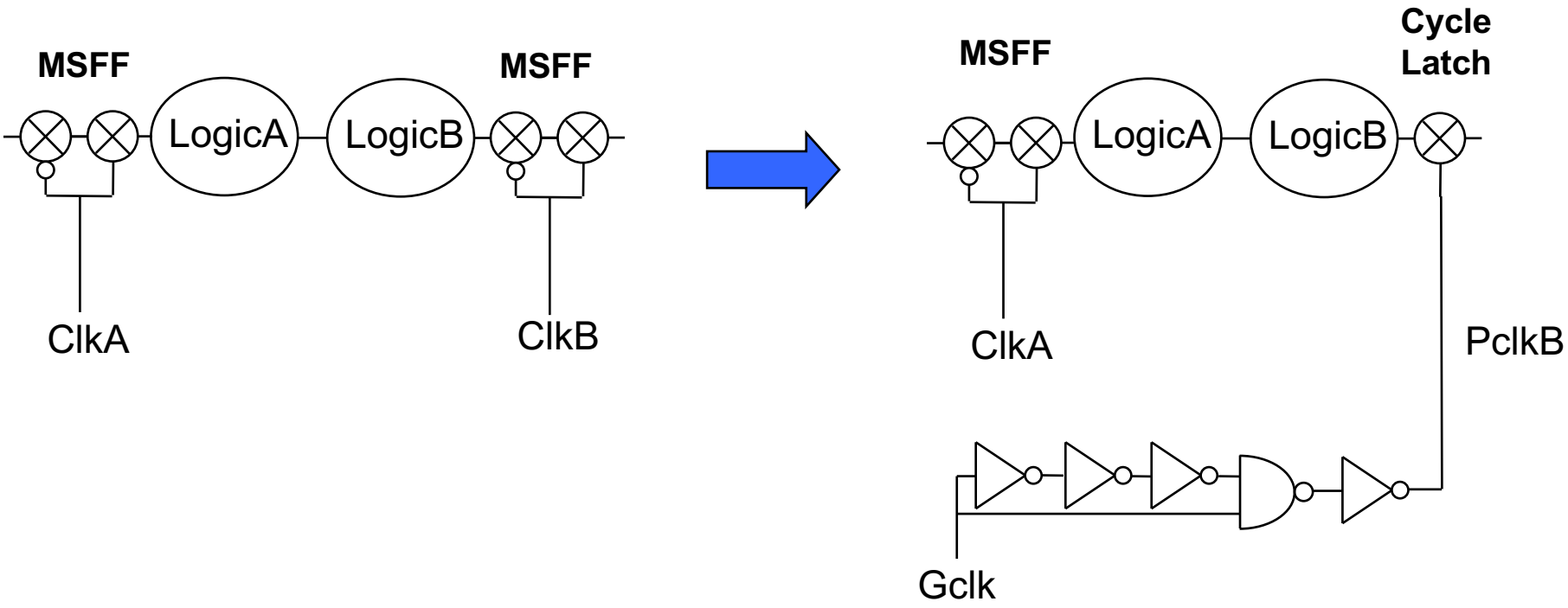
Change Phase-based to Cycle-based



Using only flip-flops allows a full cycle of logic between sequentials.

Con: Eliminates time borrowing

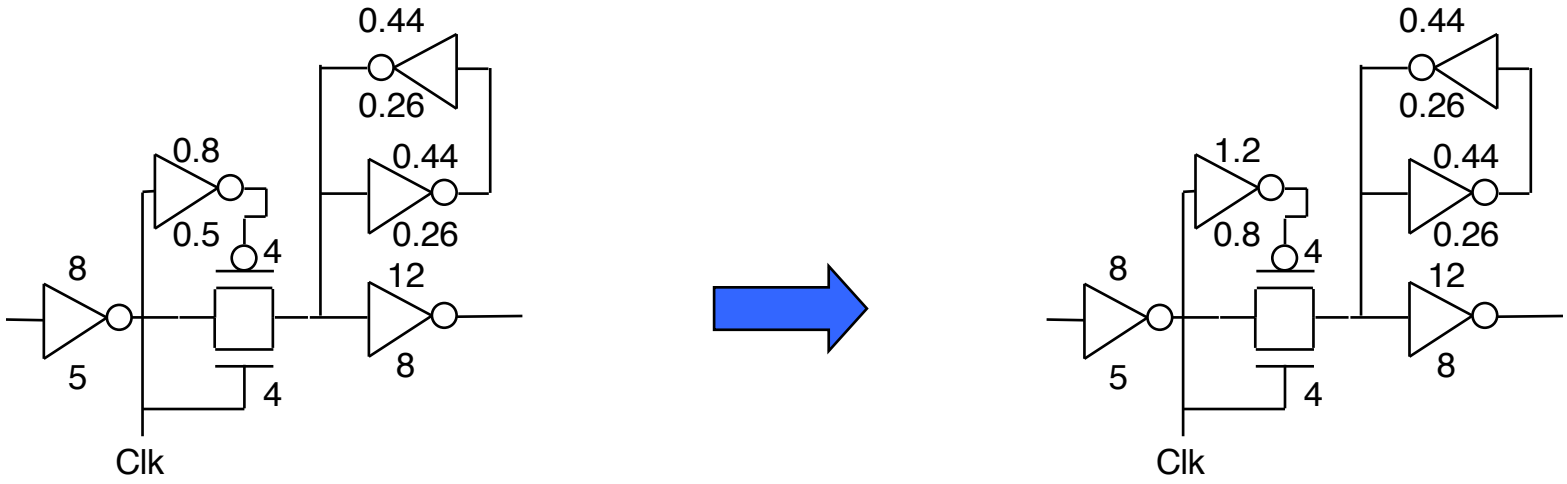
Pulsed Latches



Reduce sequential overhead by replacing MSFF with latch driven by pulsed clock.

Con: Increased mindelay requirement
More difficult timing analysis
PulseWidth-to-Delay race created

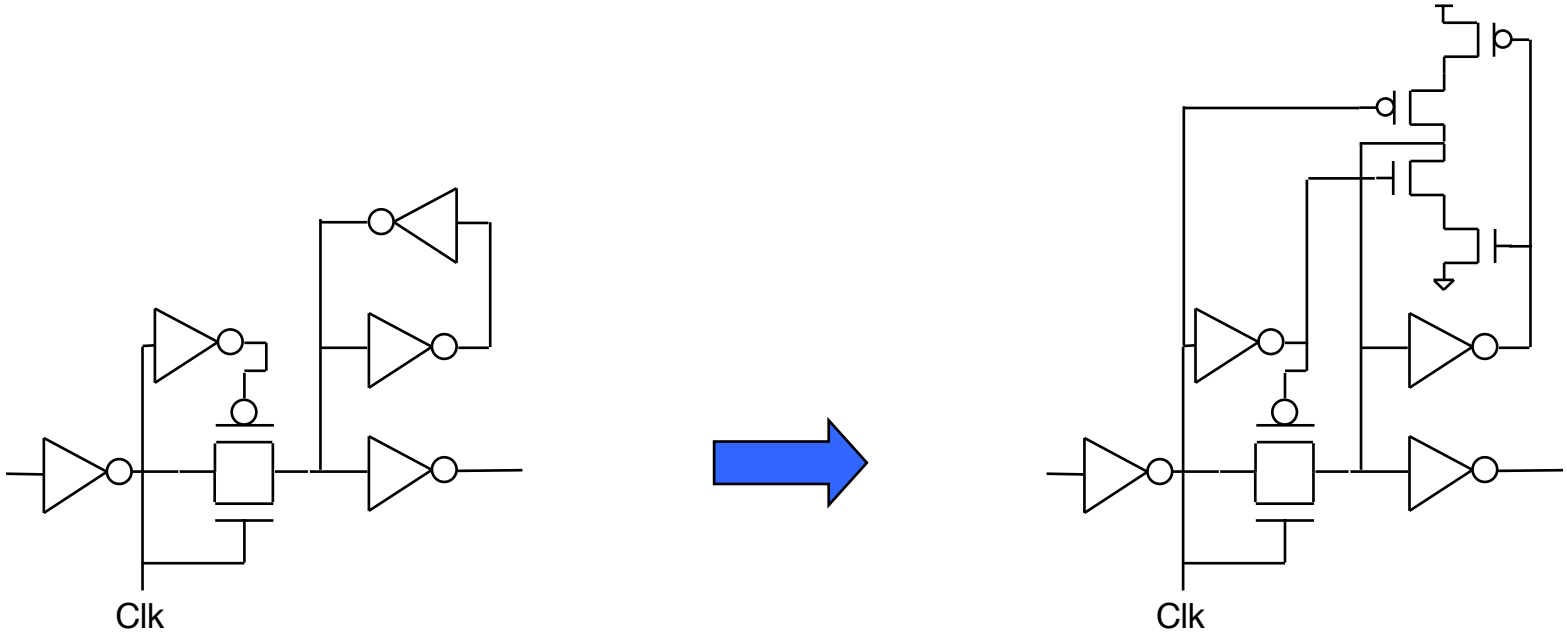
Speed Up Latch's Clock Inverter



Faster clock inverter closes pass gate sooner and reduces hold time.

Con: Very small improvement
Increased clock load

Change Jam Latch to Interrupted Keeper

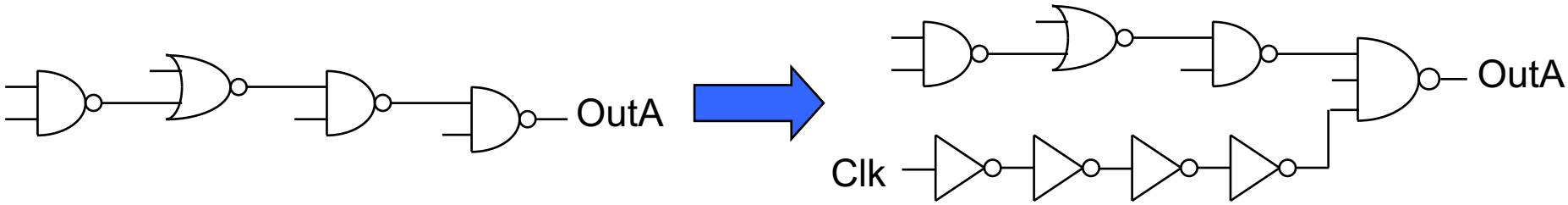


State node can be made to switch faster by eliminating contention with the keeper.

Con: Very small improvement
Increased clock load

Timer Circuit

Assume fall of OutA is the critical race

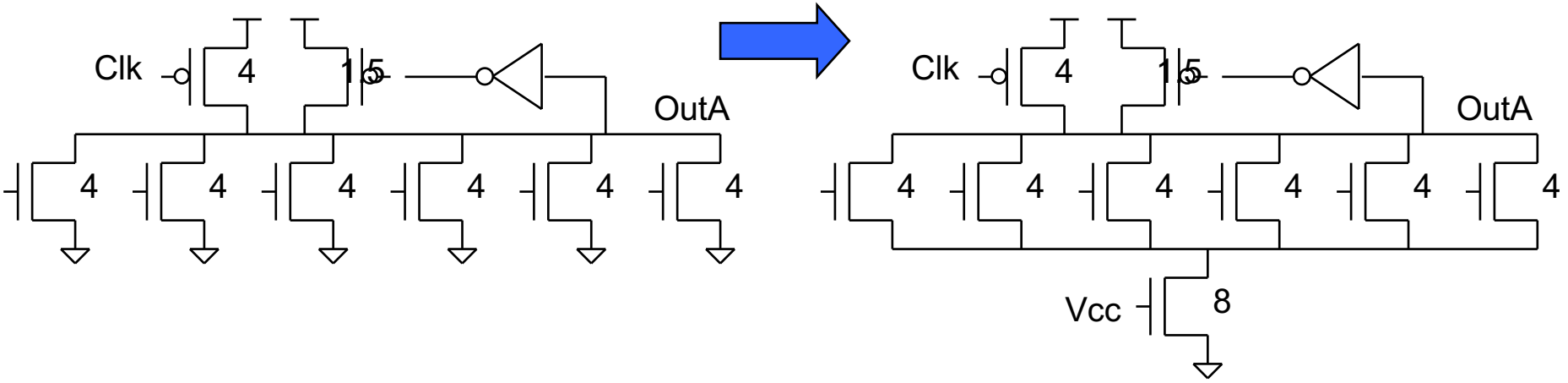


Timing signal prevents switching before a well controlled delay.

Con: Increases clock load Increases area
May not track with process variation

Current Limiting Device

Assume fall of OutA is the critical race



Added series device limits current when multiple parallel devices are on.

Con: Also slows single input switching

Review

- **MaxDelay Solutions**
  - Many methods available most make mindelay worse
- **MinDelay Solutions**
  - Many methods available, most make maxdelay worse
- **Pitfalls**
  - Be careful with contention, floating, and weakly held nodes

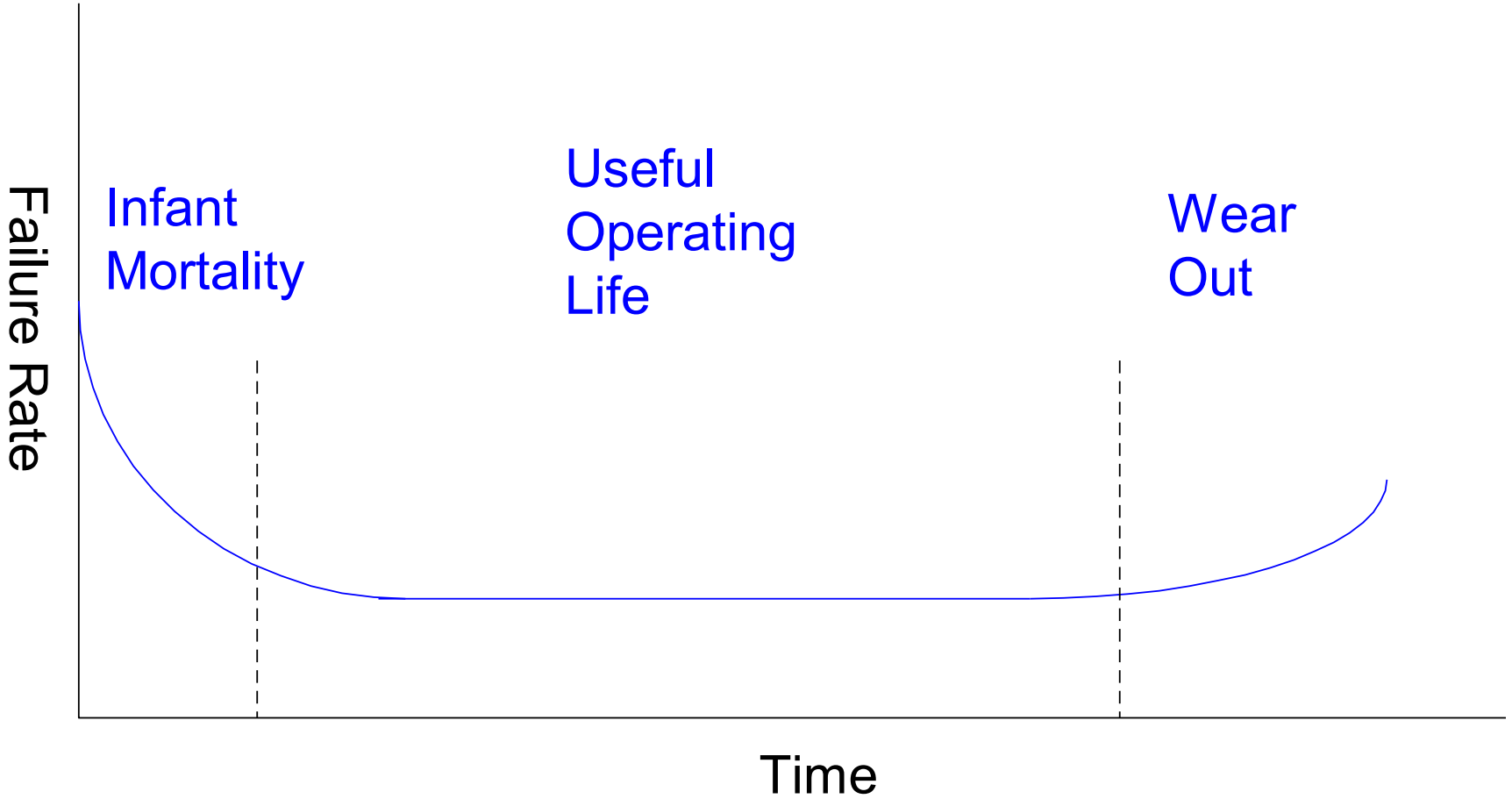
Circuit Robustness

Noise

- **Sources**
  - Power supply noise / ground bounce
  - Capacitive coupling
  - Charge sharing
  - Leakage
  - Noise feedthrough
- **Consequences**
  - Increased delay (for noise to settle out)
  - Or incorrect computations

Reliability

- **Hard Errors**
- **Soft Errors**



Electromigration

- "Electron wind" causes movement of metal atoms along wires
- Excessive electromigration leads to open circuits
- Most significant for unidirectional (DC) current
  - Depends on current density J_{dc} (current / area)
  - Exponential dependence on temperature
  - Black's Equation: $$MTTF \propto \frac{e^{\frac{E_a}{kT}}}{J_{dc}^{\ n}}$$
  - Typical limits: $J_{dc} < 1 - 2$ mA / μm²

Self-Heating

- **Current through wire resistance generates heat**
  - Oxide surrounding wires is a thermal insulator
  - Heat tends to build up in wires
  - Hotter wires are more resistive, slower
- **Self-heating limits AC current densities for reliability**

$$I_{rms} = \sqrt{\frac{\int_0^T I(t)^2 dt}{T}}$$

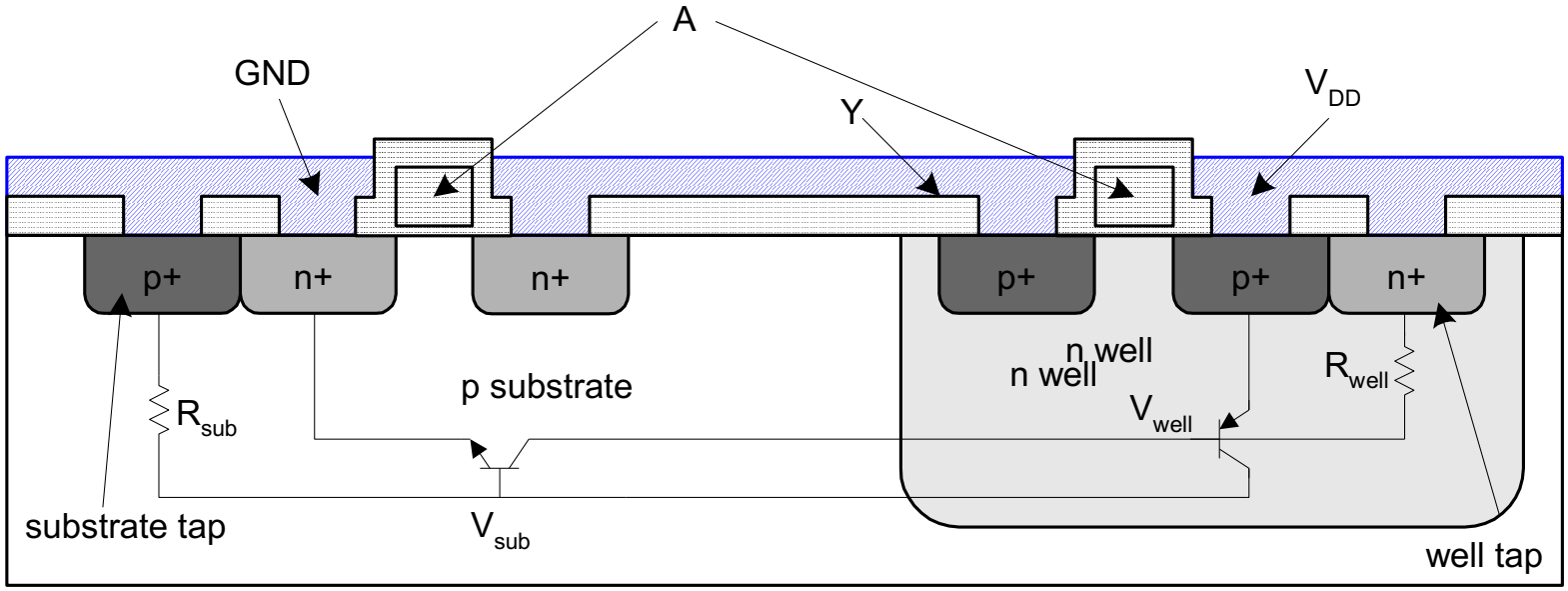
  - Typical limits: $J_{rms} < 15$ mA / μm^2

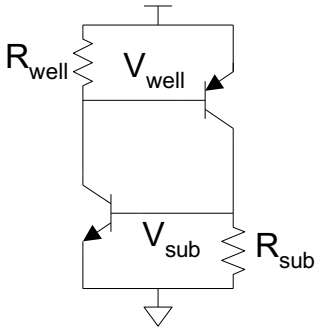
Hot Carriers

- **Electric fields across channel impart high energies to some carriers**
  - **These "hot" carriers may be blasted into the gate oxide where they become trapped**
  - **Accumulation of charge in oxide causes shift in Vt over time**
  - **Eventually Vt shifts too far for devices to operate correctly**
- **Choose VDD to achieve reasonable product lifetime**
  - **Worst problems for inverters and NORs with slow input rise time and long propagation delays**

Latchup

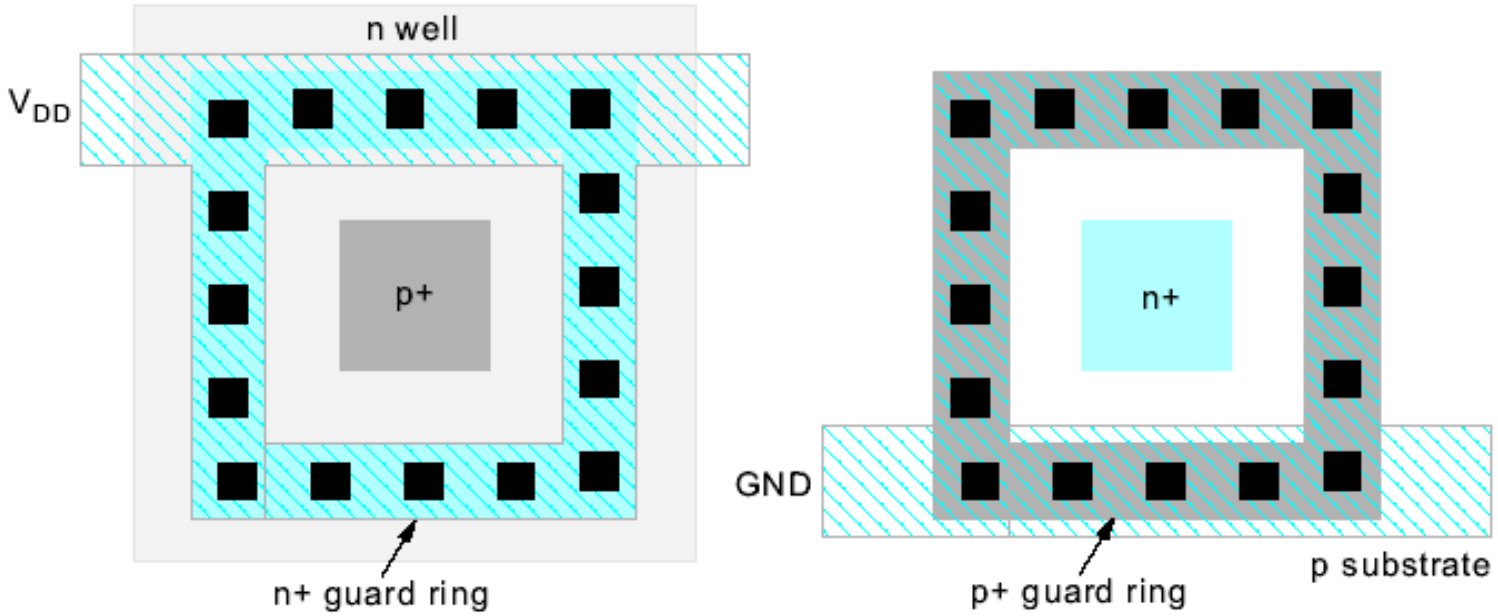
- **Latchup: positive feedback leading to V_{DD} – GND short**
  - Major problem for 1970s CMOS processes before it was well understood
- **Avoid by minimizing resistance of body to GND / V_{DD}**
  - Use plenty of substrate and well taps





Guard Rings

- Latchup risk greatest when diffusion-to-substrate diodes could become forward-biased
- Surround sensitive region with guard ring to collect injected charge



Overvoltage

- High voltages can damage transistors
  - Electrostatic discharge (ESD)
  - Oxide arcing
  - Punchthrough
  - Time-dependent dielectric breakdown (TDDB)
    - Accumulated wear from tunneling currents
- Requires low V_{DD} for thin oxides and short channels
- Use ESD protection structures where chip meets real world

Soft Errors

- In 1970s, DRAMs were observed to occasionally flip bits for no apparent reason
  - Ultimately linked to alpha particles and cosmic rays
- Collisions with particles create electron-hole pairs in substrate
  - These carriers are collected on dynamic nodes, disturbing the voltage
- Minimize soft errors by having plenty of charge on dynamic nodes
- Tolerate errors through ECC, redundancy

Summary

- **Static CMOS gates are very robust**
  - Will settle to correct value if you wait long enough
- **Other circuits suffer from a variety of pitfalls**
  - Tradeoff between performance & robustness
- **Very important to check circuits for pitfalls**
  - For large chips, you need an automatic checker
  - Design rules aren't worth the paper they are printed on unless you back them up with a tool