Lecture 2:
CMOS Fabrication

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Agenda

- **Last module:**
  - Introduction to the course
  - How a transistor works
  - CMOS transistors

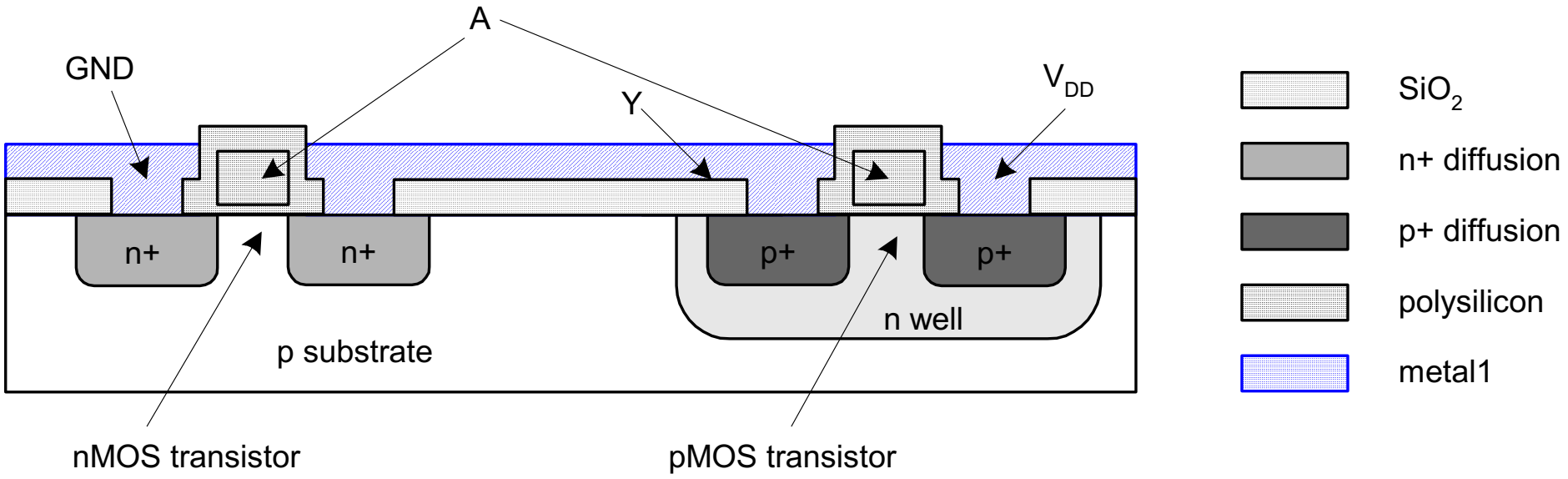
- **This module:**
  - CMOS Fabrication

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafers
- Lithography process has been the mainstream chip manufacturing process
  - Similar to a printing press
  - See Chris Mack's page for a nice litho tutorial
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

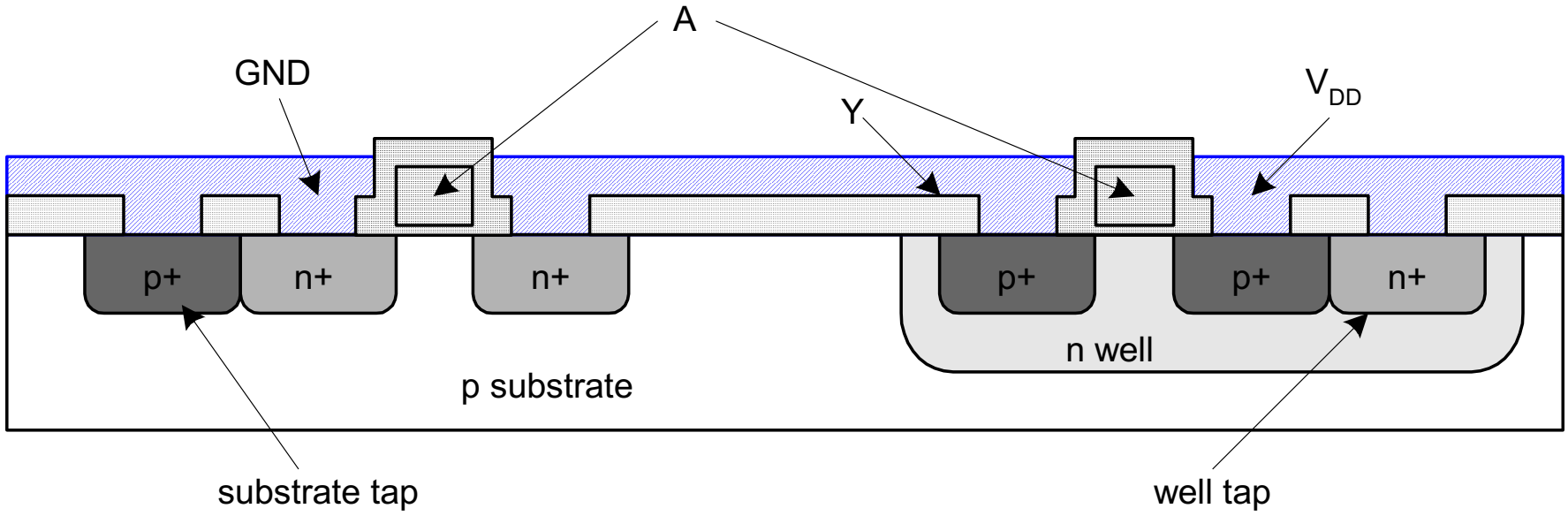
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



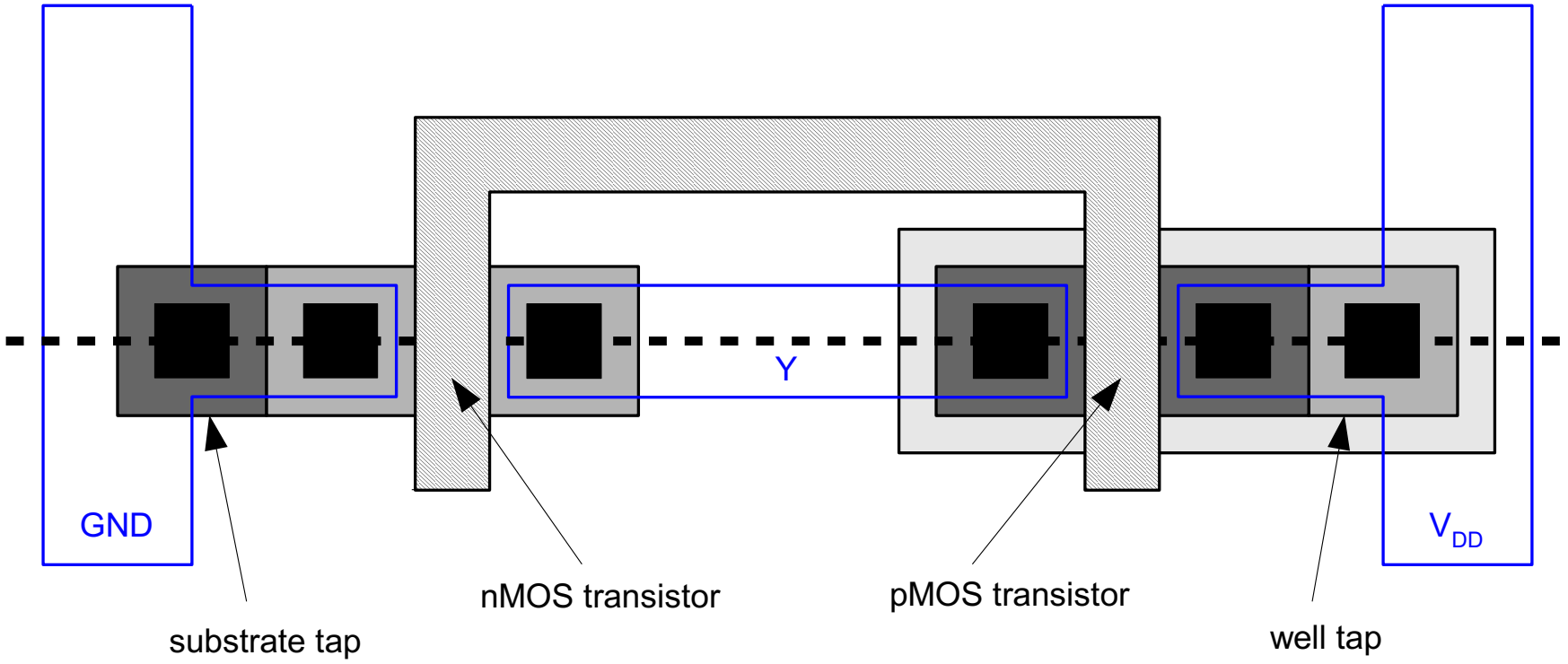
Well and Substrate Taps

- Substrate must be tied to GND, n-well to VDD
- Metal to lightly-doped semiconductor forms poor connection called Schottky Diode
- Use heavily doped well and substrate contacts / taps



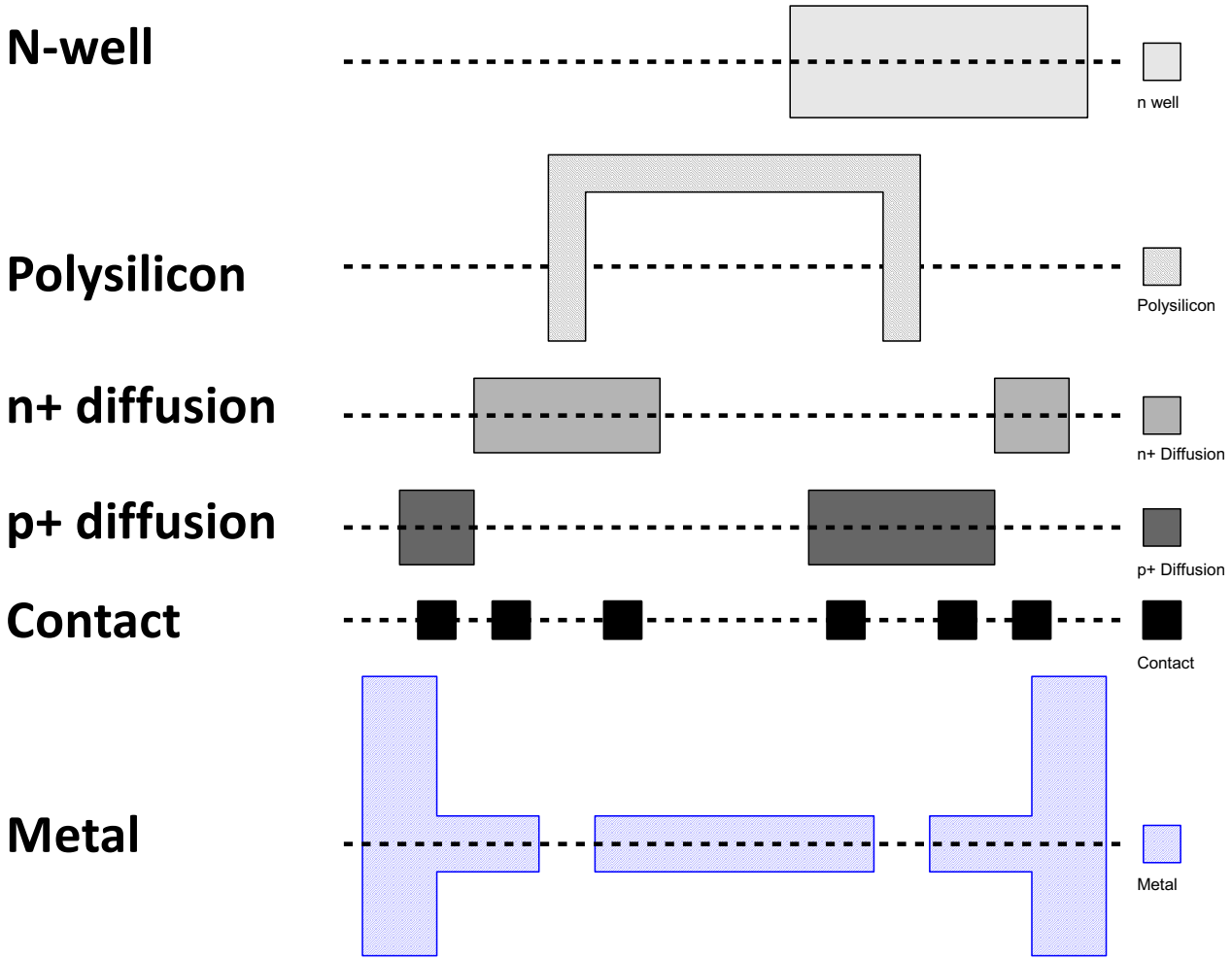
Inverter Mask Set

- Transistors and wires are defined by masks
- Cross-section taken along dashed line



Detailed Mask Views

Six masks to build simple inverter

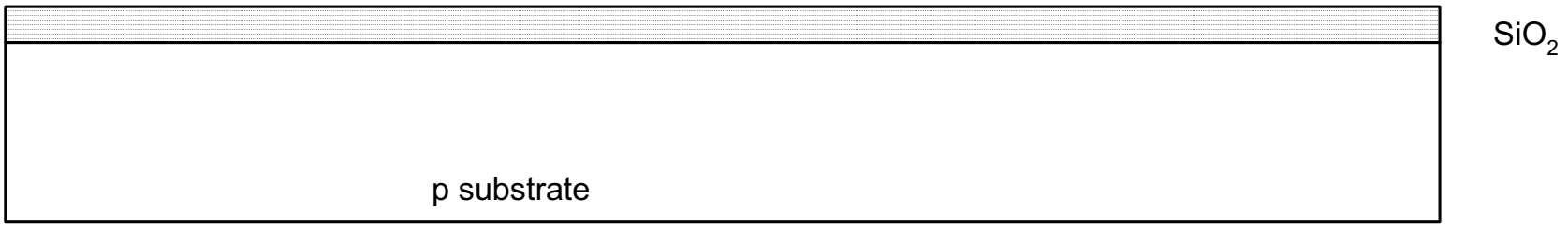


Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

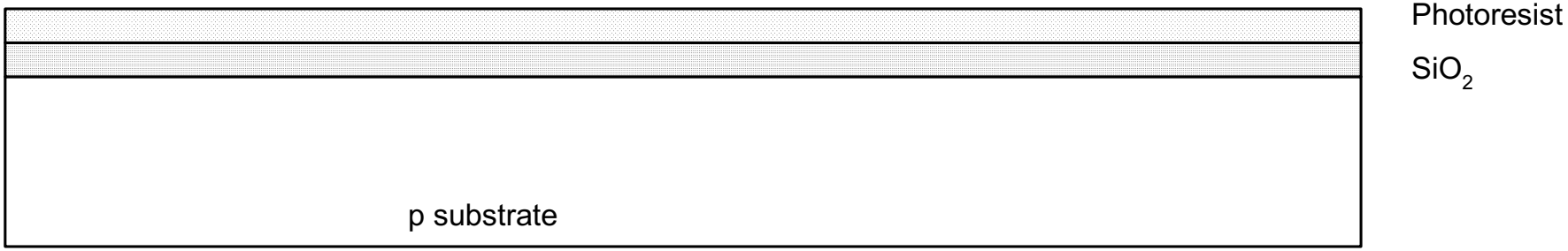
Oxidation

- **Grow SiO_2 on top of Si wafer**
  - **900℃ - 1200℃ with H_2O or O_2 in an oxidation furnace**



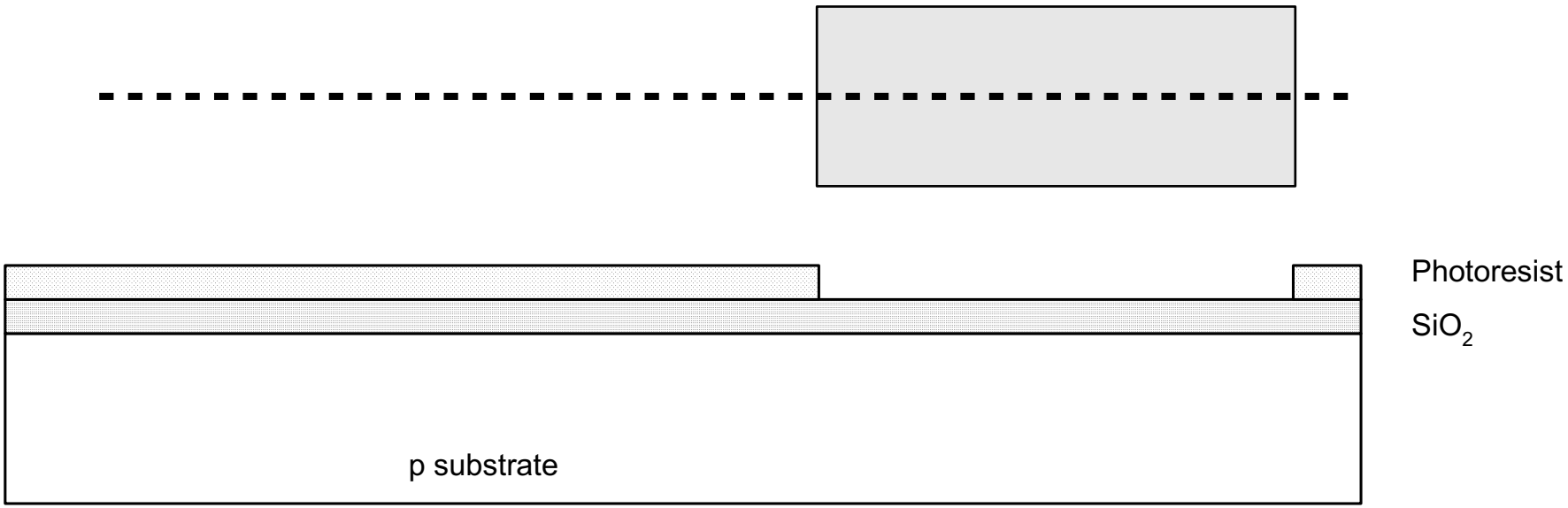
Photoresist

- **Spin on photoresist**
  - **Photoresist is a light-sensitive organic polymer**
  - **Softens where exposed to light**



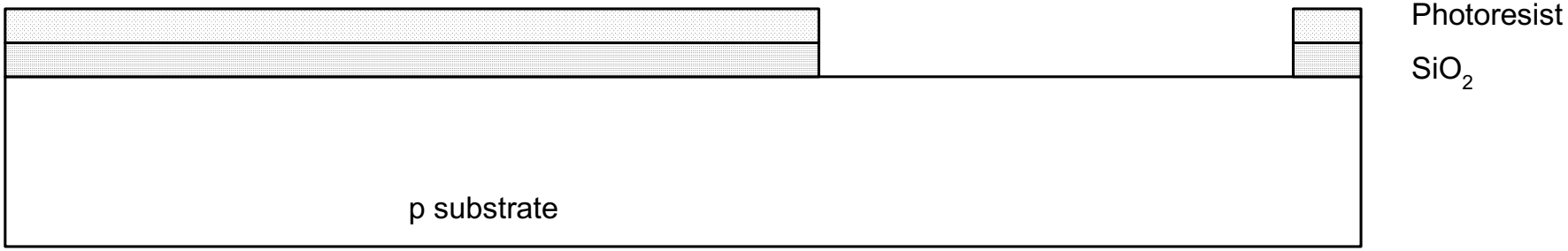
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



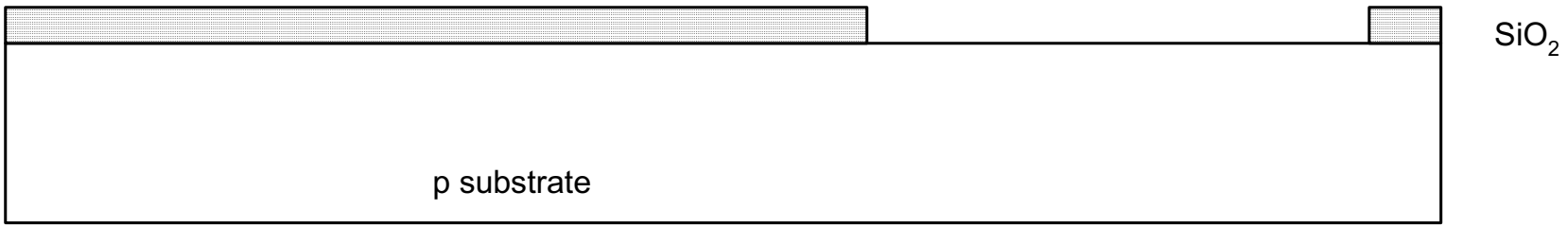
Etch

- **Etch oxide with hydrofluoric acid (HF)**
  - **Seeps through skin and eats bone; nasty stuff!!!**
- **Only attacks oxide where resist has been exposed**



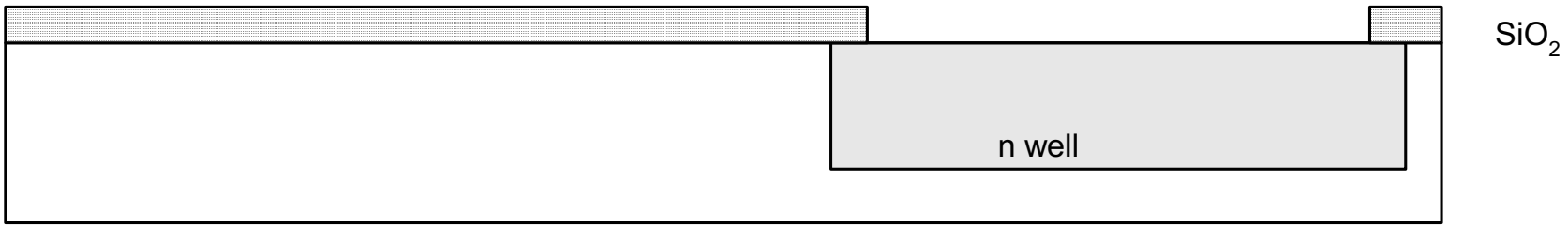
Strip Photoresist

- **Strip off remaining photoresist**
  - Old days we used a mixture of nitric and sulphuric acids called piranah etch
  - Now we use a plasma etch which is much safer (and greener).
- **Necessary so resist doesn't melt in the next step**



n-Well

- **n-Well formed with diffusion or ion implant**
- **Diffusion**
  - **Place wafer in furnace with Arsine (AsH_3) gas**
  - **Heat until As atoms diffuse into exposed Si**
- **Ion Implantation**
  - **Blast wafer with beam of As ions**
  - **Ions blocked by SiO_2, only enter exposed Si**

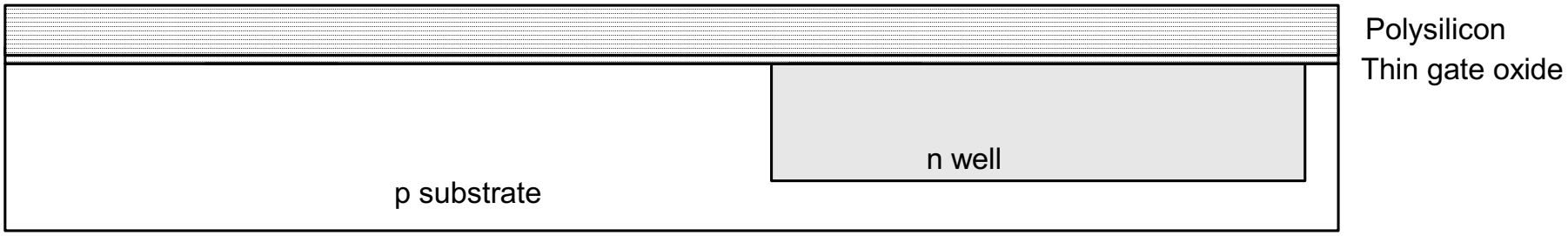


Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

Polysilicon

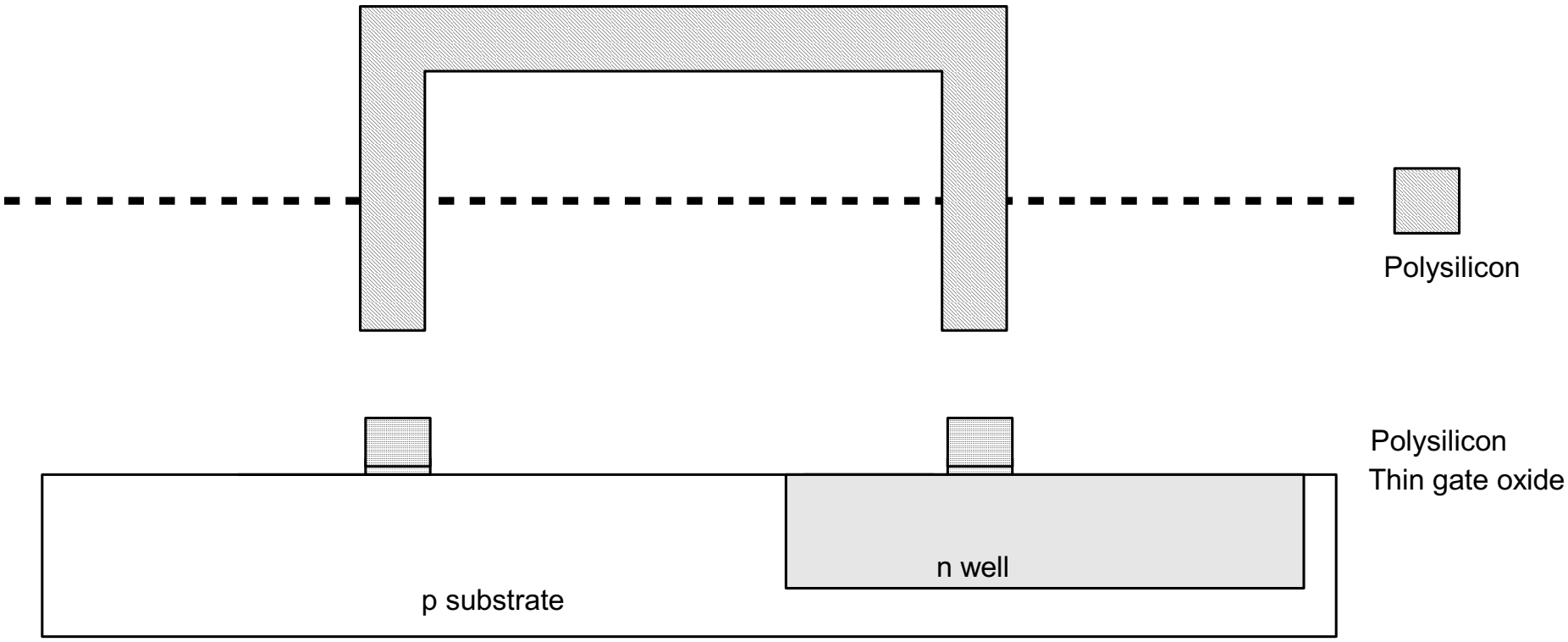
- **Grow/deposit very thin layer of gate oxide**
  - **< 20 Å (6-7 atomic layers)**
- **Chemical Vapor Deposition (CVD) of Si layer**
  - **Place wafer in furnace with Silane gas (SiH_4)**
  - **Forms many small crystals called polysilicon**
  - **Heavily doped to be good conductor**



Trend towards metal gates and rare earth (Hf, etc.) oxides in nanometer-scale processes

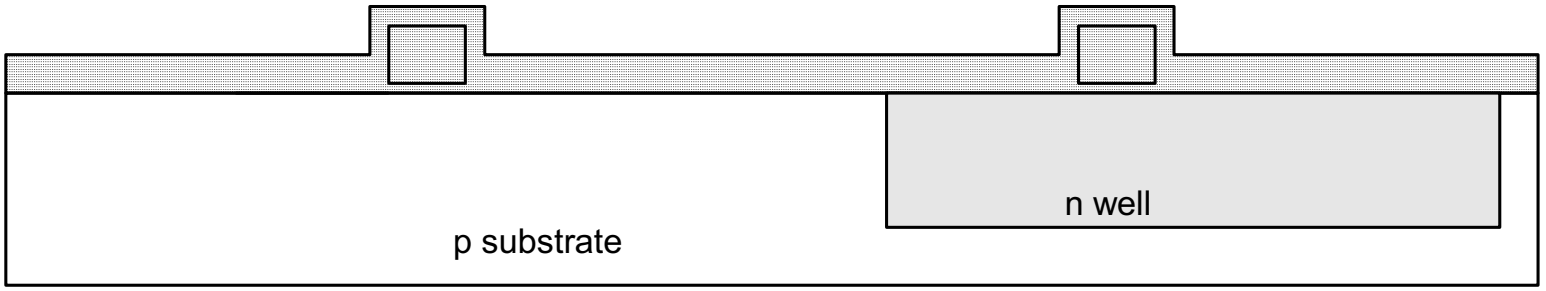
Polysilicon Patterning

- **Use same lithography process to pattern polysilicon**



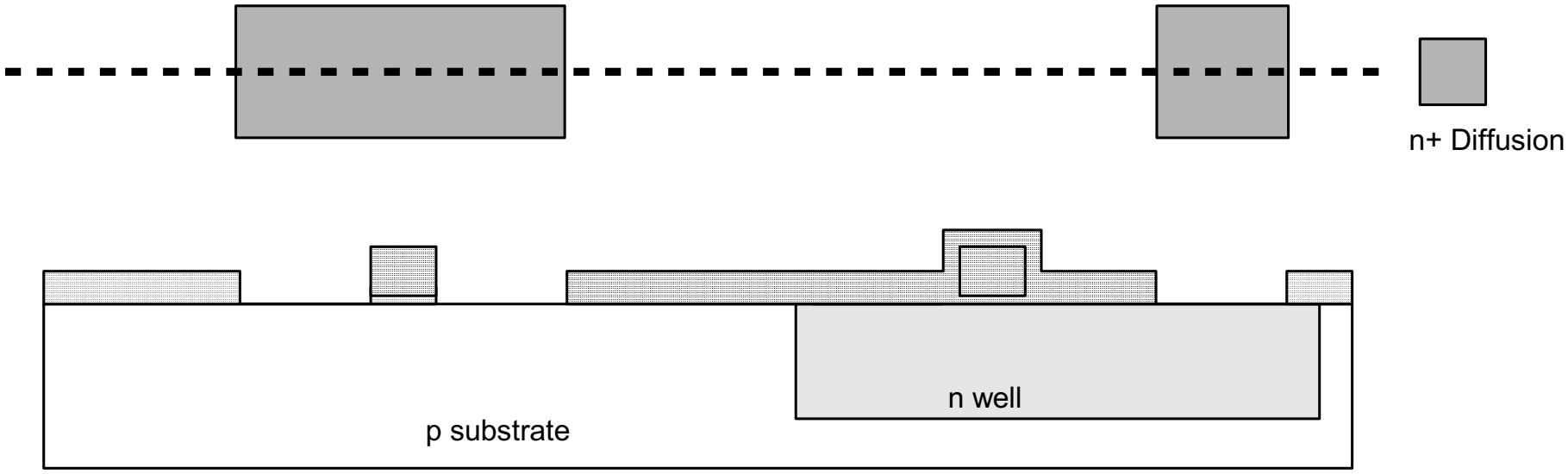
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



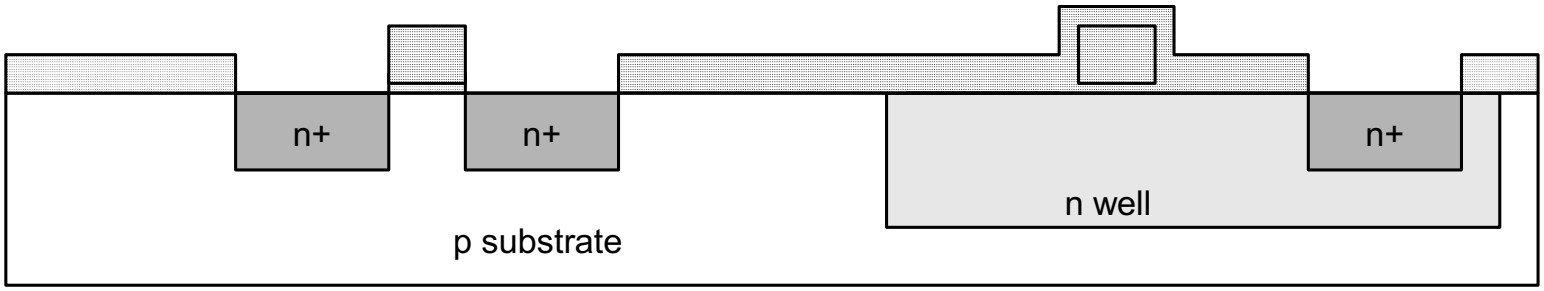
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* - gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



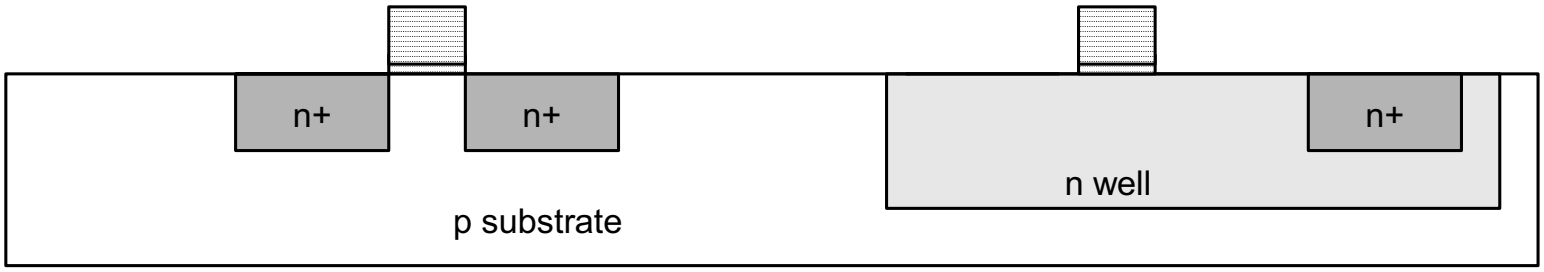
N-diffusion, Cont'd

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



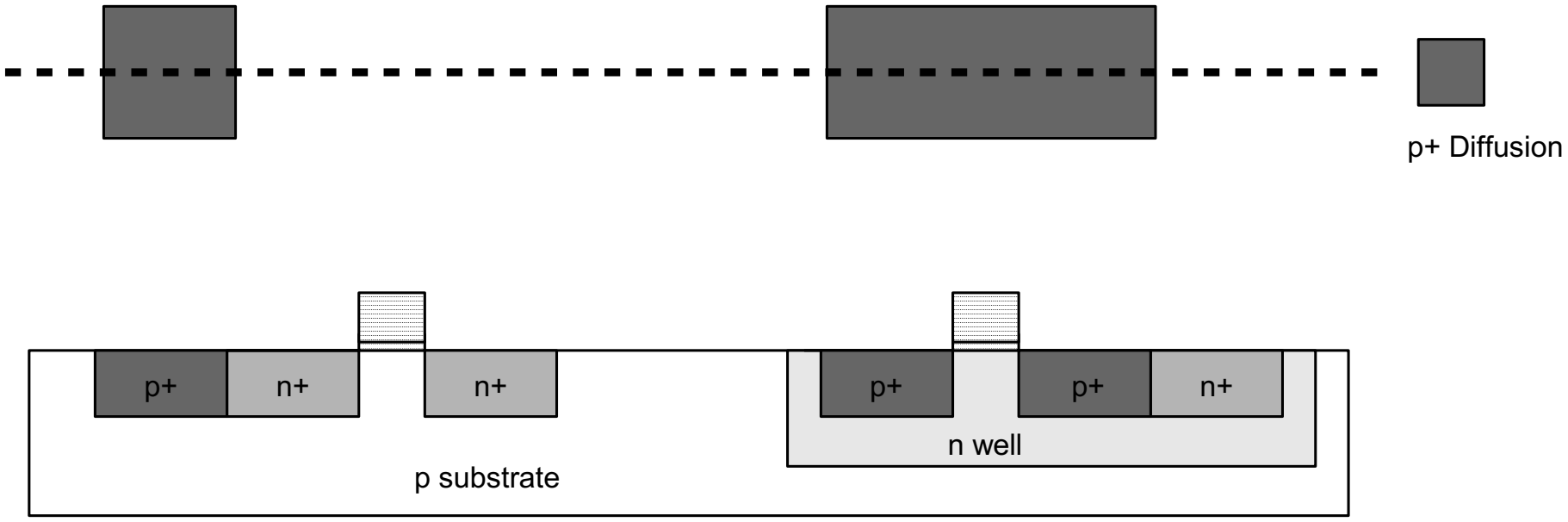
N-diffusion, Cont'd

- **Strip off oxide to complete patterning step**



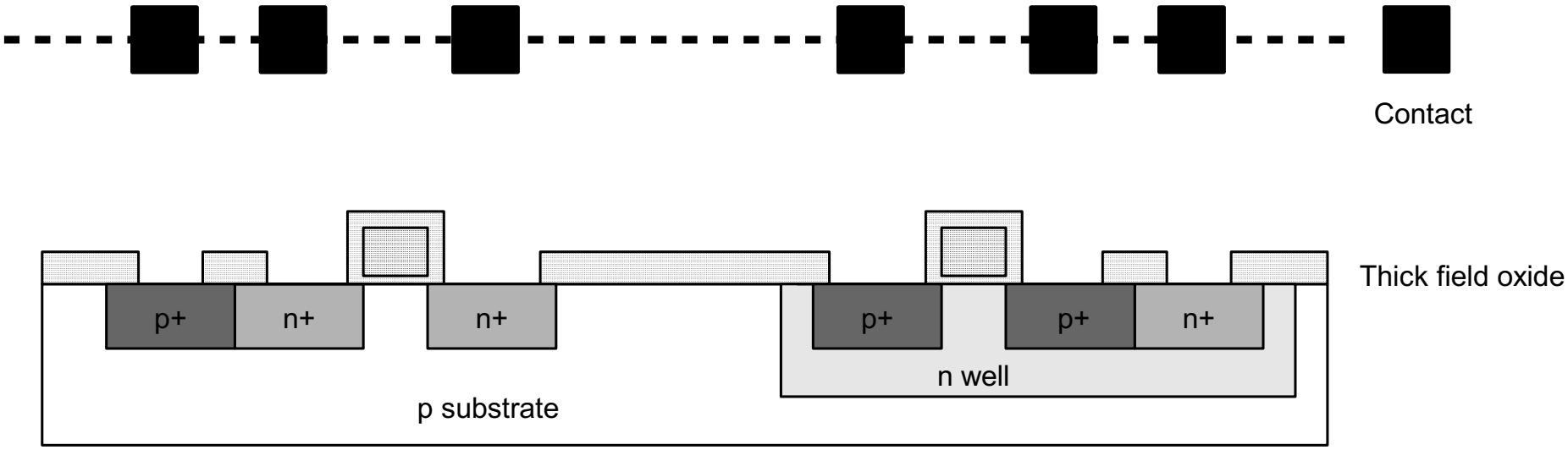
P-Diffusion

- **Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact**



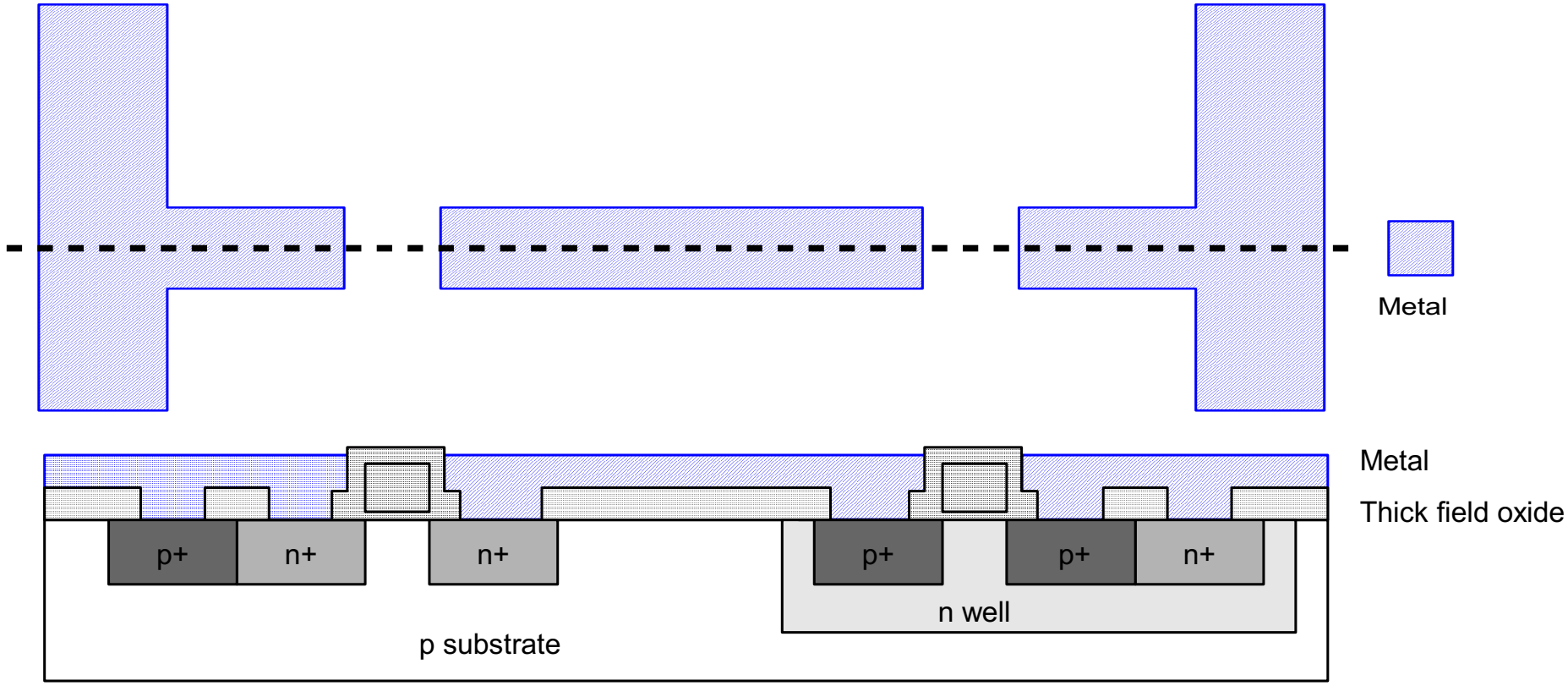
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed

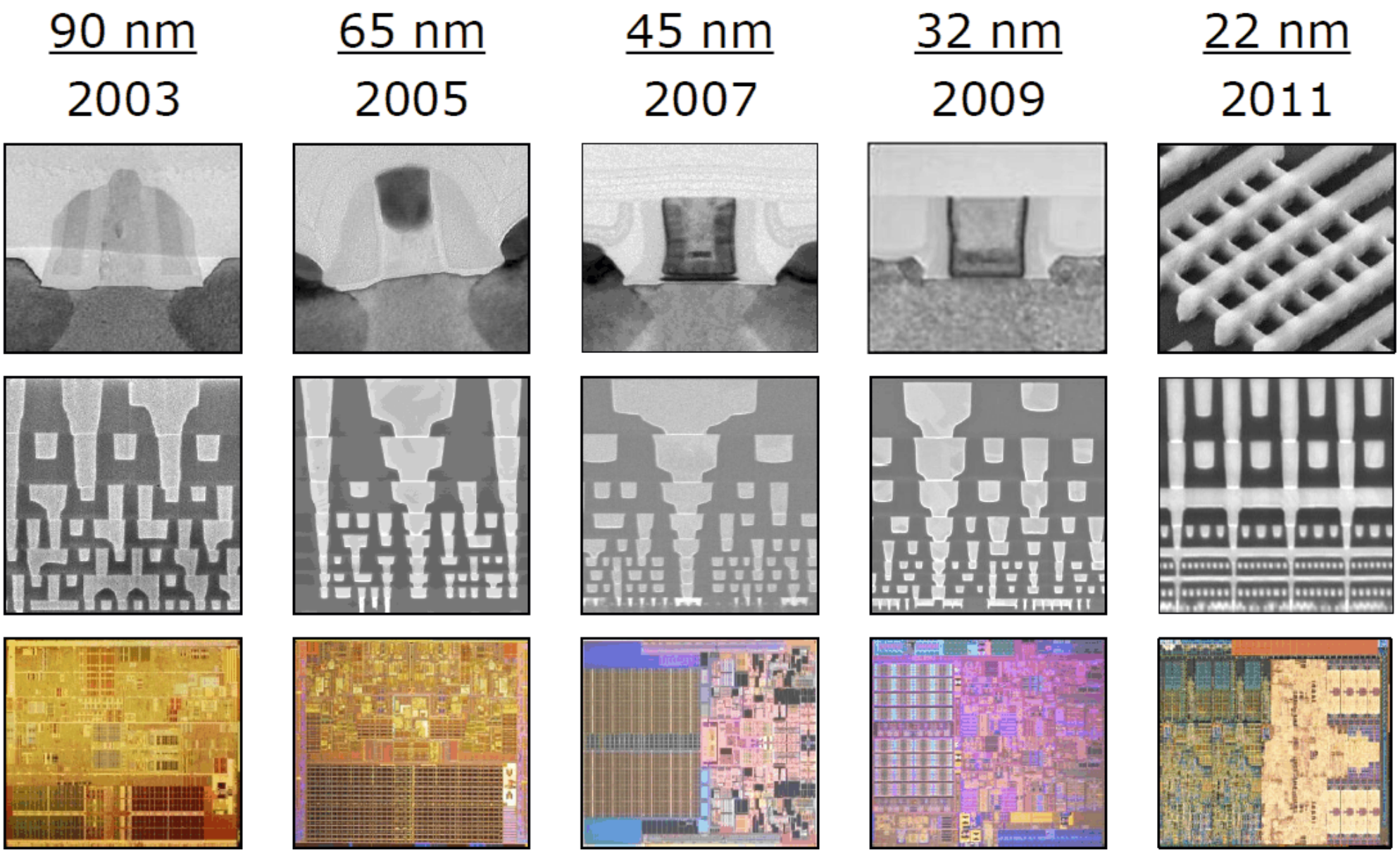


Metallization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

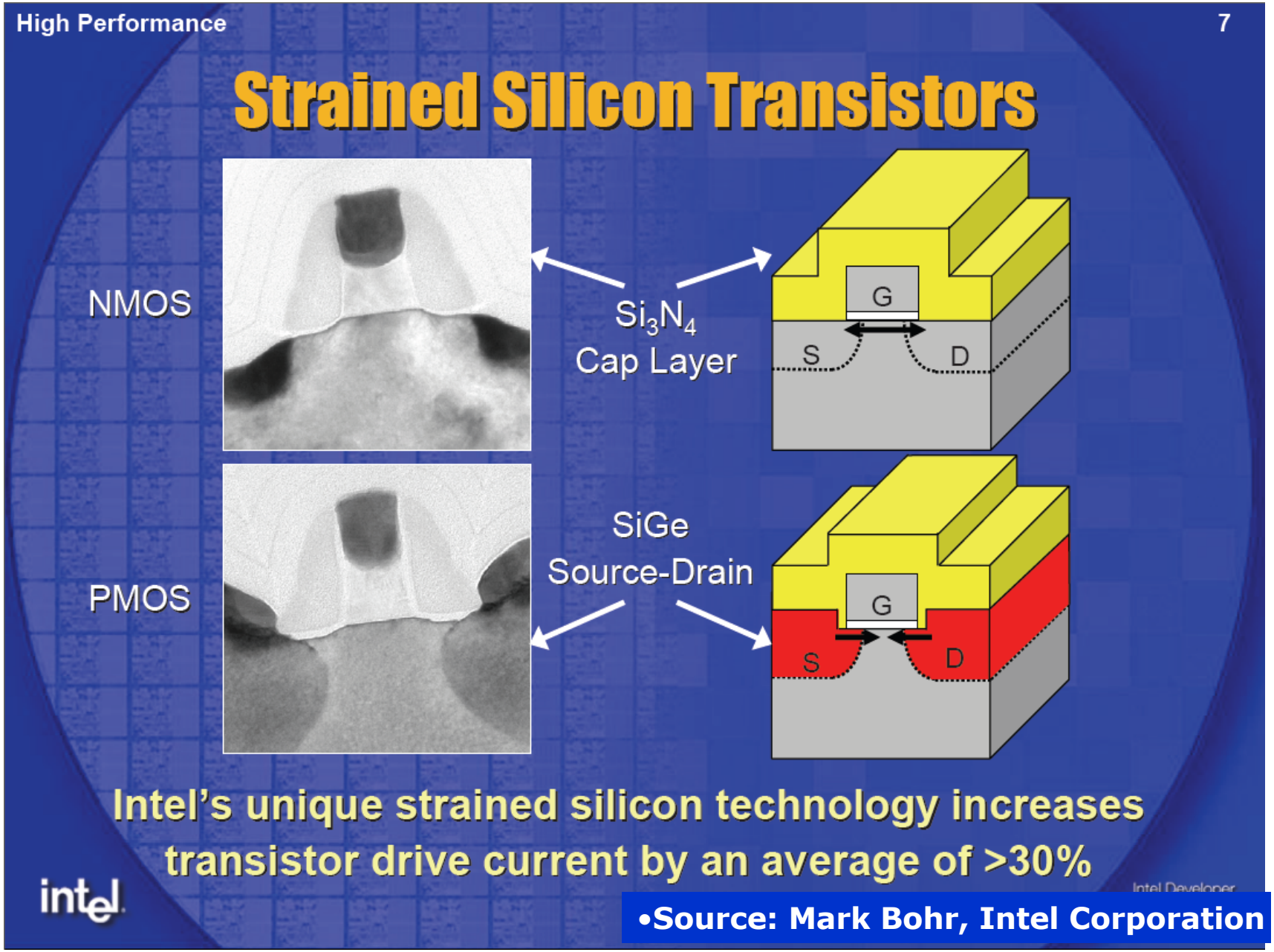


Intel's 2-Year Technology Cadence

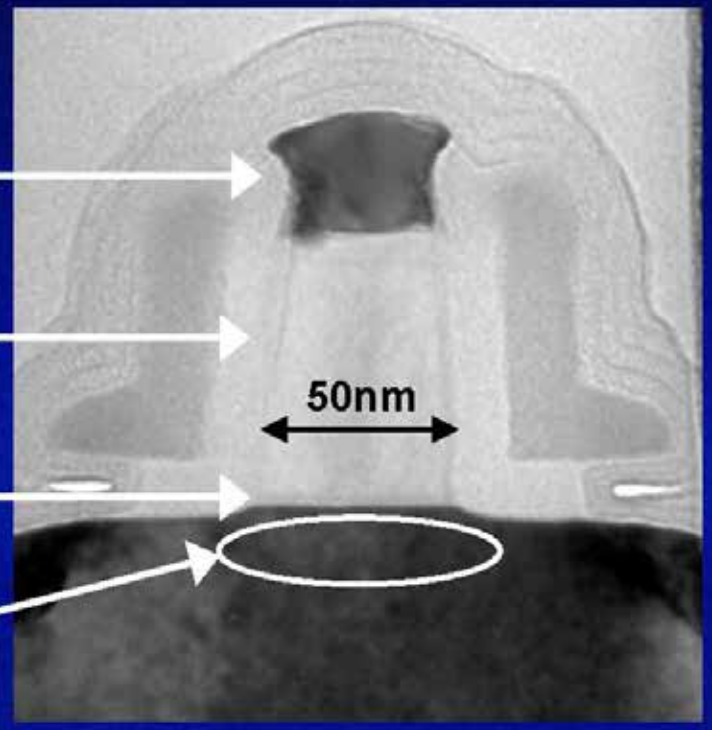


•Source: Mark Bohr, Intel Corporation

MOBILITY IMPROVEMENT



90 nm Generation Transistor



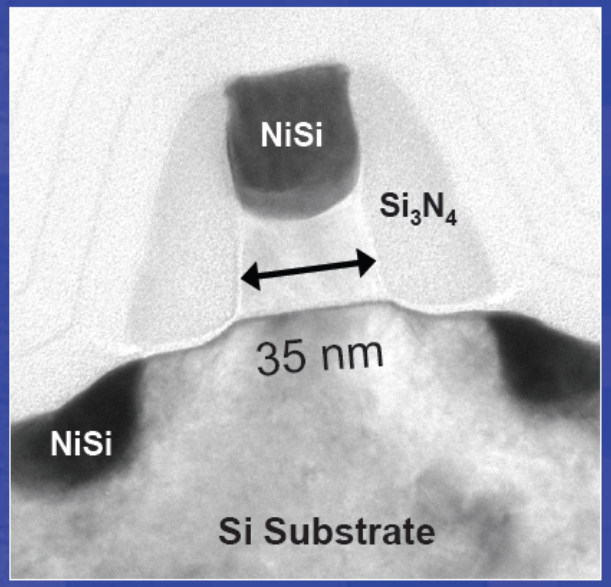
- Strained silicon increases electron/hole mobility.

Intel

- **Source: Mark Bohr, Intel Corporation**

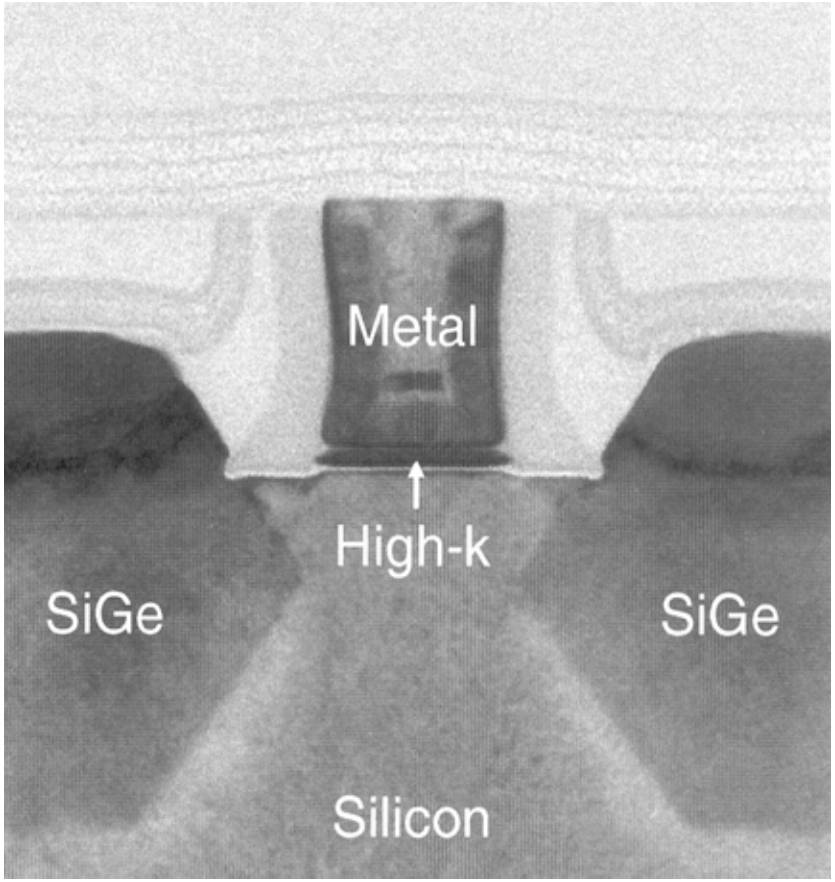
65 nm Generation Transistors

- 35 nm gate length
- 1.2 nm gate oxide
- NiSi for low resistance
- 2ND generation strained silicon for enhanced performance



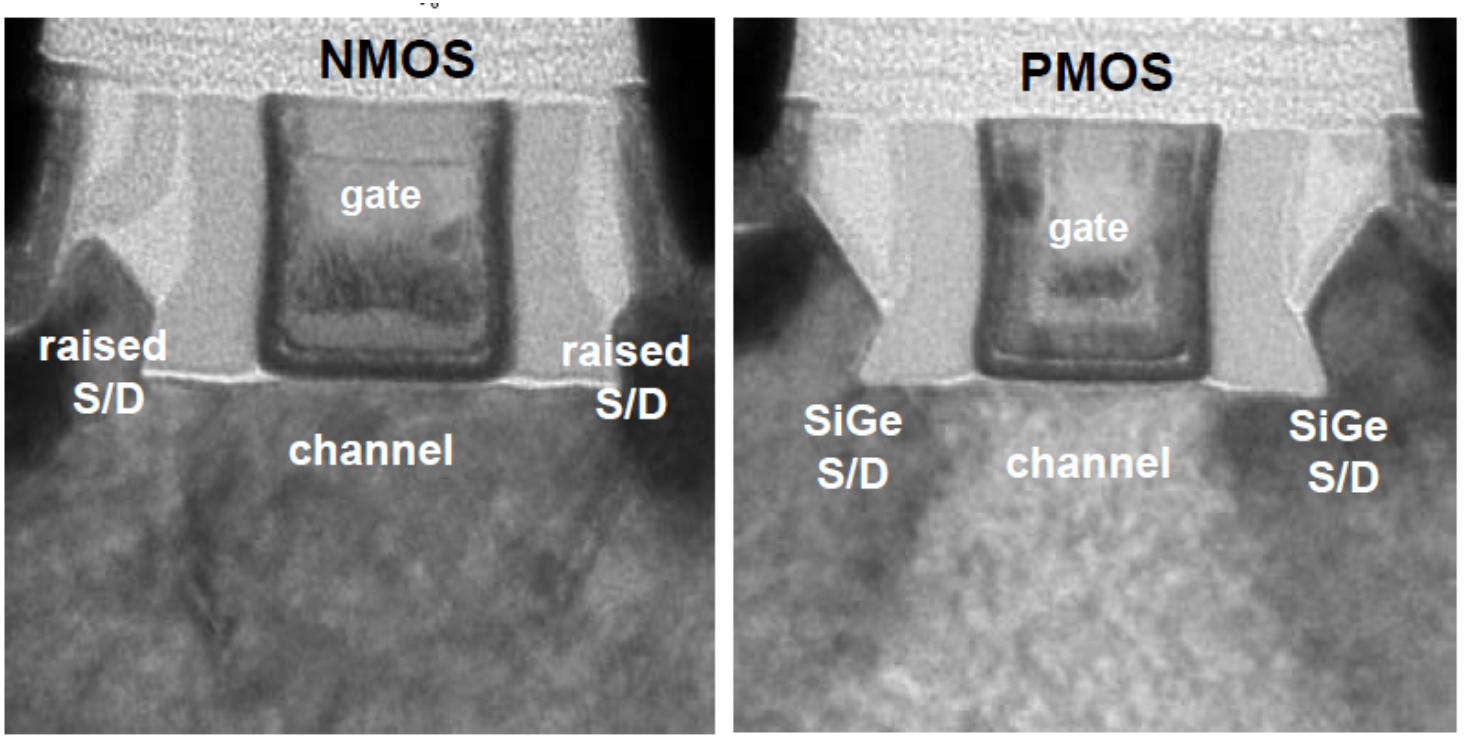
•Source: Mark Bohr, Intel Corporation

High-K, Metal Gate 45 nm CMOS (Intel)



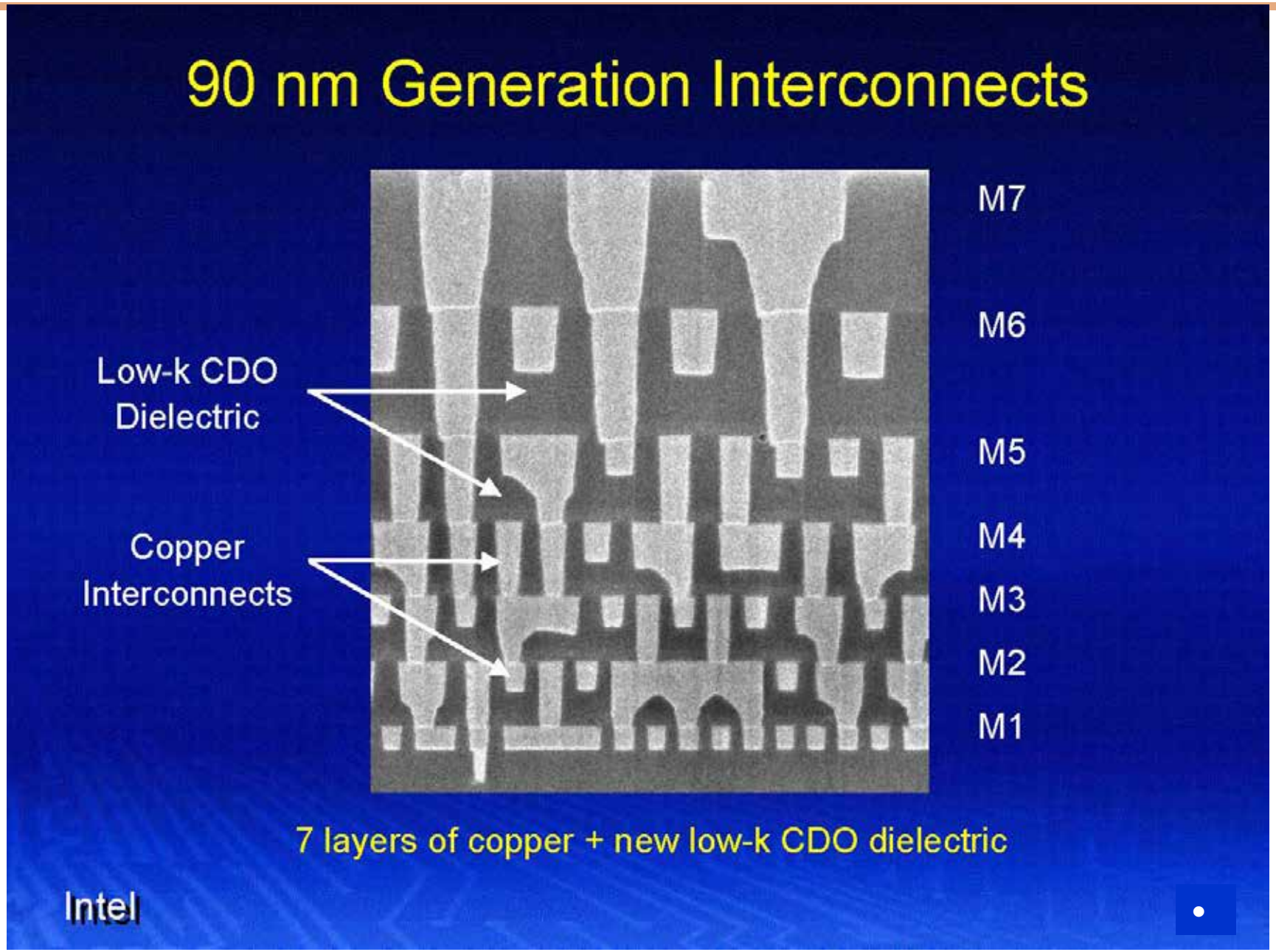
•K. Mistry, et al., "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging", Tech. Digest IEDM, Dec 2007.

High-K, Metal Gate 32 nm CMOS (Intel)

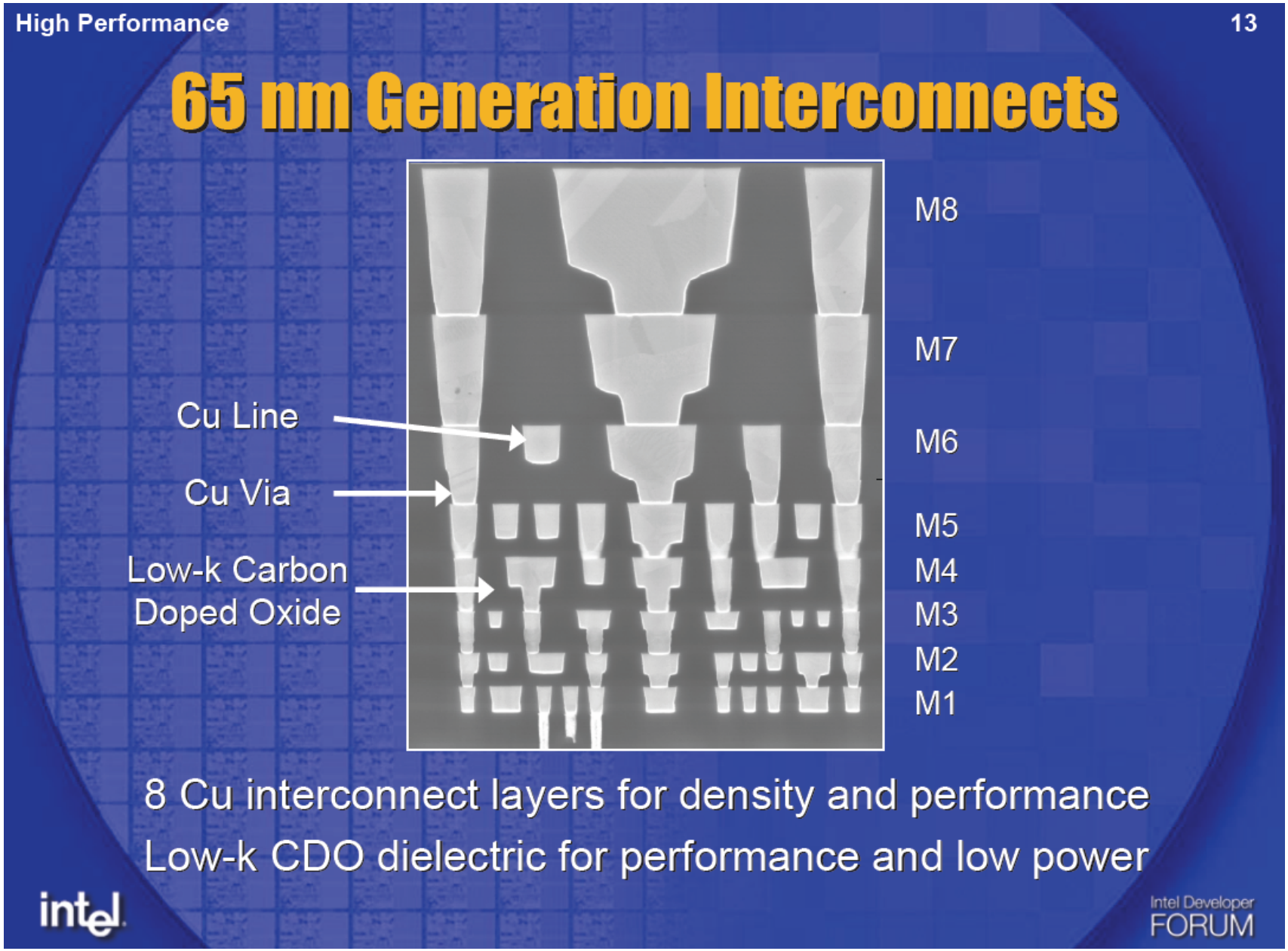


•P. Packan, et al., "High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors", Tech. Digest IEDM, Dec 2009.

90nm INTERCONNECT



65nm INTERCONNECT



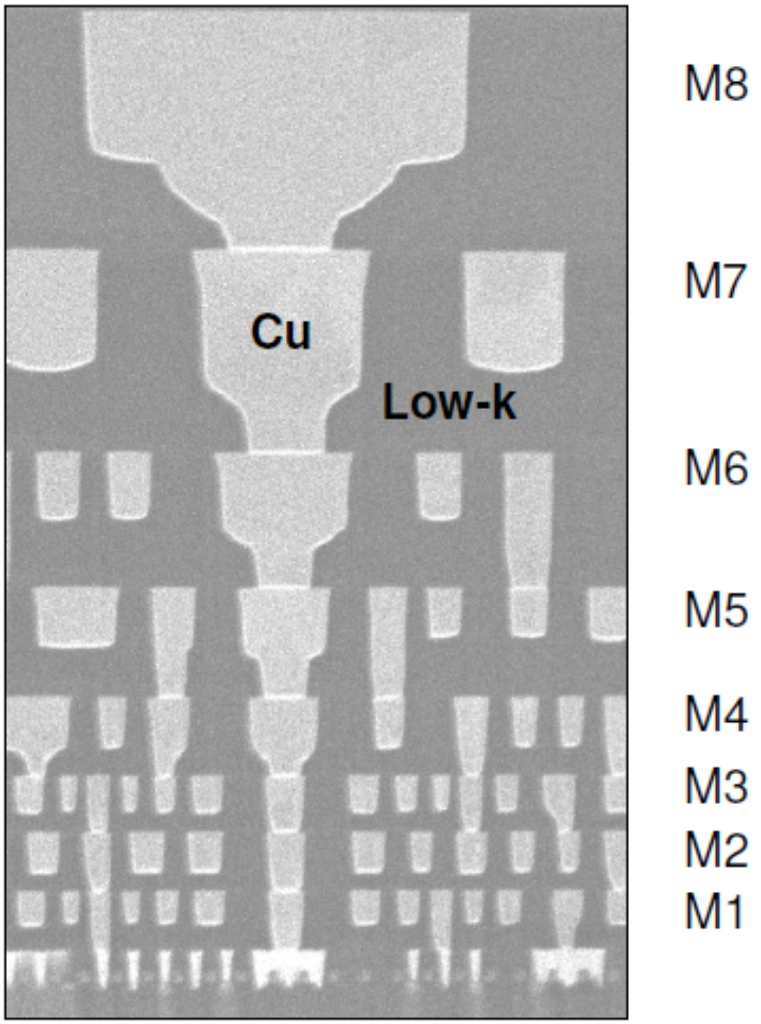
45nm Interconnect

Loose pitch + thick metal on upper layers:

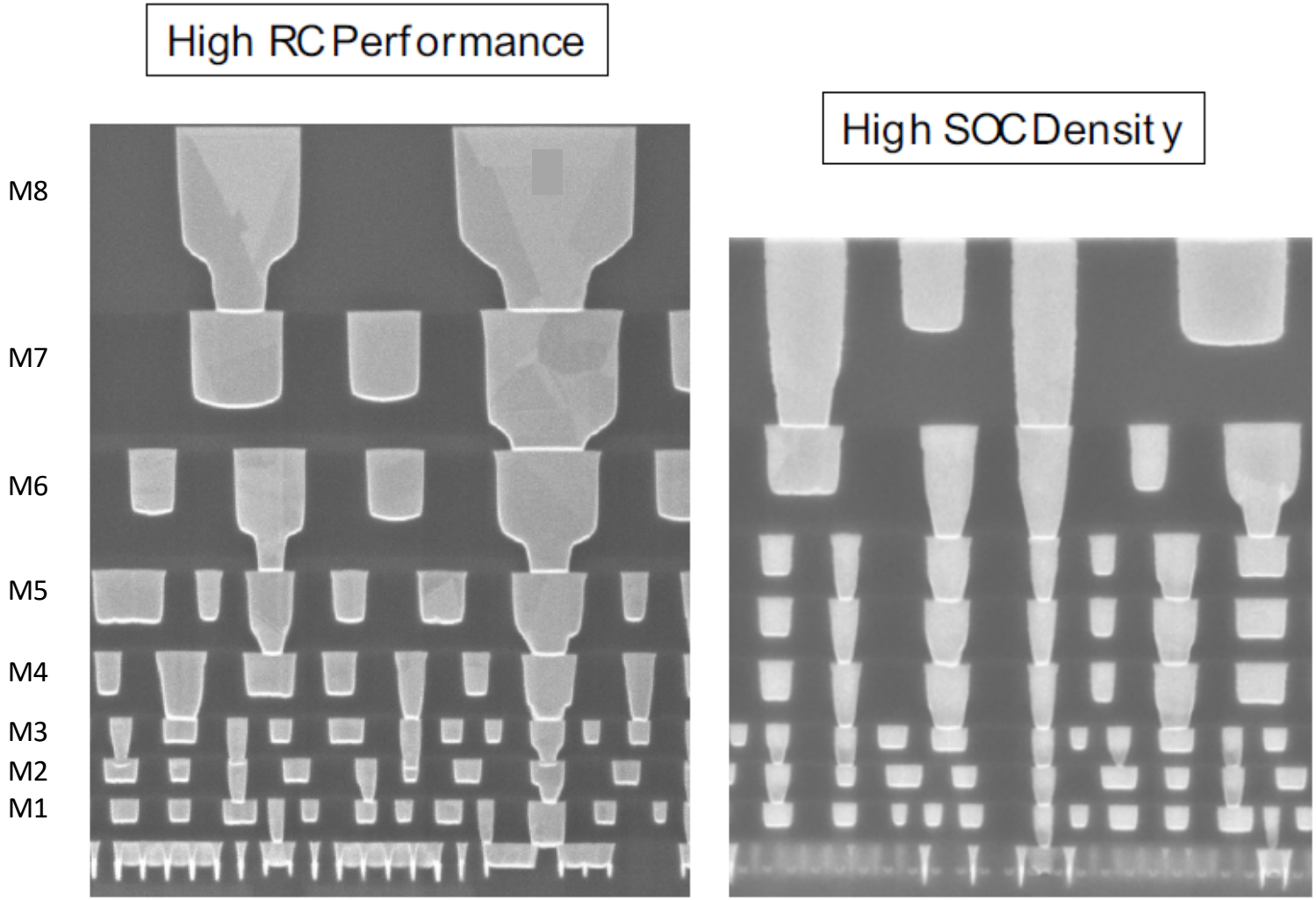
- High speed global wires
- Low resistance power grid

Tight pitch on lower layers:

- Maximum density for local interconnects



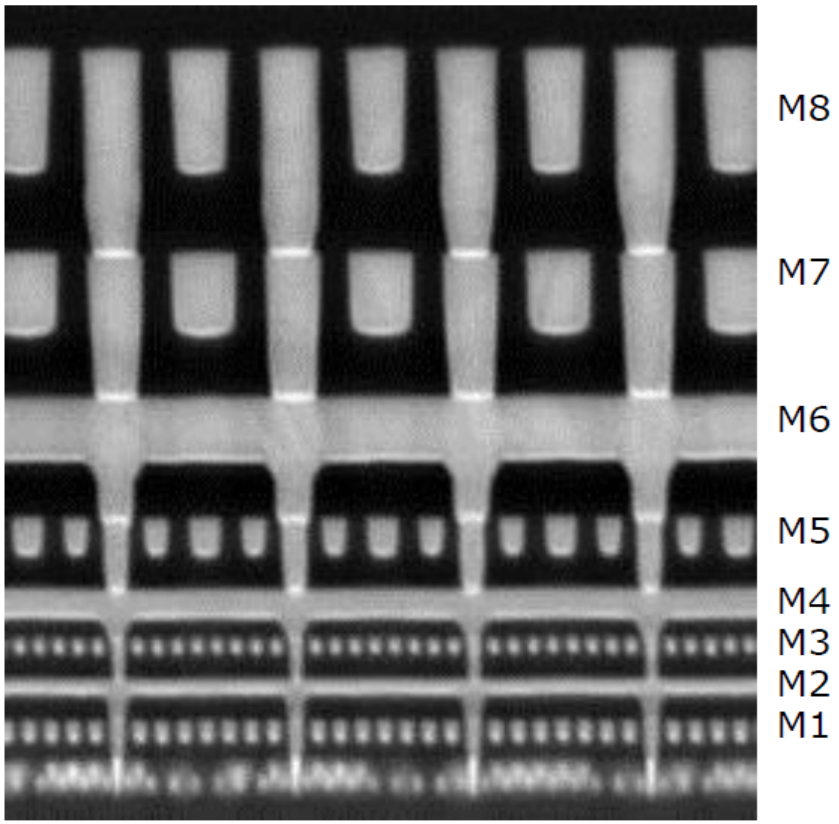
32nm Interconnect



•C.-H. Jan, et al., "A 32nm SoC Platform Technology with 2nd Generation High-k/Metal Gate Transistors Optimized for
•Ultra Low Power, High Performance, and High Density Product Applications", IEDM, Dec 2009.

22nm Interconnect

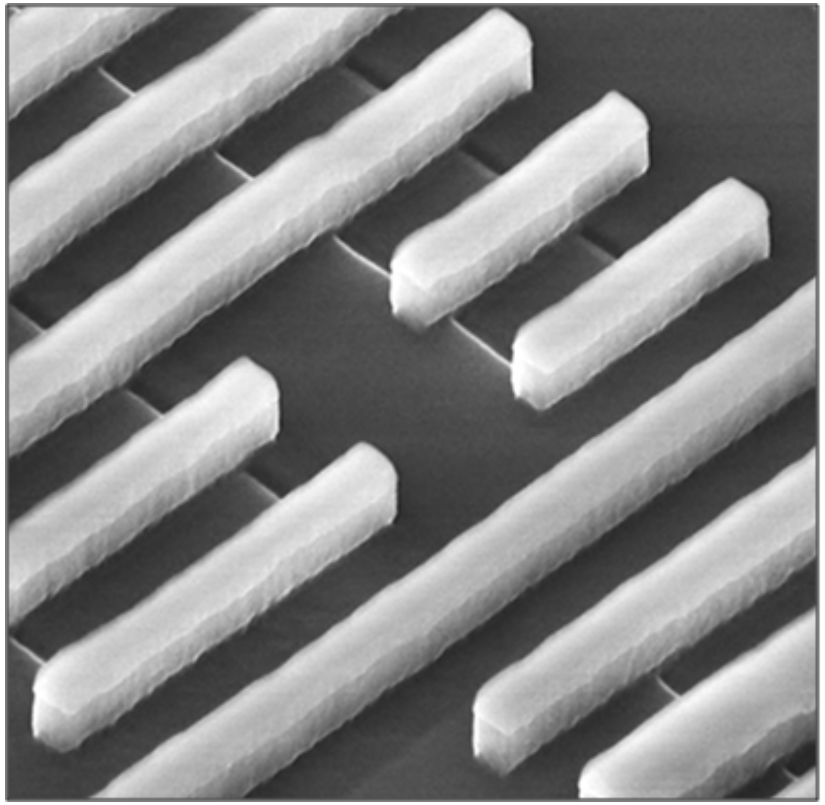
Layer	Pitch
TM	14 um
M8	360 nm
M7	320 nm
M6	240 nm
M5	160 nm
M4	112 nm
M3	80 nm
M2	80 nm
M1	90 nm



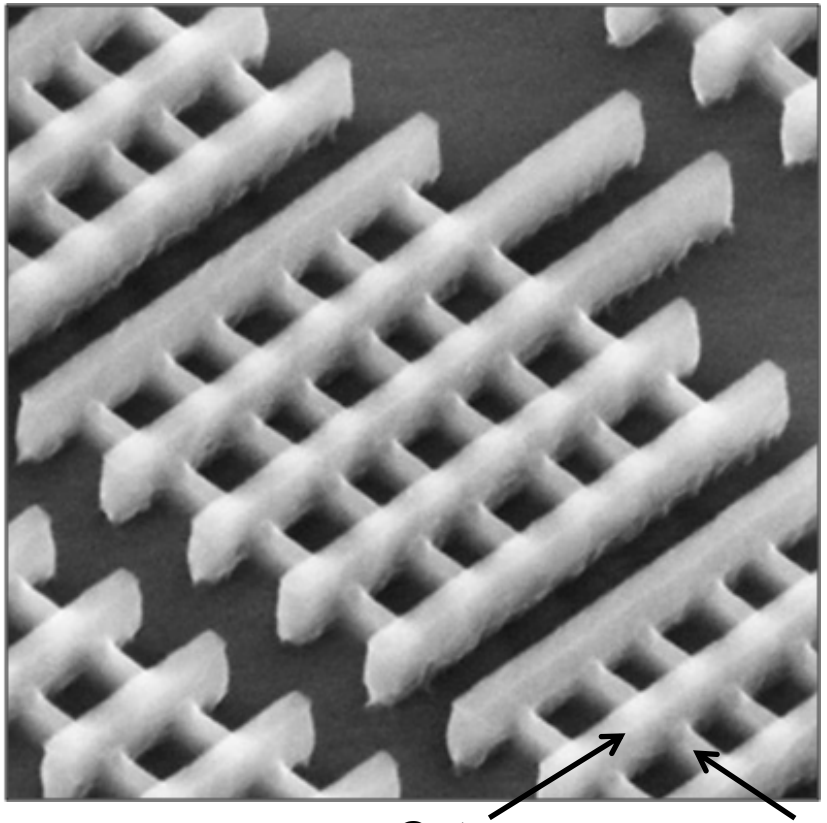
IDF 2012

FIN-FET Transistor Innovation

32 nm Planar Transistors



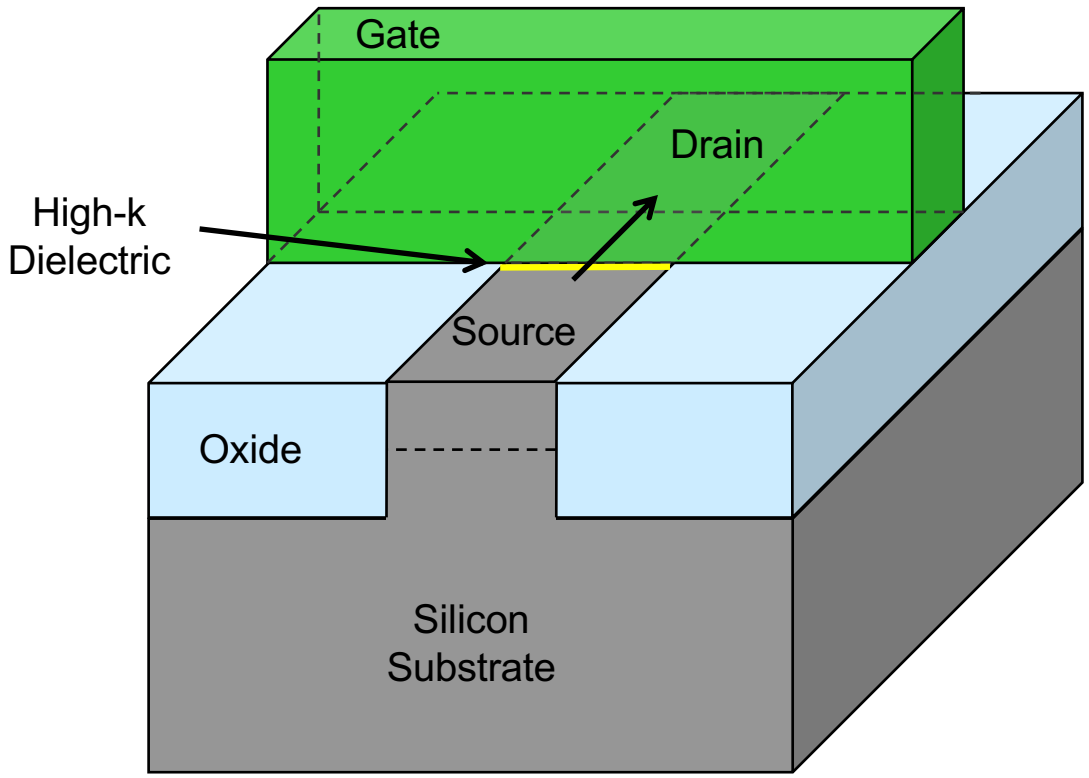
22 nm Tri-Gate Transistors



Intel's 22 nm technology introduces revolutionary 3-D Tri-Gate transistors

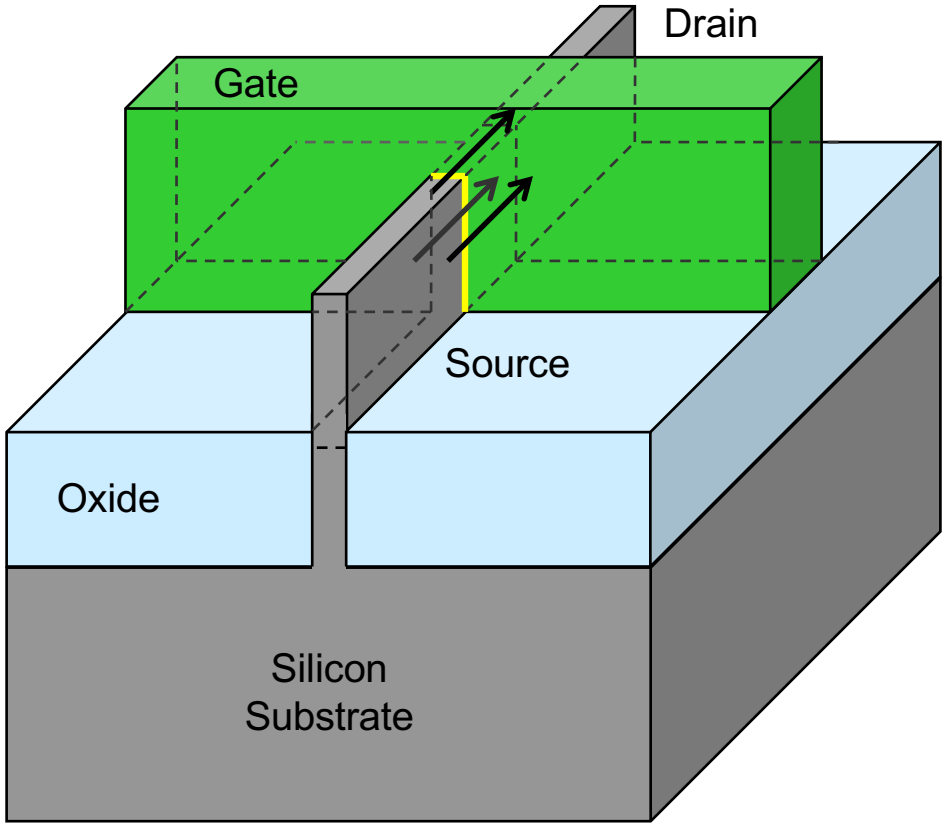
(courtesy: Mark Bohr, Sr. Intel Fellow)

Traditional Planar Transistor



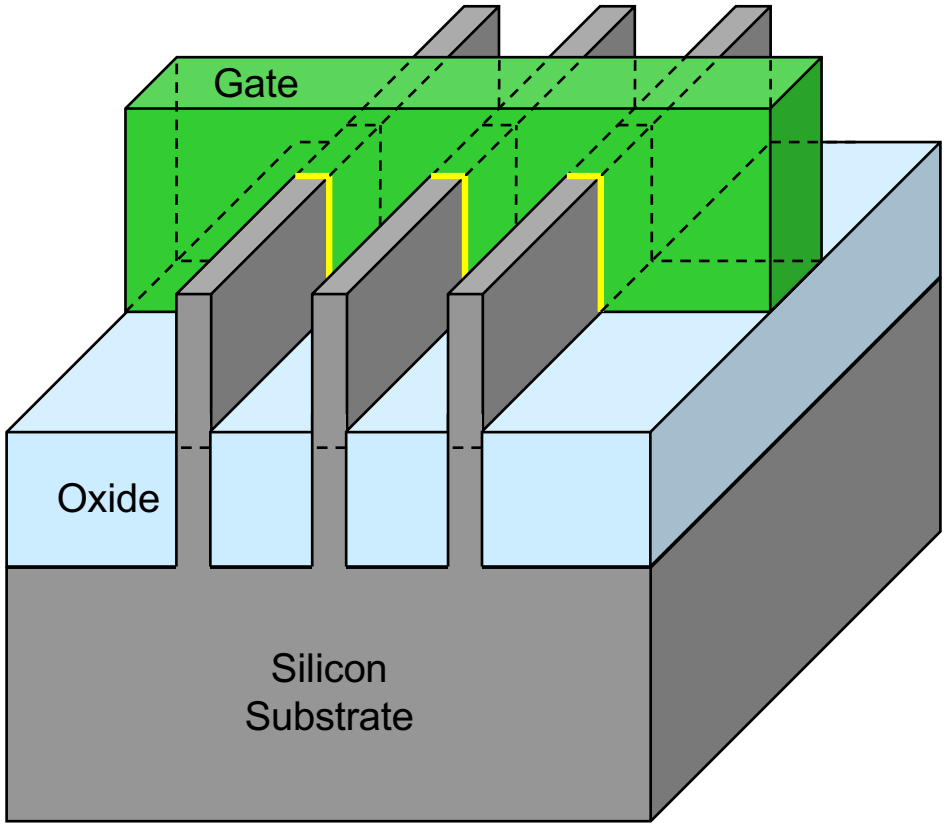
Traditional 2-D planar transistors form a conducting channel on the silicon surface under the gate electrode

22 nm FIN-FET Transistor



3-D Tri-Gate transistors form conducting channels on three sides of a vertical silicon fin

22 nm FIN-FET Transistor



Tri-Gate transistors can connect together multiple fins for higher drive current and higher performance