Lecture 7:
CMOS DC & Transient Response

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Agenda

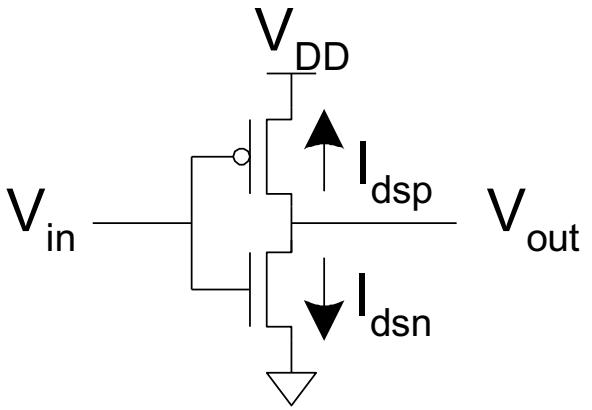
- DC Response
- Logic Levels and Noise Margins
- Transient Response
- Delay Estimation

DC Response

- **DC Response: V_{out} vs. V_{in} for a gate**
- **Ex: Inverter**
  - When $V_{in} = 0$ -> $V_{out} = V_{DD}$
  - When $V_{in} = V_{DD}$ -> $V_{out} = 0$
  - In between, V_{out} depends on transistor size and current
  - By KCL, we know that

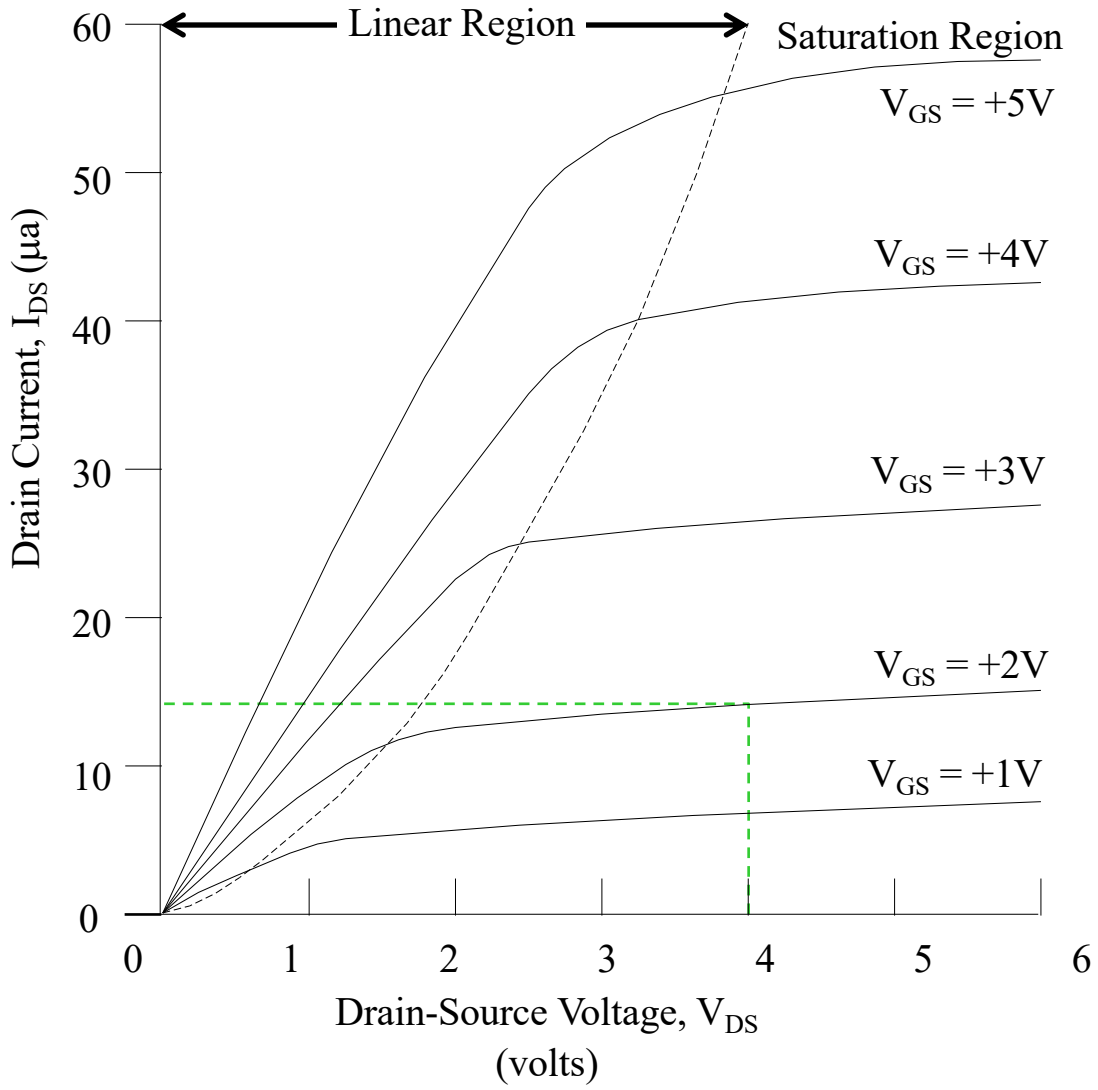
$$I_{dsn} = |I_{dsp}|$$

  - We could solve equations
  - But graphical solution gives more insight



Transistor Operation Review

- Current depends on region of transistor behavior
- For what Vin and Vout are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?

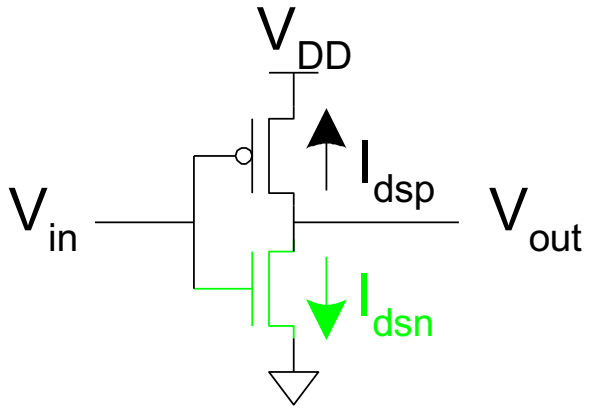


nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

$$V_{gsn} = V_{in}$$

$$V_{dsn} = V_{out}$$



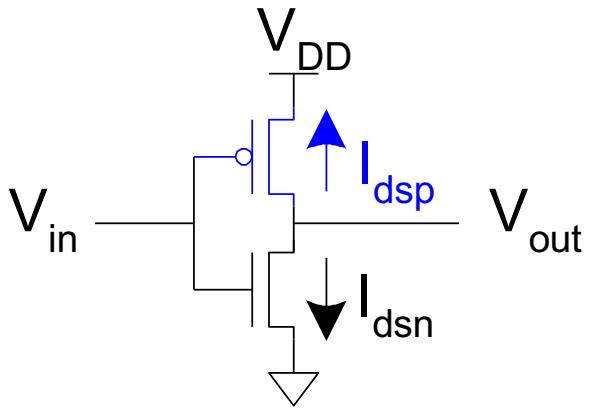
pMOS Operation

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$$V_{gsp} = V_{in} - V_{DD}$$

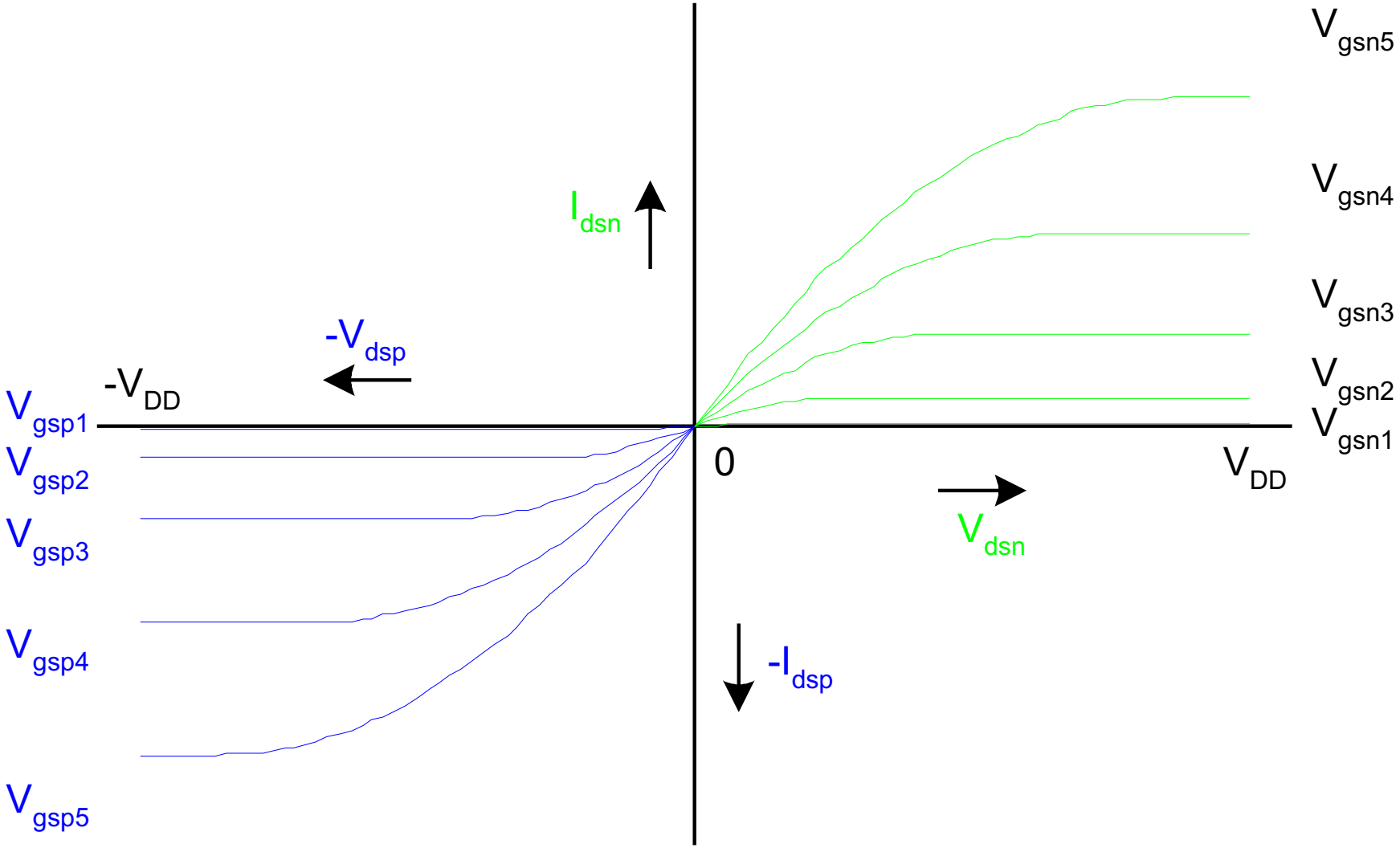
$$V_{dsp} = V_{out} - V_{DD}$$

$$V_{tp} < 0$$

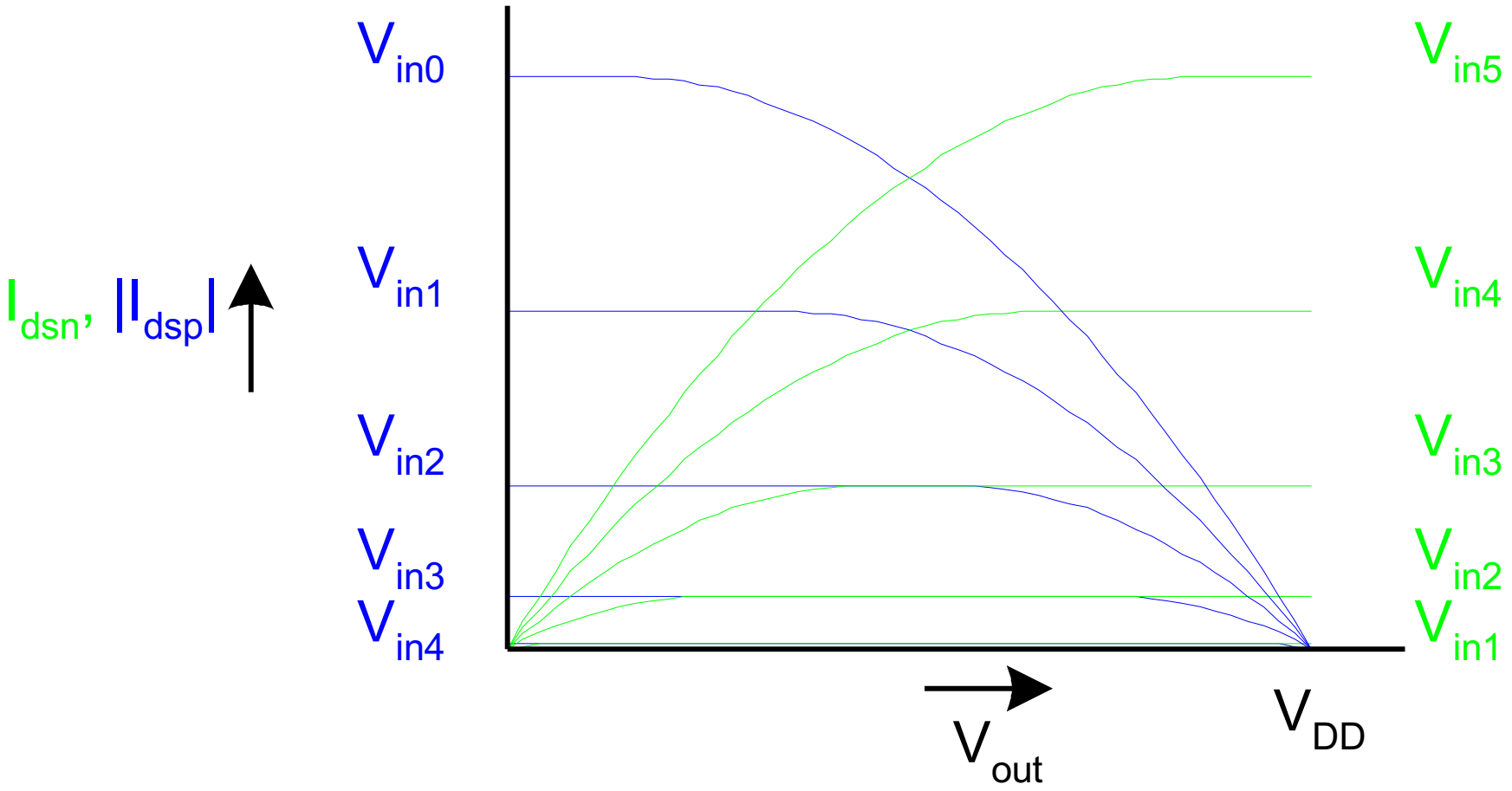


I-V Characteristics

- **Make pMOS wider than nMOS such that βn = βp**

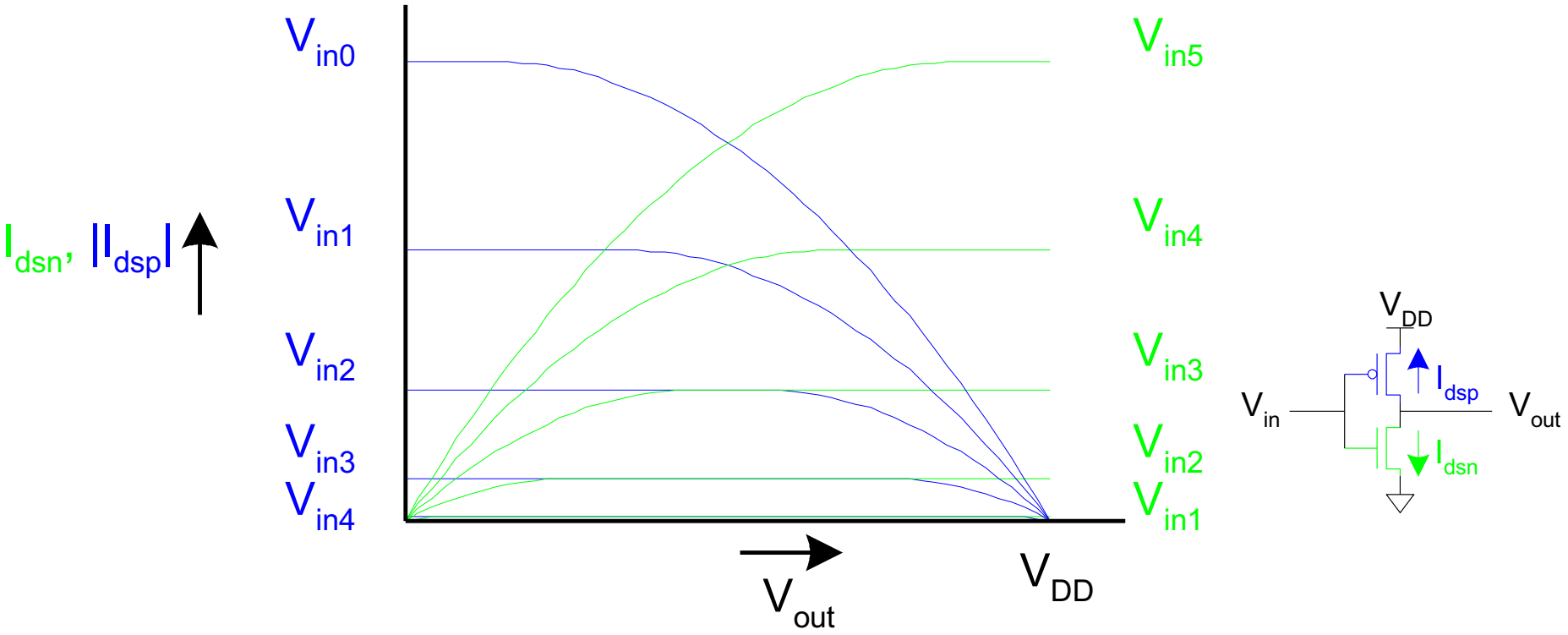


Current vs. Vout, Vin



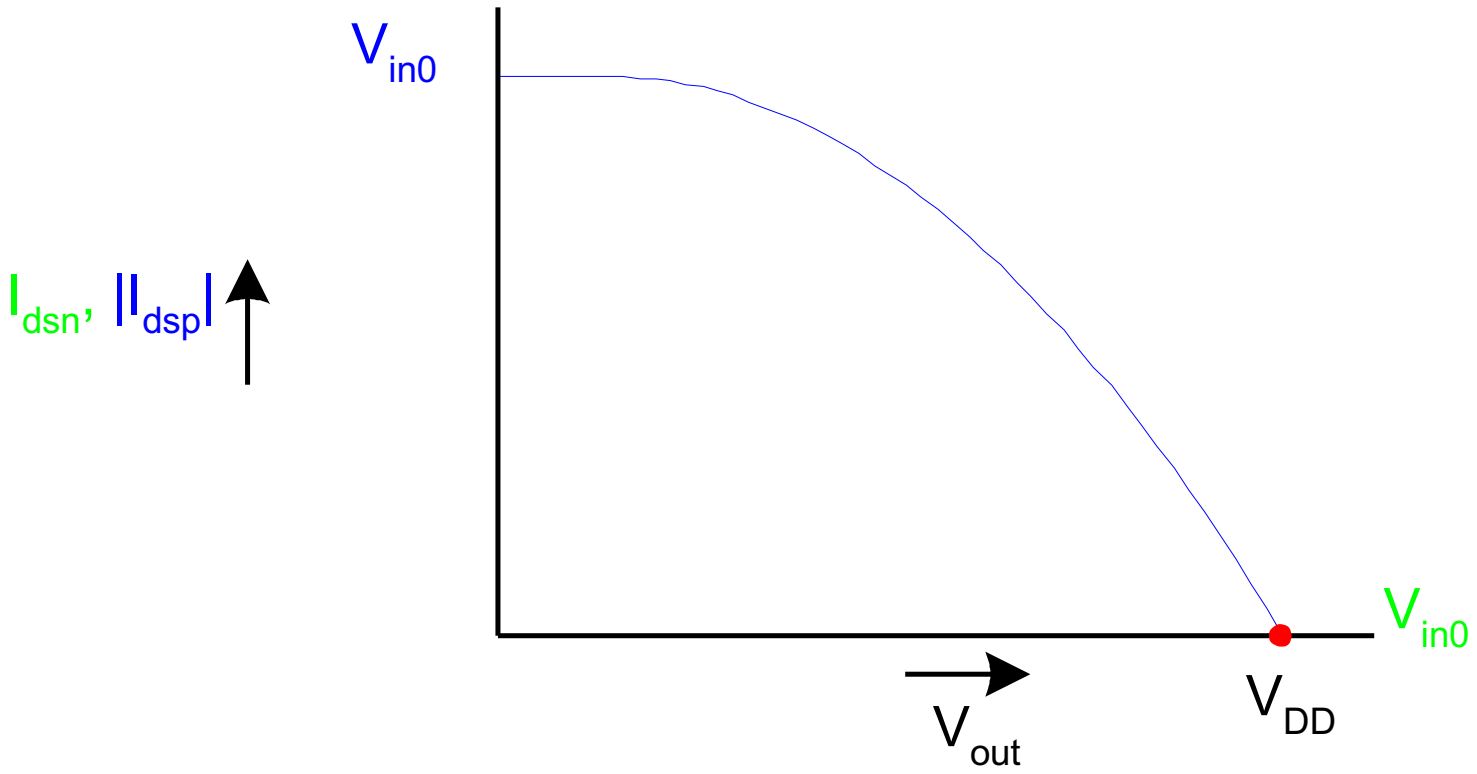
Load Line Analysis

- **For a given V_{in}:**
  - **Plot I_{dsn}, I_{dsp} vs. V_{out}**
  - **V_{out} must be where |currents| are equal**



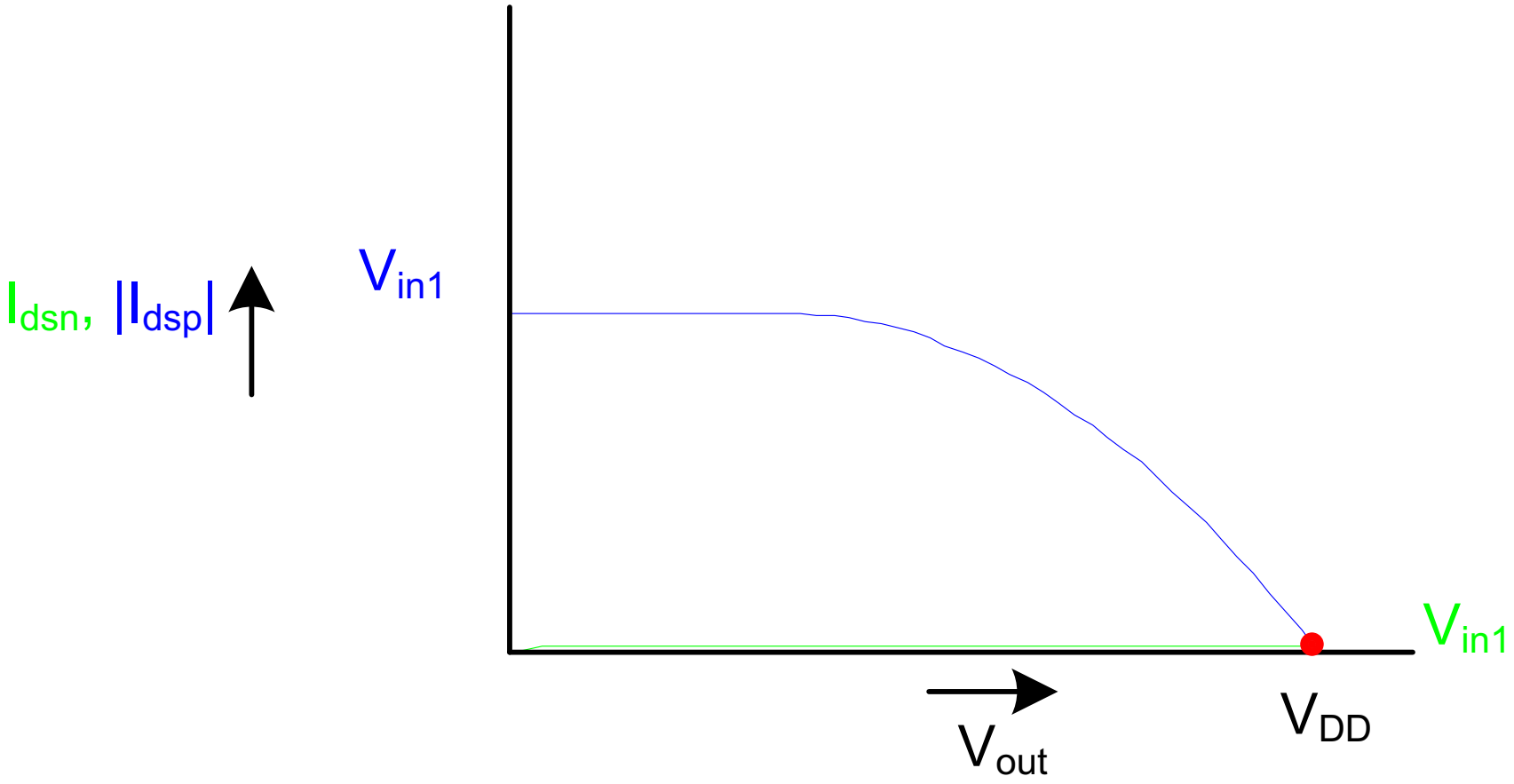
Load Line Analysis

- $V_{in} = 0$



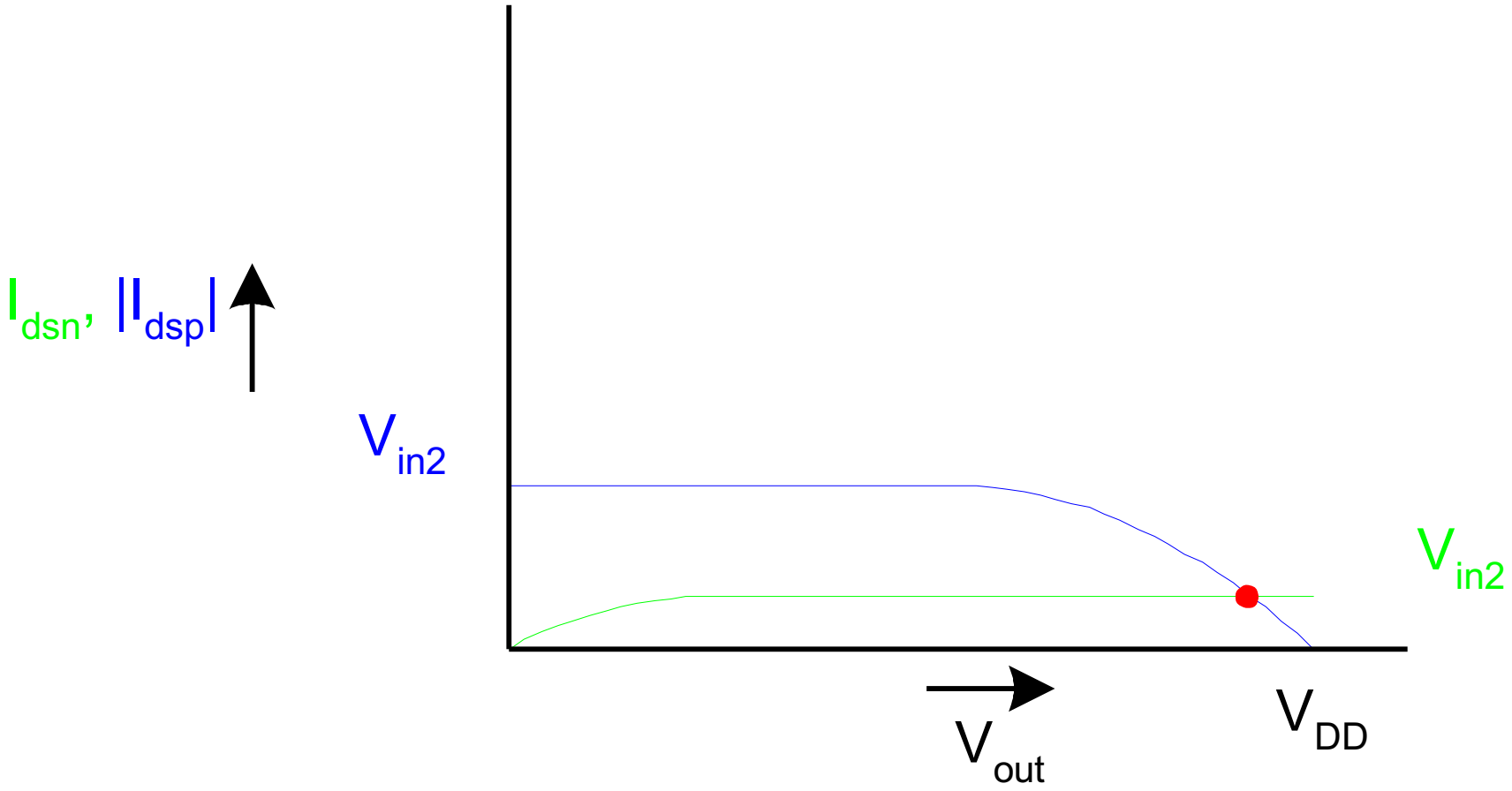
Load Line Analysis

- $V_{in} = 0.2V_{DD}$



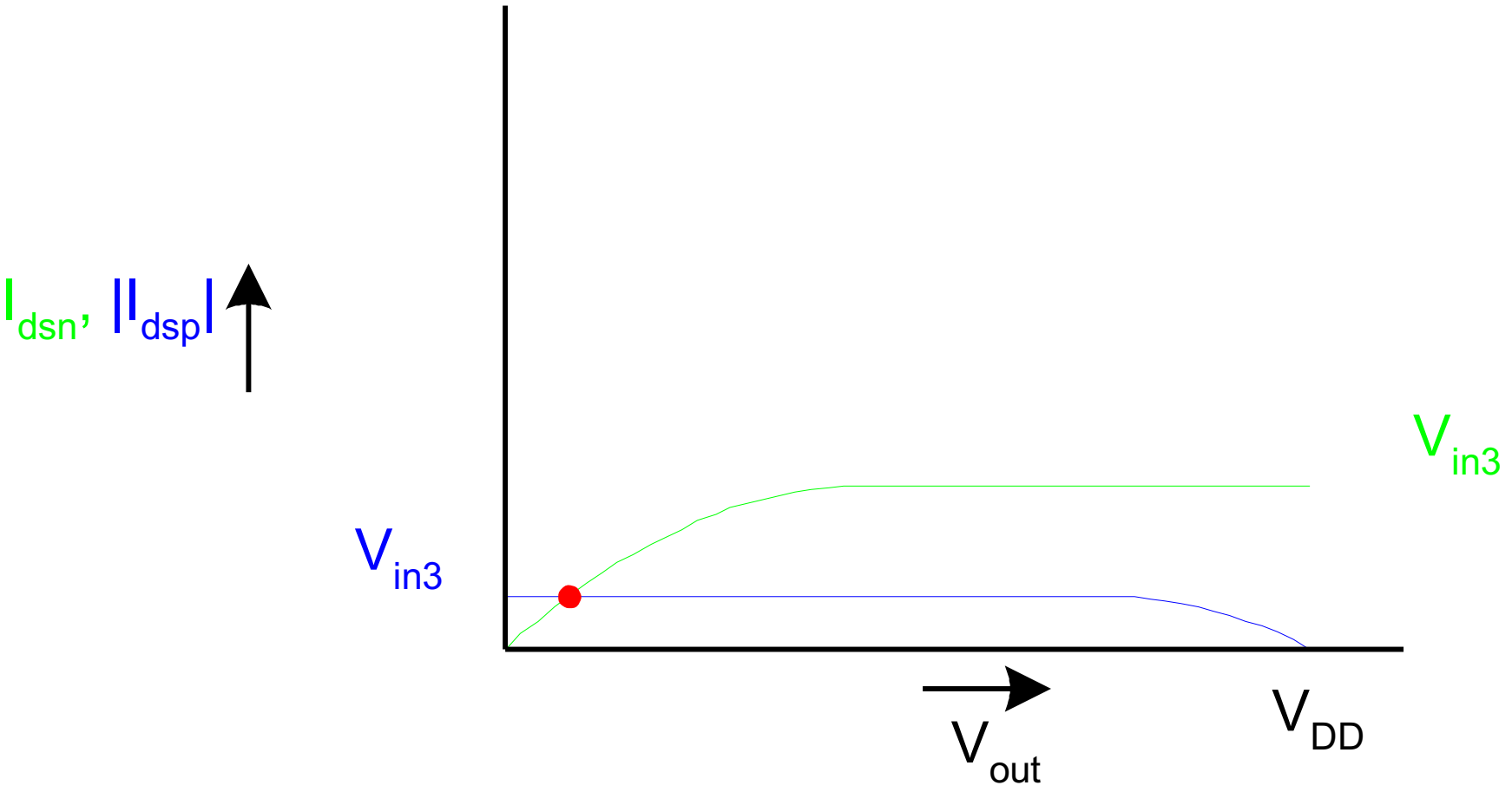
Load Line Analysis

- $V_{in} = 0.4V_{DD}$



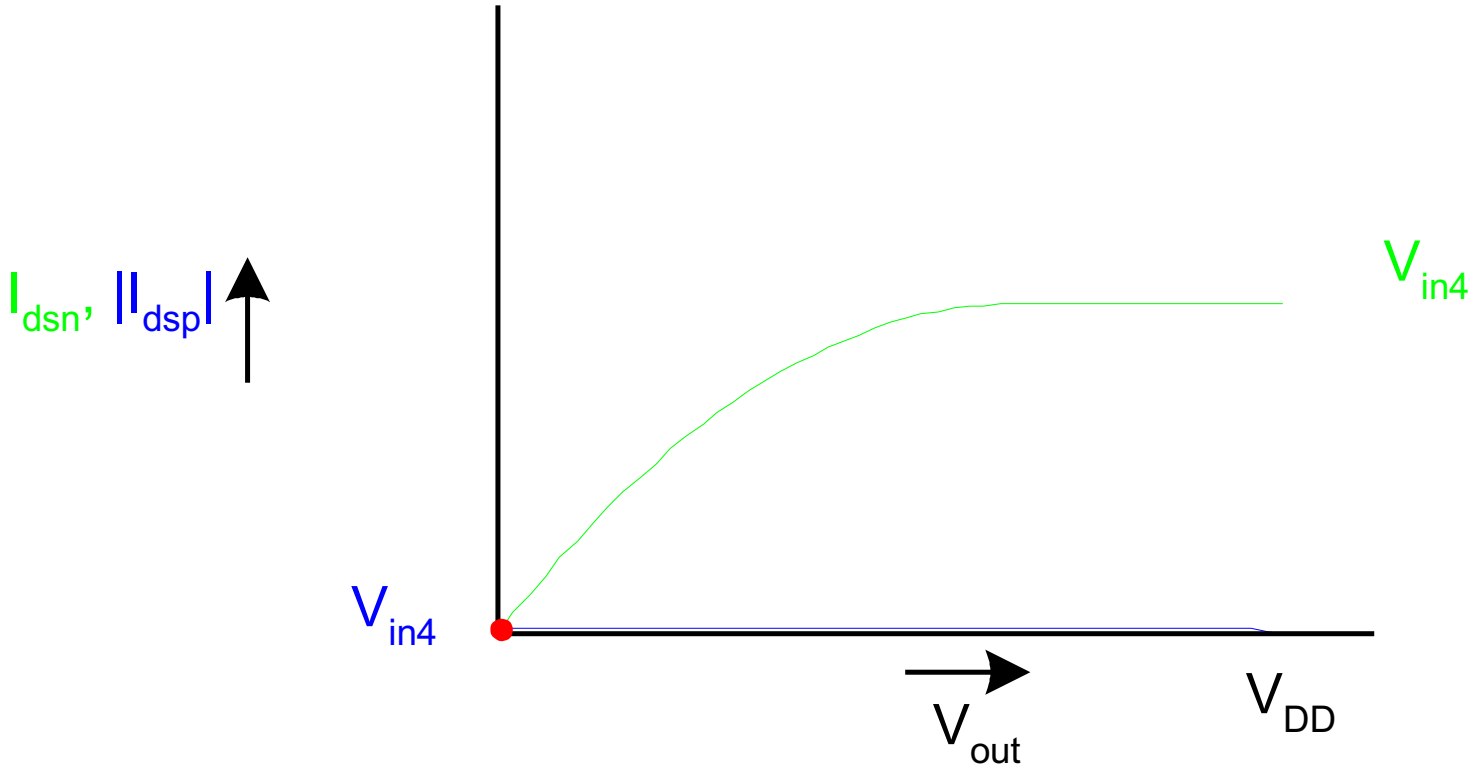
Load Line Analysis

- $V_{in} = 0.6V_{DD}$



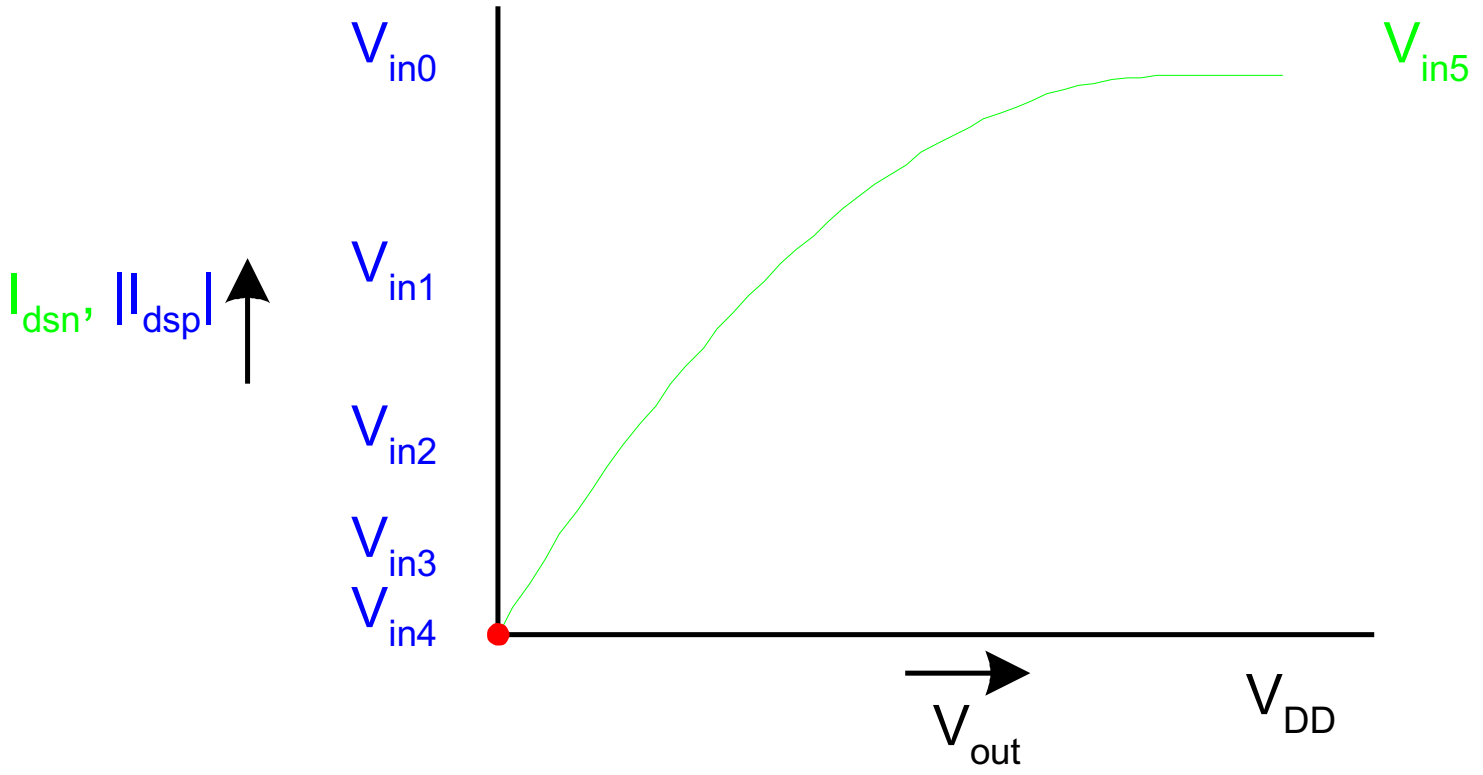
Load Line Analysis

- $V_{in} = 0.8V_{DD}$

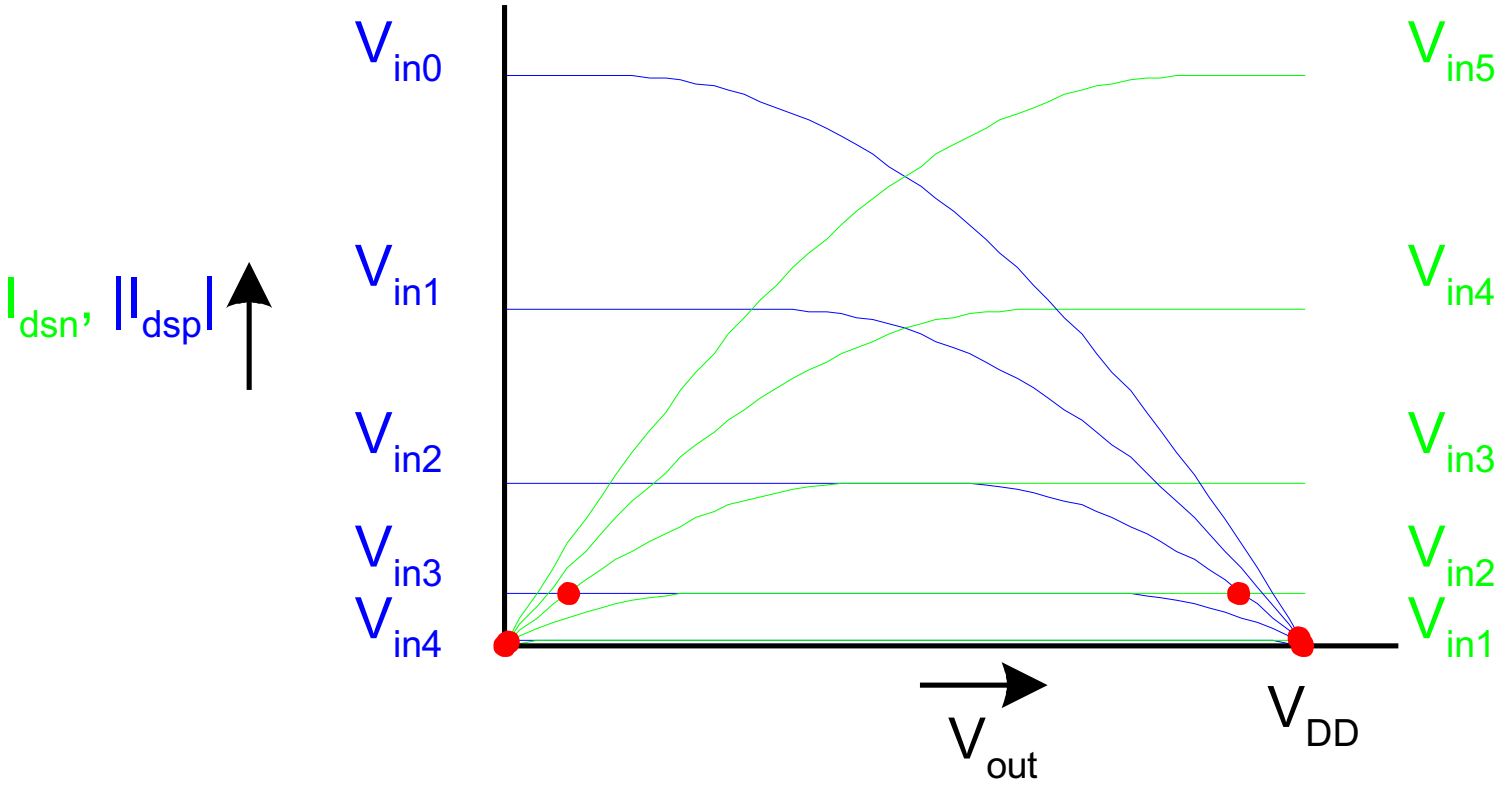


Load Line Analysis

- $V_{in} = V_{DD}$

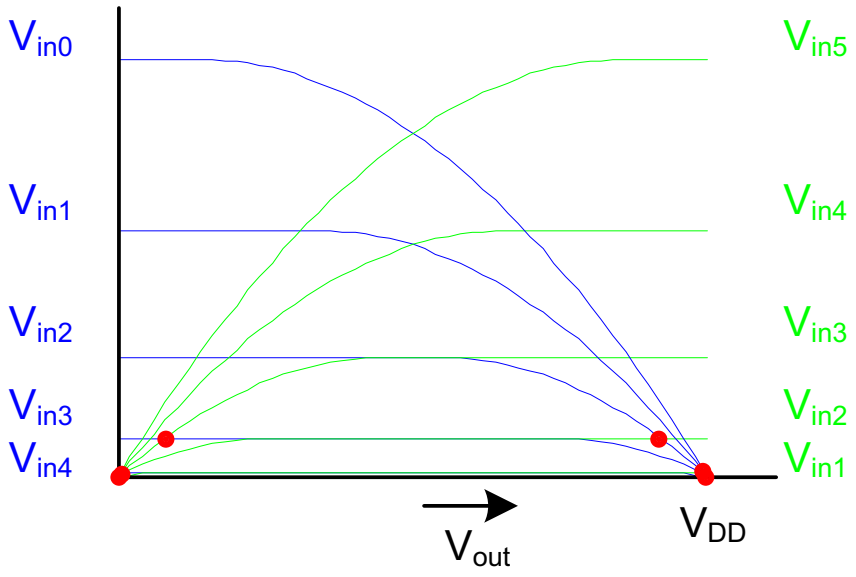


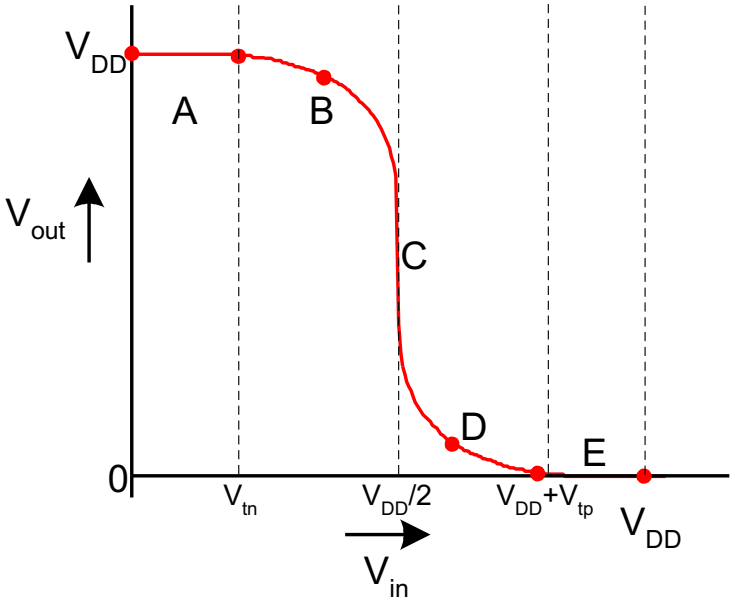
Load Line Summary



DC Transfer Curve

- **Transcribe points onto V_{in} vs. V_{out} plot**

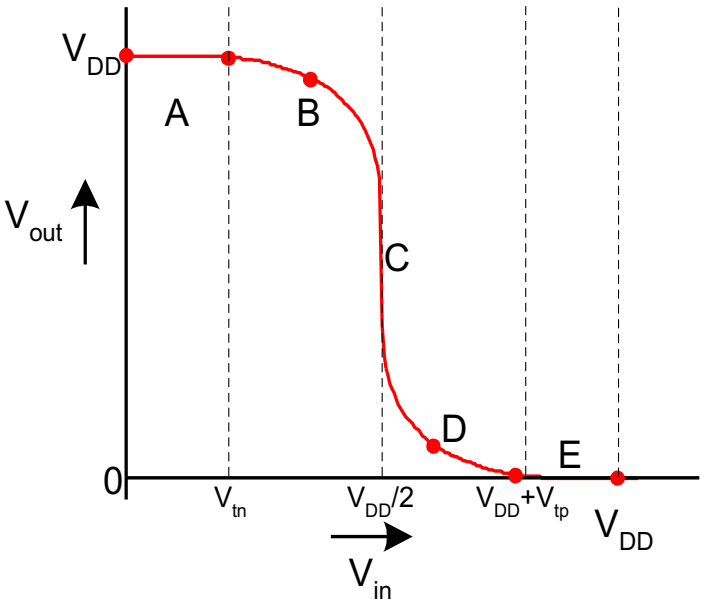




Operating Regions

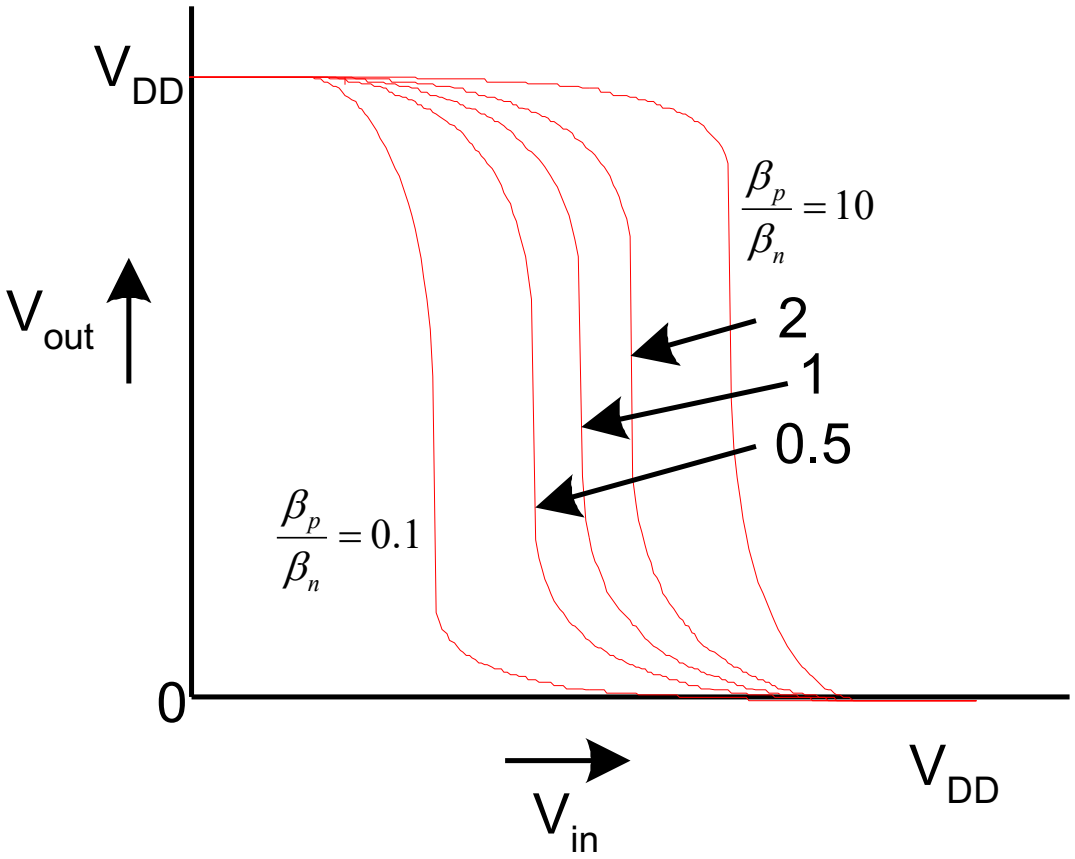
- **Revisit transistor operating regions**

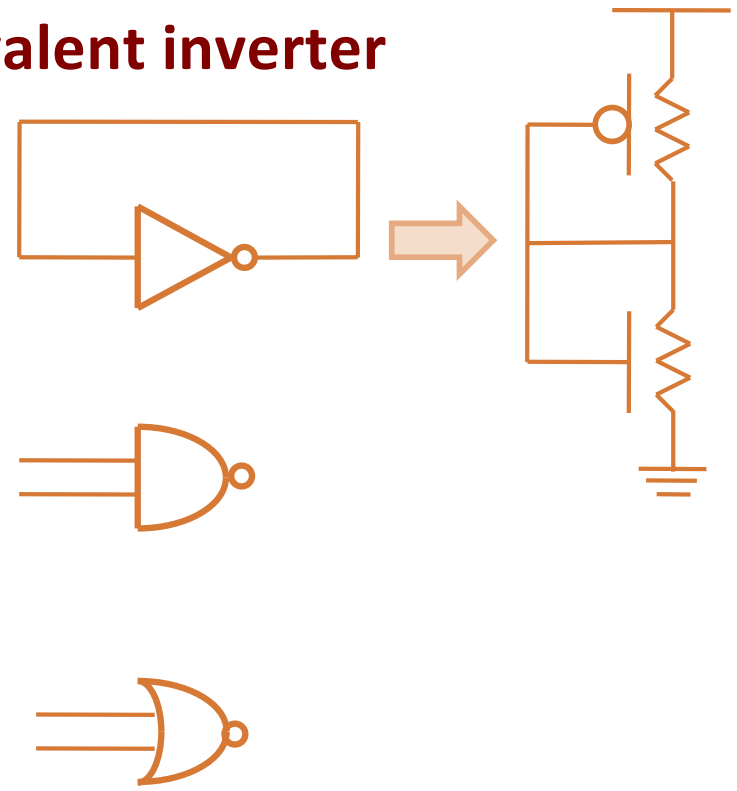
Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff



Beta Ratio

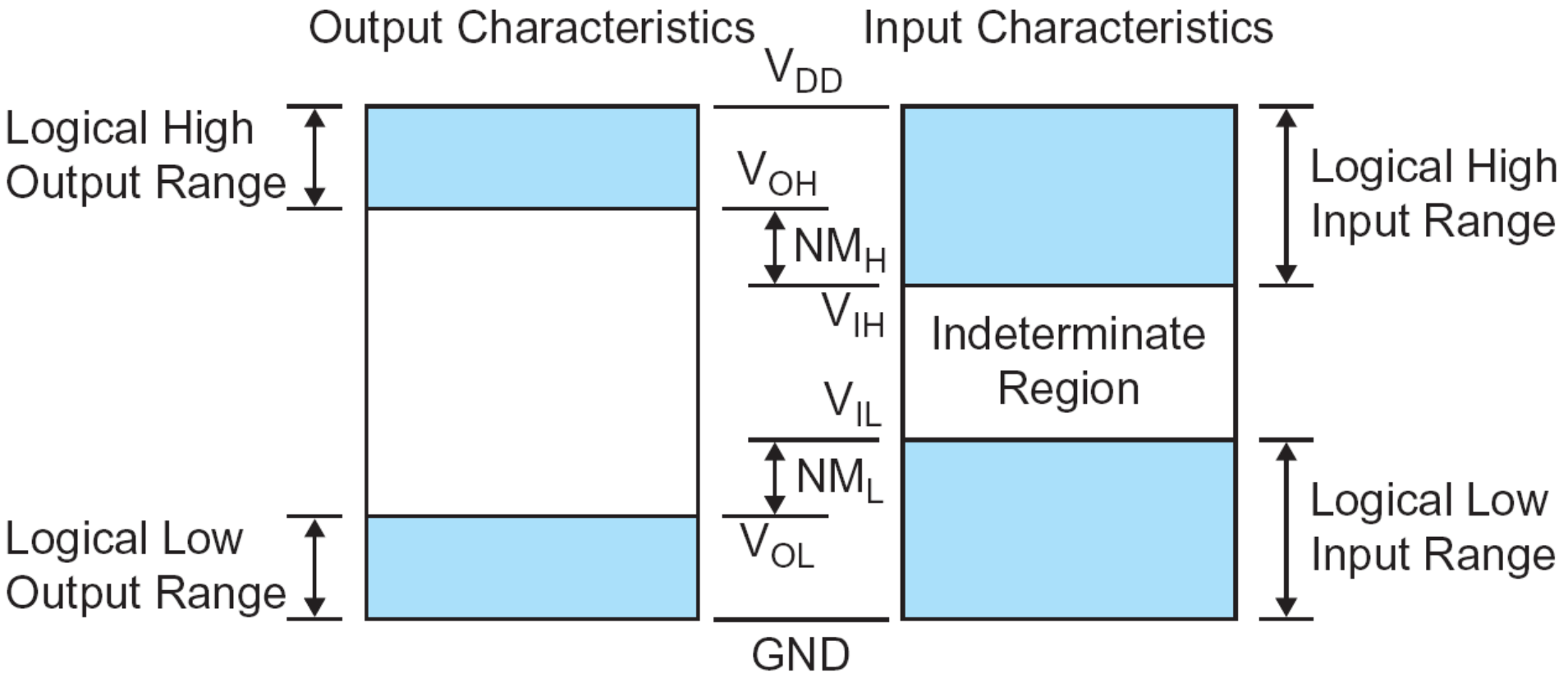
- If $\beta_p / \beta_n \neq 1$, switch point will move from $V_{DD}/2$
- Called a *skewed* gate
- Other gates: decompose into an equivalent inverter





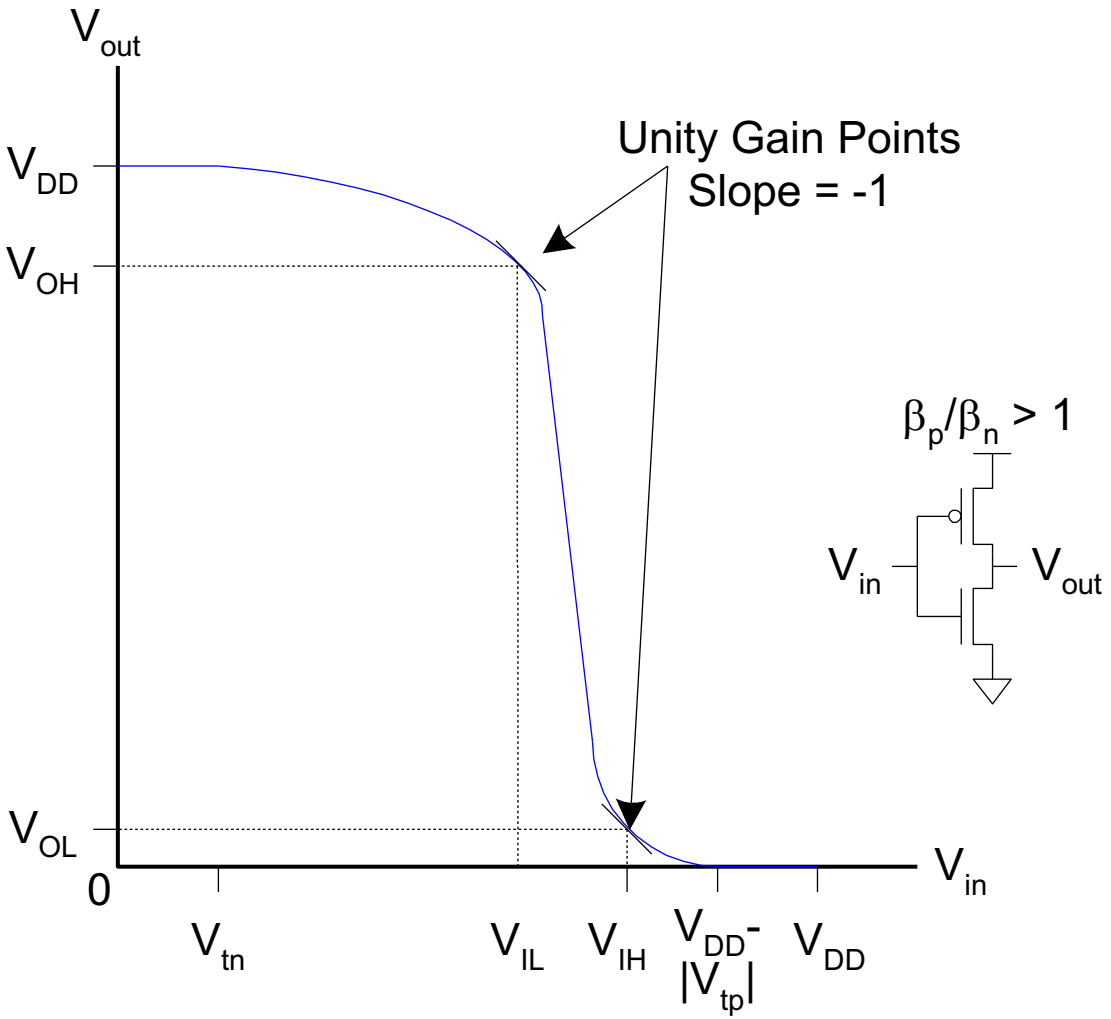
Noise Margins

- **How much noise can a gate input see before it does not recognize the input?**



Logic Levels

- **To maximize noise margins, select logic levels at the unity gain point of DC transfer characteristic**



Transient Response

- ***DC analysis*** **tells us V_{out} if V_{in} is constant**

- ***Transient analysis*** **tells us $V_{out}(t)$ if $V_{in}(t)$ changes**
  - **Requires solving differential equations**

- **Input is usually considered to be a step or ramp**
  - **From 0 to V_{DD} or vice versa**

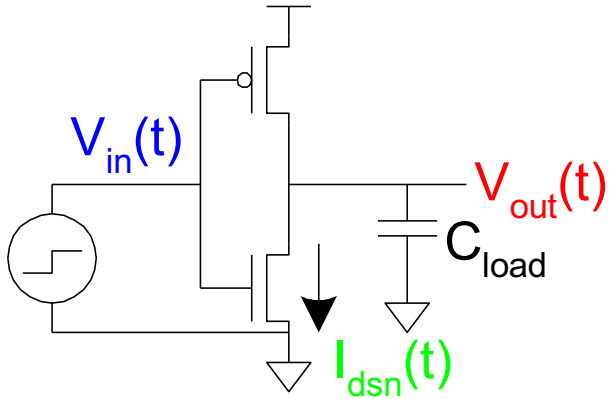
Inverter Step Response

- **Ex: find step response of inverter driving load cap**

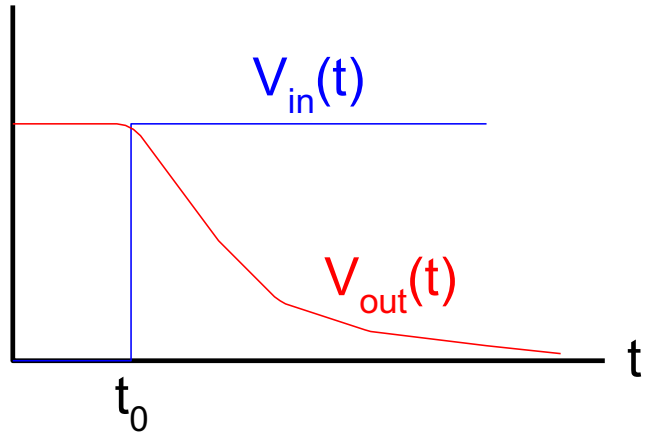
$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}(t)}{dt} = -\frac{I_{dsn}(t)}{C_{load}}$$

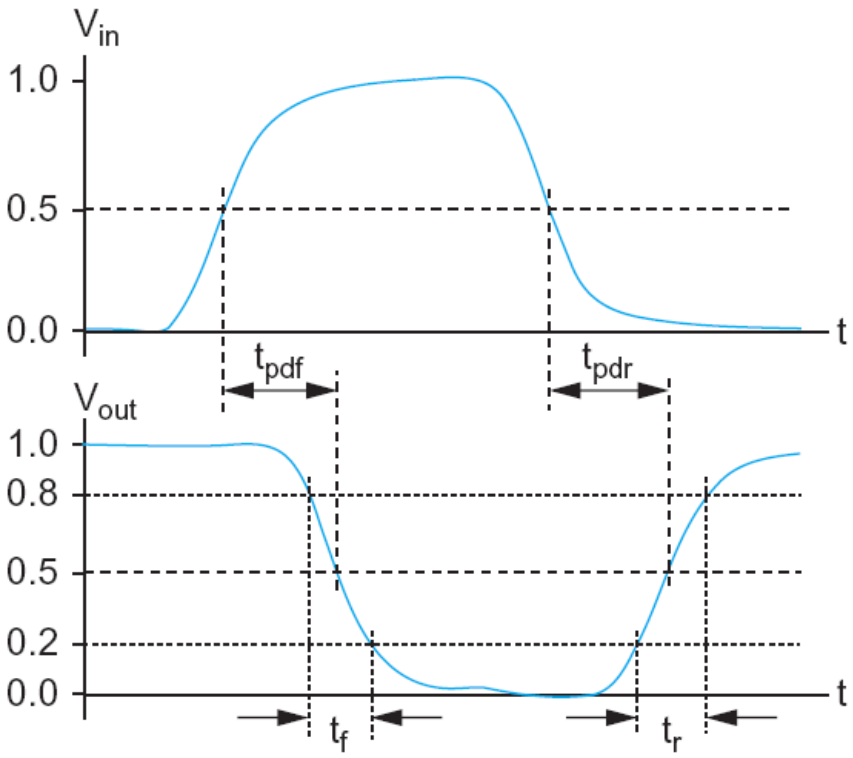


$$I_{dsn}(t) = \begin{cases} 0 & t \le t_0 \\ \frac{\beta}{2}(V_{DD} - V)^2 & V_{out} > V_{DD} - V_t \\ \beta\left(V_{DD} - V_t - V_{out}(t)/2\right)V_{out}(t) & V_{out} < V_{DD} - V_t \end{cases}$$



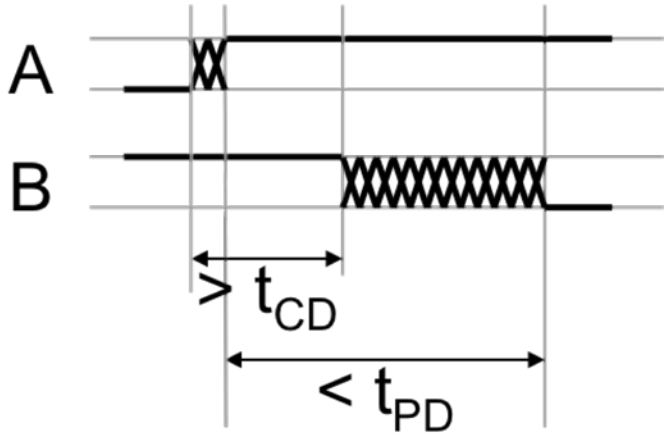
Delay Definitions

- t_{pdr}: *rising propagation delay*
  - Max time from input to rising output crossing $V_{DD}/2$
- t_{pdf}: *falling propagation delay*
  - Max time from input to falling output crossing $V_{DD}/2$
- t_{pd}: *average propagation delay*
  - $t_{pd} = (t_{pdr} + t_{pdf})/2$
- t_r: *rise time*
  - From output crossing 0.2 V_{DD} to 0.8 V_{DD}
- t_f: *fall time*
  - From output crossing 0.8 V_{DD} to 0.2 V_{DD}



Delay Definitions

- t_{cdr}: *rising contamination delay*
  - Minimum time from input to rising output crossing $V_{DD}/2$
- t_{cdf}: *falling contamination delay*
  - Minimum time from input to falling output crossing $V_{DD}/2$
- t_{cd}: *average contamination delay*
  - $t_{pd} = (t_{cdr} + t_{cdf})/2$



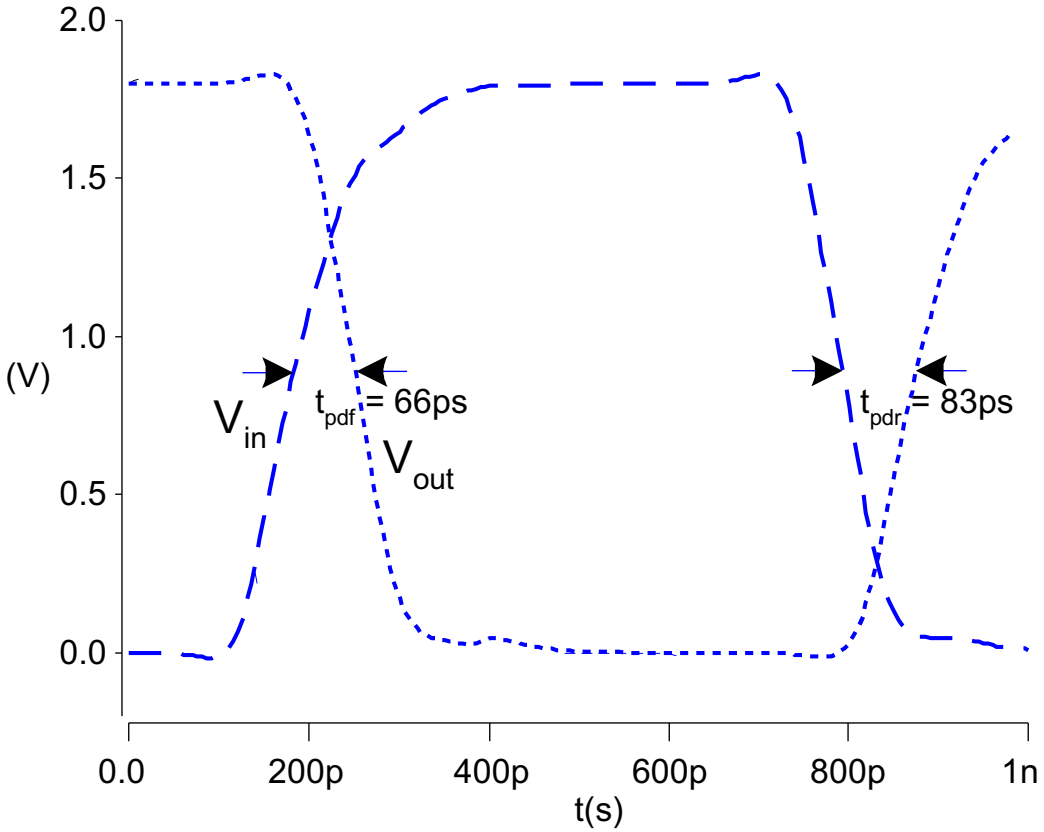
NOTE:

Contamination delay **is not the same thing as** ***minimum delay. It*** **is the minimum amount of time from an input signal change to an output signal change**

Minimum delay **- is the minimum amount of time from an input signal change (to its correct value) to an output signal taking on its correct value (t_{pd})**

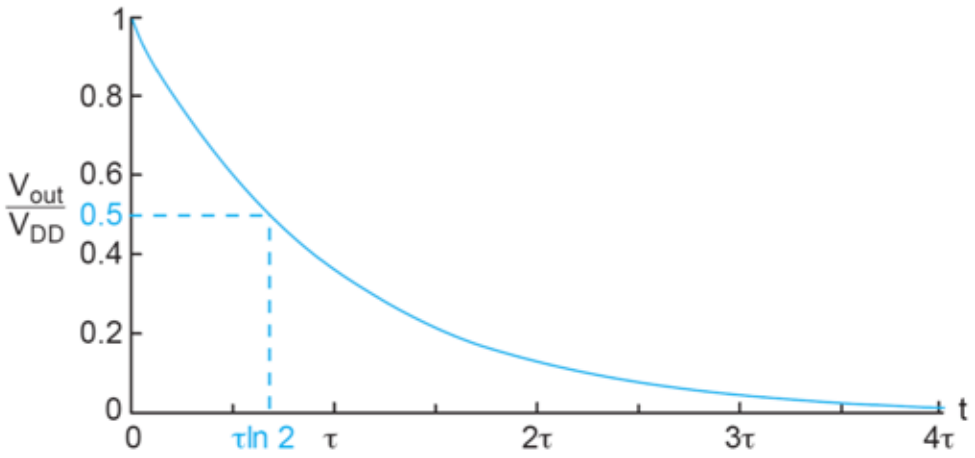
Simulated Inverter Delay

- Solving differential equations by hand too hard
- SPICE simulator solves equations numerically
  - Uses more accurate I-V models too!
  - But simulations can take a long time to run



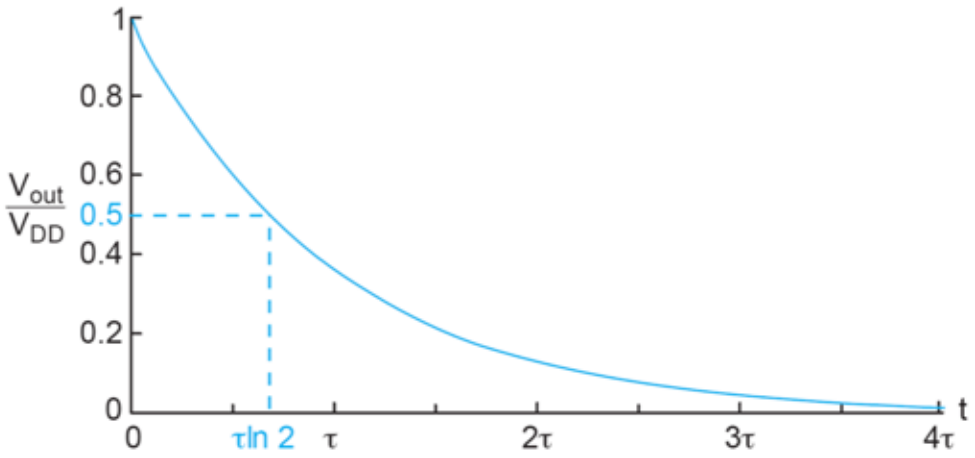
Delay Estimation

- We would like to be able to easily estimate delay
  - Not as accurate as simulation
  - But easier to ask "What if?"
- The step response usually looks like a 1st order RC response with a decaying exponential.
- Use RC delay models to estimate delay
  - C = total capacitance on output node
  - Use effective resistance R
  - So that tpd = $R_{eff}C$



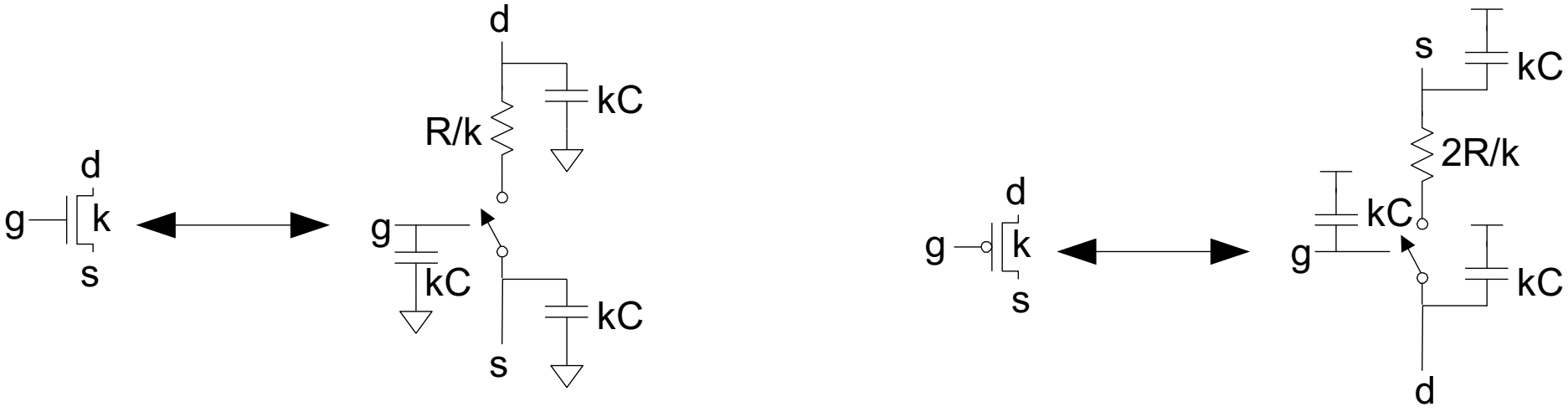
Effective Resistance

- **Shockley models have limited value**
  - Not accurate enough for modern transistors
  - Too complicated for much hand analysis
- **Simplification: treat transistor as resistor**
  - Replace Ids(Vds, Vgs) with effective resistance R
    - Ids = Vds/R
  - R averaged across switching of digital gate
- **Too inaccurate to predict current at any given time**
  - But good enough to predict RC delay



RC Delay Models

- **Use equivalent circuits for MOS transistors**
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance R, capacitance C
  - Unit pMOS has resistance 2R, capacitance C
- **Capacitance proportional to width**
- **Resistance inversely proportional to width**

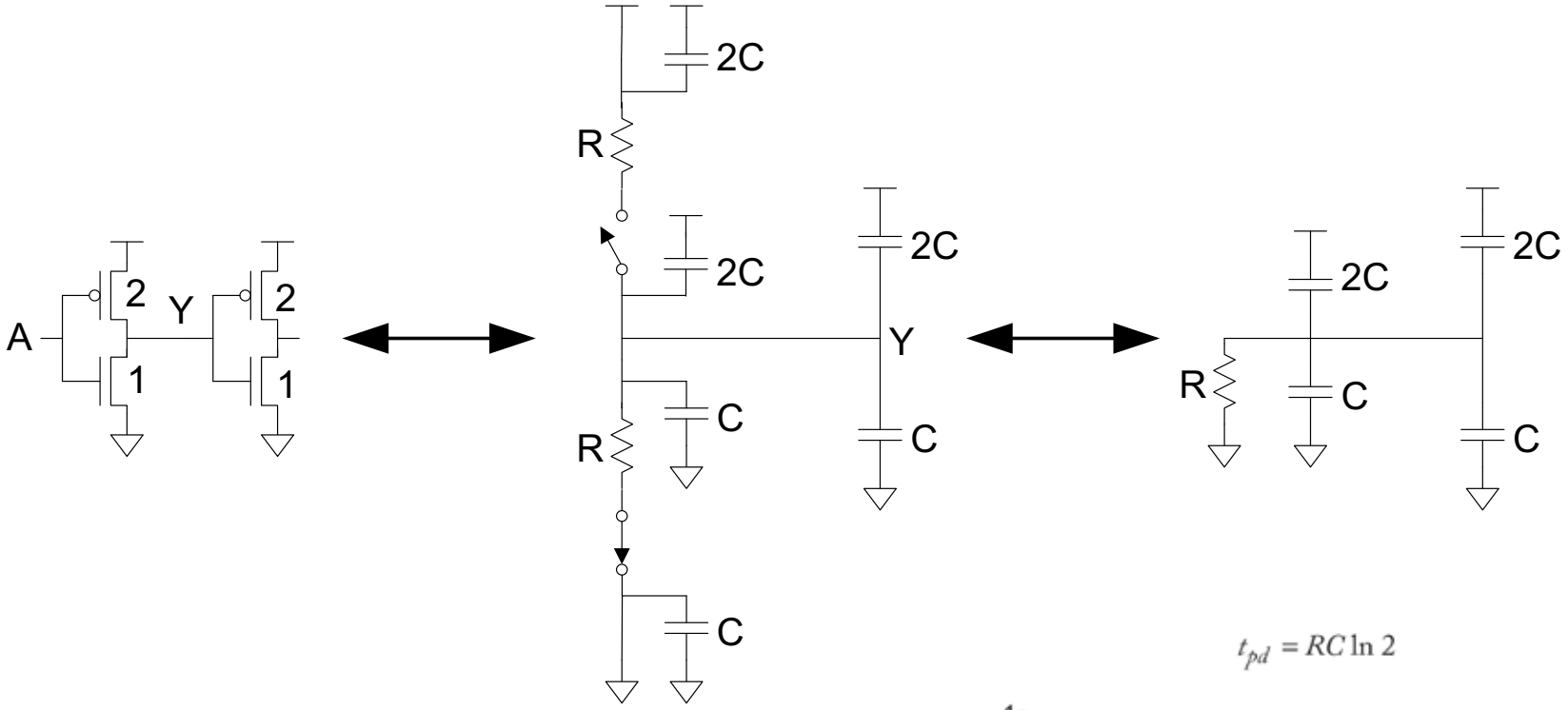


RC Values

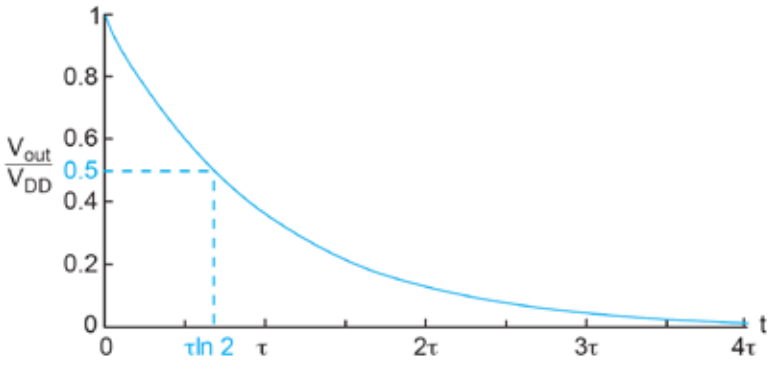
- **Capacitance**
  - C = Cg = Cs = Cd = 2 fF/µm of gate width for technology scaled devices
- **Resistance**
  - R ≈ 10 KΩ•µm in 0.6 µm process
  - Improves with shorter channel lengths
  - 1.25 KΩ•µm in 65 nm process
- **Unit transistors**
  - May refer to minimum contacted device (4/2 λ)
  - Or maybe 1 µm wide device
  - Doesn't matter as long as you are consistent

Inverter Delay Estimate

- **Estimate the delay of a fanout-of-1 inverter**

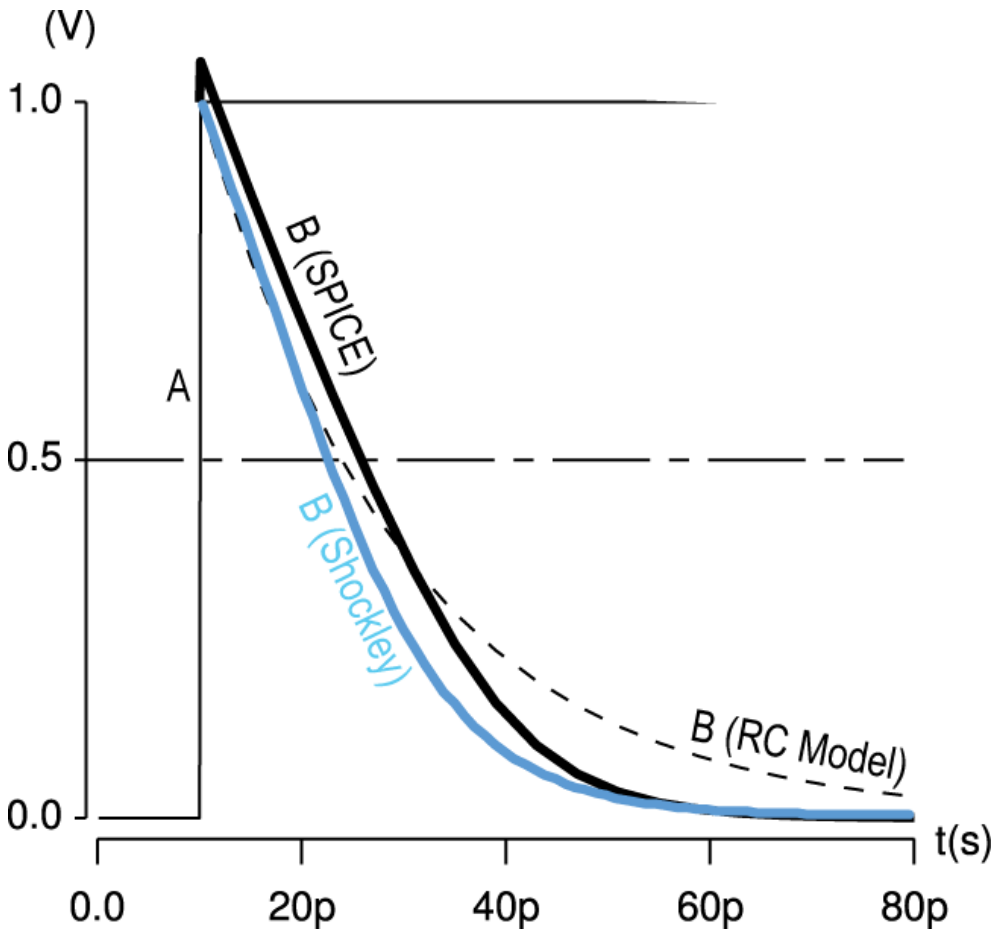


$$t_{pd} = RC \ln 2$$



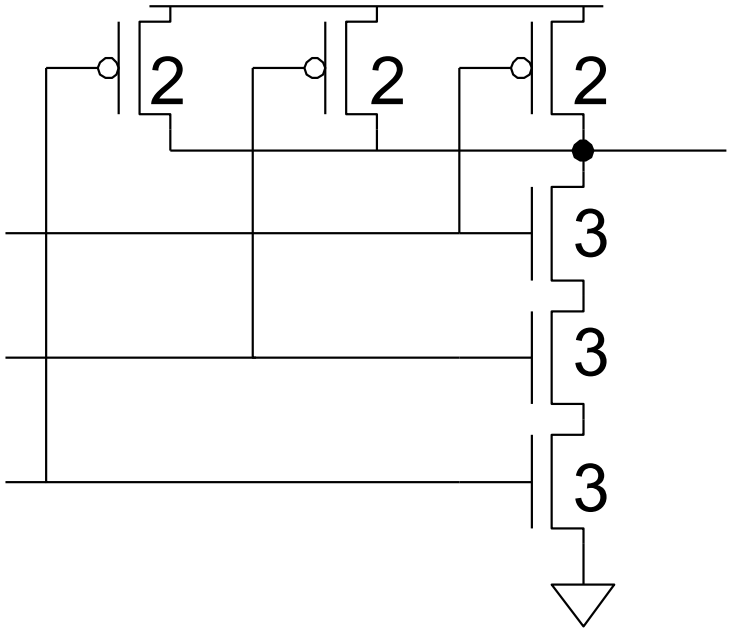
$d = R_{eff} * 6C$

Delay Model Comparison



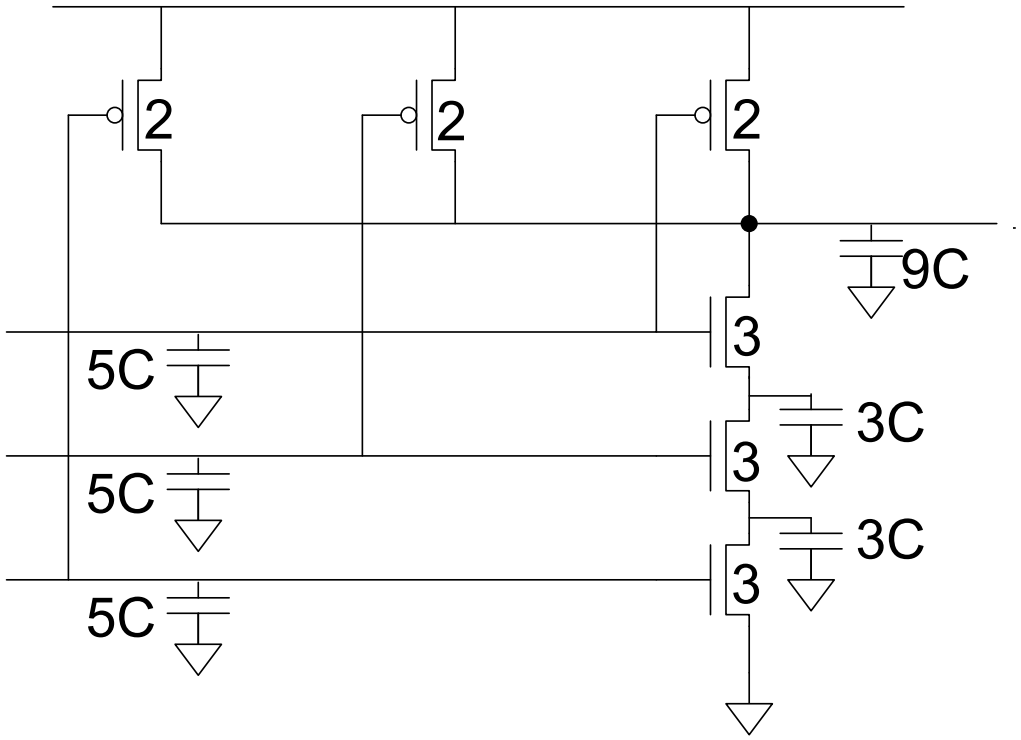
Example: 3-input NAND

- **Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).**
  - **Assume βp = ½βn**



3-input NAND Caps

- **Annotate the 3-input NAND gate with gate and diffusion capacitance.**

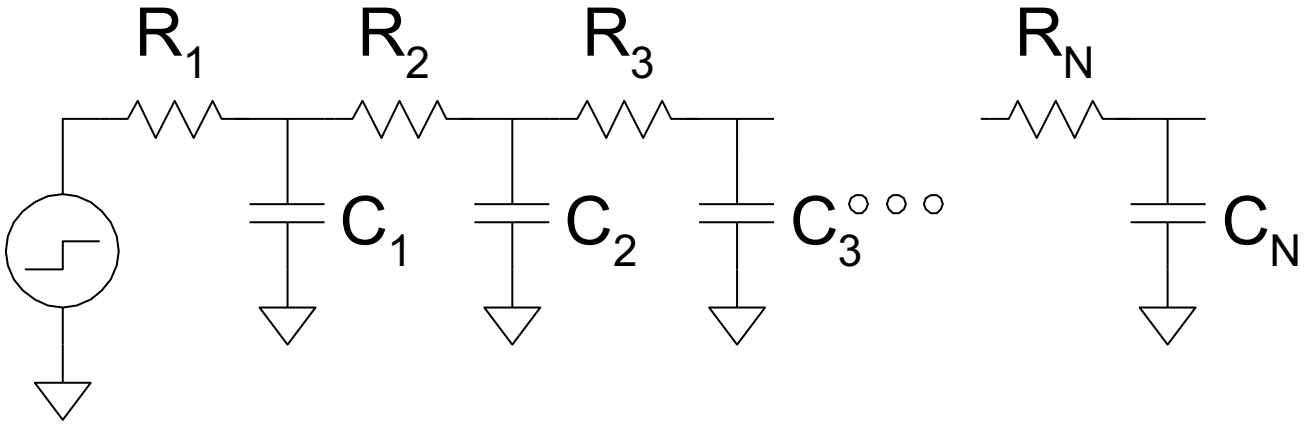


Elmore Delay

- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC ladder*
- Elmore delay of RC ladder

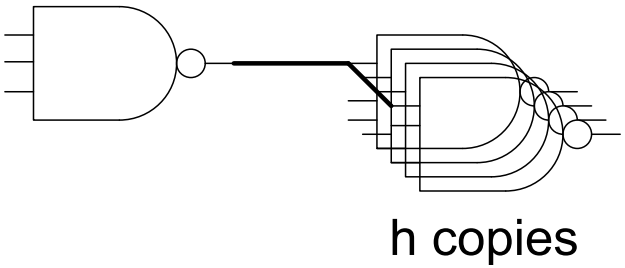
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

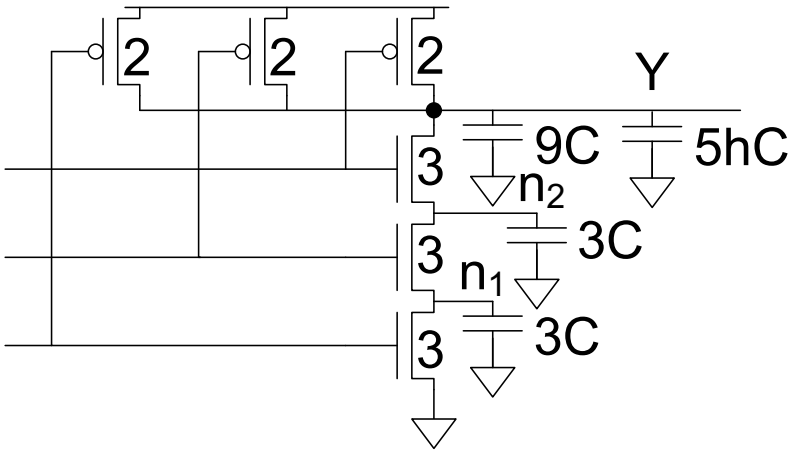
$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$

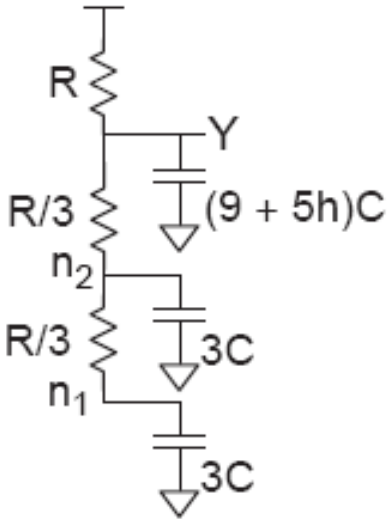


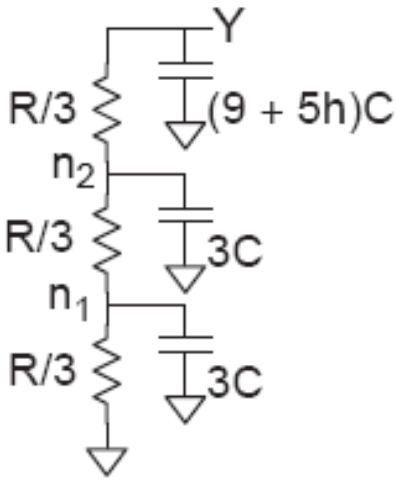
Fanout Example: 3-input NAND

- **Estimate worst-case rising and falling delay of 3-input NAND driving *h* identical gates.**







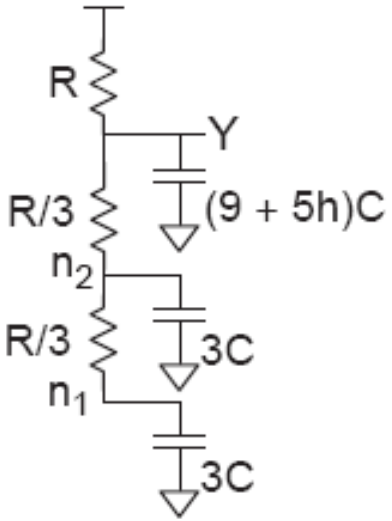


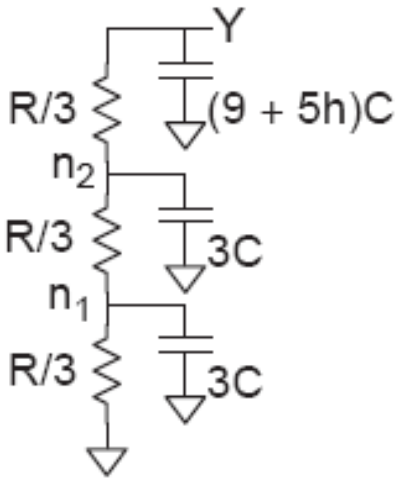
$$t_{pdr} = (9+5h)RC$$

$$t_{pdf} = (3C)\left(\tfrac{R}{3}\right) + (3C)\left(\tfrac{R}{3}+\tfrac{R}{3}\right) + \left[(9+5h)C\right]\left(\tfrac{R}{3}+\tfrac{R}{3}+\tfrac{R}{3}\right)$$
$$= (12+5h)RC$$

Delay Components

- **Delay has two parts**
  - **Parasitic delay**
    - **9 or 12 RC**
    - **Independent of load**
  - **Effort delay**
    - **5h RC**
    - **Proportional to load capacitance**



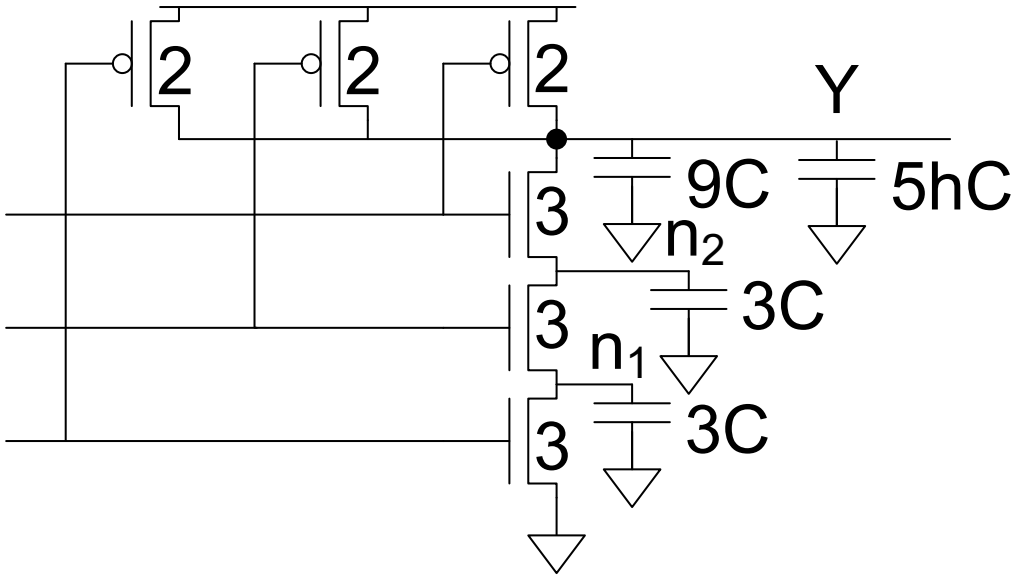


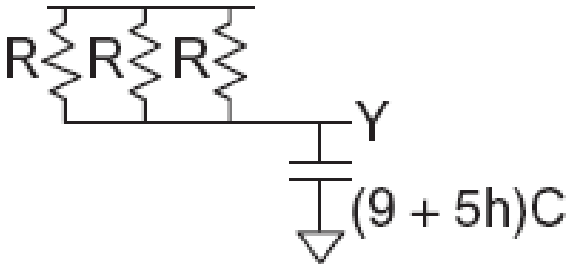
$$t_{pdr} = (9+5h)RC$$

$$t_{pdf} = (3C)\left(\tfrac{R}{3}\right) + (3C)\left(\tfrac{R}{3}+\tfrac{R}{3}\right) + \left[(9+5h)C\right]\left(\tfrac{R}{3}+\tfrac{R}{3}+\tfrac{R}{3}\right)$$
$$= (12+5h)RC$$

Contamination Delay

- Best-case (contamination) delay can be substantially less than propagation delay.
- Ex: If all three inputs fall simultaneously

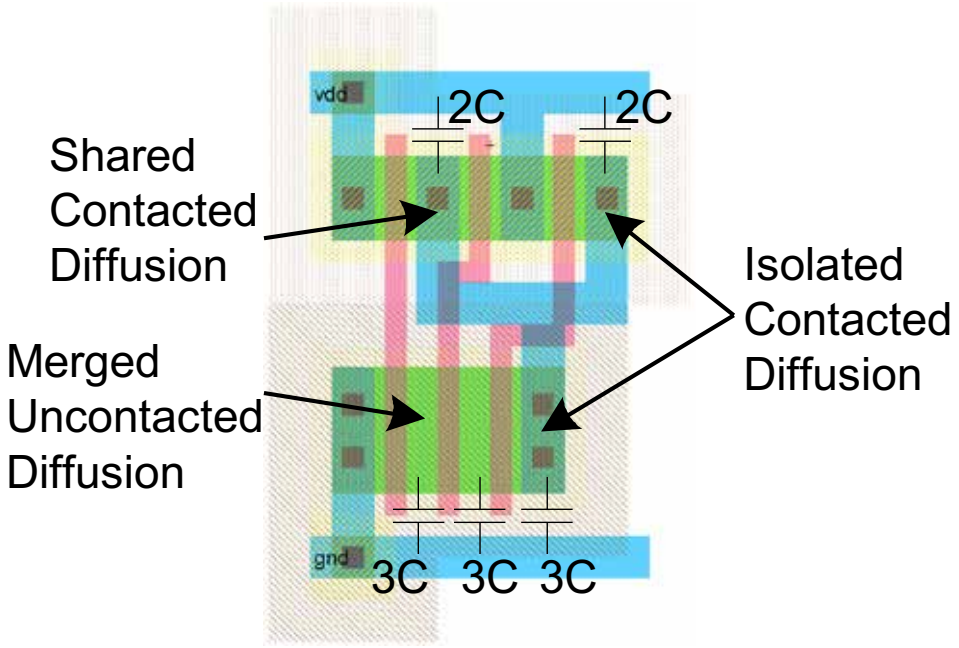


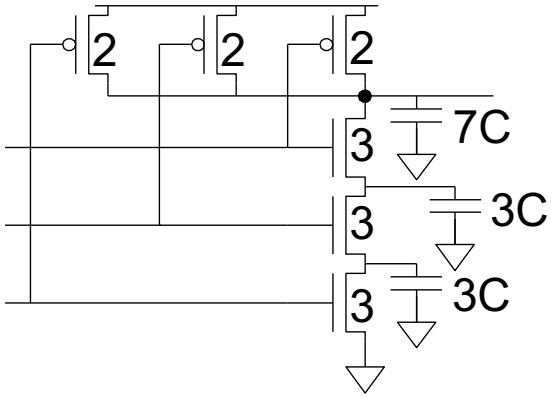


$$t_{cdr} = \left[(9+5h)C\right]\left(\frac{R}{3}\right) = \left(3+\frac{5}{3}h\right)RC$$

Diffusion Capacitance

- We assumed contacted diffusion on every source / drain.
- Good layout minimizes diffusion area
- Ex: NAND3 layout shares one diffusion contact
  - Reduces output capacitance by 2C
  - Merged uncontacted diffusion might help too





Layout Comparison

- **Which layout is better?**