EE382M-7: VLSI-I
Fall 2013

Lecture: Tu Th 9:30-11am in is UTC 3.132
Unique No.: 17220

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Description: We will study the process of implementing a digital system as a CMOS integrated circuit. The course will begin with a review of the basics of MOS transistor operation and the manufacturing process for CMOS VLSI chips. We will then study implementation of logic gates in CMOS. Specifically, we will cover layout, design rules, and circuit families. Afterwards, we will examine techniques for timing and power analysis and clocking. We will also examine ways to optimize timing and power. This will be followed by an overview of datapath design, specifically adders and multipliers. We will also study memory arrays, including SRAM and DRAM cell and clock design. The course will conclude with a survey-level discussion of several topics, including functional verification, test, design-for-test, electrical effects, and future trends.

Prerequisite: Electrical Engineering 316, 438, and 339 with a grade of at least C in each. Students are expected to be able to design logic circuits and implement state machines using logic and memory elements.

Textbook:
- N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* (4th *Edition)*, 2010. Addison-Wesley.

Reference Textbooks:
- Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd Edition, Prentice Hall, ISBN: 0-13-090996-3, 2003.
- S.M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design (3rd edition)*, McGraw Hill, ISBN 0-07-246053-9, 2003.

Grading Policy:

Homework	10%
Midterm Exams I and II	30%
3 Laboratory Exercises	35%
Final Project	25%

Lecture Outline (tentative):

Date	Day	Topic of Lecture/Discussion	Reading
8/29	Th	Introduction, CMOS Transistors	1.1 - 1.3
9/3	Tu	CMOS Fabrication and Layout	3.1 - 3.5
9/5	Th	CMOS Logic	1.4 - 1.5
9/10	Tu	MOS Transistor - 1	2.1 - 2.3.1
9/12	Th	MOS Transistor - 2	2.1 - 2.3.1
9/17	Tu	CMOS Gate: Static and Dynamic Characteristics	2.3.2-2.6, 4.3-4.4
9/19	Th	Combinational Logic -1: Logical Effort	4.5
9/24	Tu	Combinational Logic -2	4.5
9/26	Th	Datapath Design - 1: Adders	11.1 - 11.2. *Lab 1 Due*
10/1	Tu	Datapath Design – 2: Multipliers, Detectors	11.3 - 11.10
10/3	Th	Interconnect in CMOS Technology	6.1 - 6.6
10/8	Tu	*Mini-review*	
10/10	Th	**Midterm 1**	
10/15	Tu	Sequential Elements – 1	10.1 - 10.4
10/17	Th	Sequential Elements -2	Notes
10/22	Tu	Hardware Description Languages, Synthesis	Notes
10/24	Th	Dynamic Logic	9.2.2-9.2.5, 9.4 - 9.5 *Lab 2 Due*
10/29	Tu	Memory – 1: Organization / Architecture	12.1 - 12.3 *Project Topic/Team Due*
10/31	Th	Memory - 2: CAMs, ROMs, PLAs	12.4 - 12.7
11/5	Tu	*Mini-review*	
11/7	Th	**Midterm 2**	
11/12	Tu	Memory – 3: SRAM, DRAM, Peripherals	
11/14	Th	Introduction to Test	15, Notes
11/19	Tu	Nanometer Scale MOS Transistor	2.4, 7.2 *Lab 3 Due*
11/21	Th	Thanksgiving Holiday	
11/26	Tu	Design for Low Power - 1	5.1 - 5.3, 5.5
11/28	Th	Design for Low Power - 2	5.1 - 5.3, 5.5
12/3	Tu	Skew-Tolerant Design	10.5 - 10.6, 13.4
12/5	Th	Technology Scaling and Economics	7.4, 14.5
12/6	Fri		*Project Due*

Course Web Page: http://courses.utexas.edu/
We will rely heavily on the course management system Black Board. It will be used for posting the homework assignments and course handouts, and for making the announcements. The students are required to regularly check the course site.

College Drop/Add Policy: An engineering student must have the Dean's approval to add or drop a course after the fourth class day of the semester.

Students with Disabilities: The University of Texas at Austin provides upon request appropriate academic accommodations for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4641 TTY.

Scholastic Dishonesty: Faculty in the ECE Department are committed to detecting and responding to all instances of scholastic dishonesty and will pursue cases of scholastic dishonesty in accordance with university policy. Scholastic dishonesty, in all its forms, is a blight on our entire academic community. Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, collusion, falsifying academic records, or any act designed to give an unfair academic advantage to the student. Penalties for scholastic dishonesty are severe and can include, but are not limited to, a written reprimand, a zero on the assignment/exam, re-taking the exam in question, an F in the course, or expulsion from the University. Don't jeopardize your career by an act of scholastic dishonesty.