Department of Electrical and Computer Engineering
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ECE 382N, Spring 2000
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Homework #3, No due date (not to be turned in).

Note: This assignment is for your use in planning your term project. It does not have to be turned in. However, we strongly encourage you to start work on this early. Doing this assignment is excellent preparation for the first exam, and will aid you in catching problems before they become major hassles.

Part 1.

Expand your Data Path to include the following instructions:

prefixes: segment override (all), operand size.
instructions: BTS, JNE, JNB, HLT, ROR, SAL, SAR, BSWAP, XCHG,NOP, PUSH, POP.
addressing modes: SIB byte. data types: byte.

Show all control signals needed to control the data path. (In homework set 4 we shall start specifying the microcode or hardwired control that will produce those control signals).

Part 2.

Enter the additions of Part 1 above into your Verilog specification.

Part 3.

For your augmented specification, select an additional set of five instructions and appropriate addressing modes, prefixes. Calculate the number of cycles required to execute each of these five instructions. Your results will depend on your choices, of course. For purposes of this assignment only, assume memory access takes ten processor cycles.