Department of Electrical and Computer Engineering
University of Texas at Austin

ECE 382N, Spring 2000
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Homework #5, Due: At your first design review (March 24-31, 2000).

This assignment should be done in cooperation with your partners. This is the design you will work on together as a group from now until the end of the term. (Obviously, since this assignment is the basis of your design review, it must be completed on time.)

Part 1. To the description of your machine, add the CALL, RET, and IRET instructions, and the logic necessary to initiate exceptions and interrupts. Also add segment limit checking and the generation of an exception when the segment limit is exceeded. To test this functionality you (not your machine) will need to create an Interrupt Descriptor Table in memory, as would be done by the operating system in real life. Please hand in hardcopies of everything created to implement this functionality.

Note: Some of this is going to require additional internal registers and/or additional bits specified in existing internal registers.

Hand in the schematics created.

Part 2. Design an external bus interface. [You will need this to handle external interrupts, memory accesses, and I/O.] This should include a description of bus signals and bus protocols.

Hand in a description of this bus interface.

Part 3. Construct a block diagram for the machine that you intend to design and simulate this semester. This should include the major functional blocks (e.g. Data Path, Control, I/O components, Cache Memory, Main Memory, Level 1 Virtual Address Translation, Memory Protection etc.), and their interconnections. Be as detailed as you feel is necessary.

Hand in the block diagram.

Part 4. Construct a detailed schedule for the design of your machine. Estimate how much time you expect to spend designing, simulating, and debugging each component on the Verilog system. Allow yourself as much debugging time as possible. As time goes by, you'll be able to draw a large schematic in a single evening, but the test/debugging/resimulate cycle can be extremely time consuming. It will be advantageous to leave some time at the end for critical path analysis and redesign.

Hand in the schedule (no longer than one page).

Part 5. Coordinate with your partners and sign up for a preliminary design review. These will take place on March 24-31 in my office unless otherwise notified. They will probably take 45 minutes. A sign up sheet will be posted on my office door (Room 541) some time before the due date of this assignment. All members of your group must attend the preliminary design review. If no time slot is good for the members of your group, please see me and we will make other arrangements.