Department of Electrical and Computer Engineering
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ECE 382N, Spring 2000
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Design Project Specifications

First Design Review: by appointment, March 24-31, 2000.
Final Design Review: by appointment, May 8-12, 2000.
Final Report Due: May 12, 2000.

Design Reviews. It is my intent to hold at least two design reviews for each team this term. More will be held if necessary. Both will be in my office (541a ENS), and will be conducted by Mary Brown and me. (Sometimes one of my PhD students will wander in to learn some new ideas and ask questions. If he keeps asking questions, you should feel flattered that what you have said has impressed him.) All members of the design team must be present for each review. The purpose of a design review is to verify the integrity of the design and to catch problems before they become major. We will review your design decisions, performance/cost considerations, and other tradeoffs involved in your design. We will attempt to insure that, in fact, the machine, if built, will perform as specified. You should feel encouraged to provide supporting documentation (e.g. simulation results) to assist us in that task. The first design review is largely for your benefit. The more you can get from it, the easier the final stages of your project will be.

Final Design Review: At the final design review, you will be expected to turn in a complete design of that portion of an x86 implementation described below. This is to include state diagrams, data path, complete circuit drawings, parts list, and a complete description of the control logic.

As part of the final design review, we will provide you with a test program consisting of approximately ten x86 instructions. We will expect you to demonstrate via the Verilog simulation of your design that your design can execute the test program. [A larger sample test program will be available a week before the final design review for your use in preparing for this.]

Your design is to include at least the following:

(1) All opcodes and prefixes covered in the homework assignments.
(2) All addressing modes and data types covered in the homework assignments.
(3) Instruction and data caches.
(4) The design and specification of the external bus.
(5) The handling of cache accesses and memory, including the functionality of an MMU and basic segmentation.
(6) The design of a simple I/O device.
(7) The handling of exceptions (e.g., segment limit) and interrupts (e.g., I/O device).
(8) A responsible cycle time. NOTE: A particularly careful attention to cycle time will not go unnoticed in the grading.

Optionally, you may wish to include one or more of the following:

(1) More comprehensive pipelined instruction execution.
(2) More complete support of the memory system: paging, interleaving.
(3) Microcode or an attached processor to support integer multiply, floating point arithmetic.
(4) Microcode to support a commercial instruction set: string operations etc.
(5) The design of a DMA controller and the additional support to enable it to function in your system.

(6) Other features, as your creativity suggests, and time permits.

Note: You are not expected, and will not be penalized, if you do not implement all of the above. If you get to the point late in the term where you need to choose what must stay in and what to leave out, you are strongly encouraged to talk to the instructor and TA about it.

The Final Report. Subsequent to the design review, but not later than 5 pm, May 12, 2000, you are expected to turn in a final report describing your design. The report is to be written in clear, understandable English. The information must be clear and legible, accompanied by well-laid-out diagrams, as appropriate. We must stress that it is your responsibility to convey the information contained in your design. For your convenience, the following items should be used as a checklist of what we would expect to be included in an acceptable report:

The Report Check List.

(1) Title Page, Abstract, Contents, Chapters, Appendix.

(2) Introduction: Application area, general requirements, logic family, features, design approach.

(3) Design discussion: Brief description of control and data path, both high-level and low-level.

(4) Design considerations: Description of goals and priorities. Discussion of the tradeoffs you considered in determining your implementation, including the data path, instruction set optimizations, method of control, memory system, and console functions and start-up.

(5) Critical path analysis, including relevant timing diagrams.

(6) Final design decisions relating to the items of part (4).

(7) Conclusions: Discussion of constraints, performance, cost, recommendations for a next design, etc.

(8) Appendixes

The Instruction Set, opcodes, addressing modes, data types supported.
A start-up procedure.
Specifications, timing diagrams, etc.
Instruction execution times.
A parts list (which ones and how many of each).
Microinstruction format, and microcode listings, where and if appropriate.
Simulation results.*
Important Karnaugh maps.
PLA/ROM tables.
Schematics.

A Final Note:

Neatness, spelling, English usage, clarity, and organization of the material cannot be emphasized too much.

* During the week of May 1, you will be given a short program (this is not the test program discussed under the heading "Final Design Review" above). The annotated results of the cycle-by-cycle simulation of this short program are to be included in your report. This simulation should be done at the maximum speed of your processor (as calculated in the critical path section).