The University of Texas at Austin
Department of Electrical and Computer Engineering

Course Descriptor: EE 382N - Microarchitecture, Unique Number 15008

Instructor: Yale N. Patt (http://www.ece.utexas.edu/~patt)
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Office Hours: MW, 6:30pm to 7:30pm, and by appointment
Course Title: Microarchitecture.

Course Overview:

Objectives of the course -- EE 382N is intended to provide a solid introduction to microarchitecture to the serious graduate student who is interested either in PhD research in microarchitecture or an industrial position on a leading edge microarchitecture project. We expect to do that in two ways:

(1) Each student will participate as a member of a design team to complete a substantial design of a cpu for a subset of a commercially available modern microprocessor. We will use Intel's IA 32 (nee x86) ISA as our starting point. Each team will start with a clean sheet of paper and design the data path, microsequencer, microprogrammed or hardwired control, microcode or logic, as appropriate, interface to memory & I/O, and the selection, interconnection of parts to implement all of the above. The design will be done at the logic gate level, in structural level Verilog where the design will be concerned with timing issues (propagation delay, cycle time). The design may be an aggressive pipeline, or a more conservative microarchitecture, at the discretion of the design team. Our expectation is that each student will come out of this experience more fully appreciating the problems that come up in designing the microarchitecture for a general purpose ISA.

(2) Lectures, in addition to dealing with design issues relevant to the project, will provide in depth coverage of some of the important latest hot topics in high performance microarchitecture, and an awareness and appreciation of the field of computer architecture, particularly alternative design styles and implementation tradeoffs. We will deal with problems involving instruction supply, data supply, and instruction processing, compile-time/run-time tradeoffs, very aggressive branch prediction, wide-issue processors, in-order vs. out-of-order execution, instruction retirement. Case studies will be taken mostly from current microprocessors, although we may examine (as time allows) a classical older implementation.

Relevance of the course -- This course provides a fundamental body of knowledge useful to graduate students who plan to do PhD research in microarchitecture or plan to seek employment in the microprocessor industry upon completion of their degree.

With respect to PhD research, several major IEEE and ACM conferences deal specifically with research results from this field, including ISCA, Micro-n, HPCA, ASPLOS, and PACT. Several prestigious journals publish research based on the foundation material taught in this course. There does not appear to be any lessening of interest in this material in the research community.

With respect to the microprocessor industry, companies seek graduates who have the insights acquired from this course. Many major employers of our graduates (Intel, for example) have an increasing need for graduates who have these insights.

Where I am coming from -- The course outline lists some topics we will try to discuss during the semester. We will undoubtedly not get to all of them for several reasons: (1) there is too much here to cover in one semester. (2) "covering" the material is not something I particularly aspire to. Furthermore, we will probably not cover the topics in the static schedule I have produced, regardless how much I plan to, today.

My objective in our class meetings is to explore ideas that will be useful to your future research and/or your future work in industry. My view of research is that if you know the outcome before you start the project, then I am not interested in the work as "research." I suspect that many of our class meetings will follow some unintended path as we explore dynamically some issue that comes up. I want you to think critically about what you read, and explore creatively what might be possible. If that causes us to spend three times as long on a topic as we might otherwise if we covered the topic from my notes, it will not make me unhappy. If we get the material from my notes to yours without going through the brains of either of us, that will make me very unhappy.

Lest anyone think this is intended to encourage wild-eyed departures from fundamental knowledge, let me assure you that the one thing we always try to do is tie things to the fundamentals. My hope is to encourage you to combine mastery of the fundamentals, critical reading and analysis, and creative thinking.

CAD Tools -- For the project, we will be using a modern set of CAD design tools, provided by Synopsys, which use the Verilog design language. We will provide sufficient introductory material and examples to help you get started with these tools. Mastery of the tools is not an end in itself; on the contrary, the tools are expected to be a means to enhance your productivity in completing the project. **You are encouraged to help each other master the tools,** so that we can all get on with the business of carrying out our designs.

Finally, an important caveat -- My experience from teaching this course has been that the design project requires a much larger amount of time to complete than most students expect to be the case in the beginning. If this semester goes as the ones before it, you will be pleased with what you have accomplished after the term is over. But during the term, sometimes after a few consecutive sleepless nights, you may wonder what lapse in sanity caused you to sign up. Please consider this as you organize your workload for the semester.

Meeting Info:

The course consists of three hours of lecture plus a 1 1/2 hour discussion section each week. Lectures and discussions will take place MTW, from 5:00pm to 6:30pm. According to the University Course Schedule, class will meet on MW in ENS 126 and Tuesday in ENS 116, although those rooms may change. The course web page will always have the most up-to-date information.

On average, two of those three sessions each week will be a lecture, the third (on average) will be a discussion. Some weeks, it will be more beneficial to have three lectures. Other weeks, it will be more beneficial to have three discussion sections. The exact schedule of lectures and discussions, as best I know it today can be found in the Course Syllabus.

That is, I have (prior to the start of the course) developed a static schedule for the material. However, once the semester starts, I suspect I will make from time to time dynamic scheduling optimizations. I may also substitute a guest lecture if someone with an important message happens to be in Austin and available on a particular day. Bottom line is that I expect you to plan on being available all three days (MTW) for lecture or discussion. Please do not sign up for this course unless you are able to make all three class meetings each week.)

TAs: Moinuddin Qureshi (qk@ece.utexas.edu), Hyesoon Kim (hyesoon@ece.utexas.edu)

Course Home Page: http://www.ece.utexas.edu/courses/spring_04/ee382n-15008/

Textbook: There is no required text. References will be suggested where appropriate, depending on the topic. I expect to provide handouts on additional material when I feel that is useful. Also, Some of the lectures will use transparencies. In those cases, you will be provided with copies of the transparencies. From time to time, relevant material will be available for downloading on the course home page.

Prerequisites: Satisfactory completion of courses covering the material of EE 316 and 360N with a grade of A, or consent of the instructor.

Homework policy: Homework consists of three types: (1) problem sets, scheduled at the beginning of the semester to get the student ready for the major term project of the course, (2) individual problems assigned in class from time to time as I feel appropriate to test your comprehension of a point or to get you to take the point to the next level, and (3) the major design project discussed above.

Quizzes and Exams:

There will be two exams in class, a written exam on March 10, and an oral exam on April 15 or 16. There will be no written final exam. Also, I do not expect to give a make-up exam except in rare and well-documented circumstances.

The written exam will be closed book, with two exceptions: (1) The student may bring into the exam three sheets of paper on which the student may have written anything he/she wishes. All three sheets mus tbe original sheets (not printed nor xeroxed) in the student's own handwriting. (2) The student may bring into the exam any handouts that have been expressly permitted by the instructor prior to the exam.

The oral exam will be an individual exam in Room 541a administered by the instructor at a time suitable to fit the student's schedule. It will be 30 minutes in length. The student will be free to bring whatever reference material he/she wishes into the exam.

Grading mechanics: Three major items will contribute to your grade in this course: the design project, scores on the two mid-term exams, and homework and problem sets. You will note below that I have allocated 6% of your grade to "other" to give the TA and me some flexibility to include our subjective evaluation of your performance in the assignment of a final grade.

The items will be weighted, approximately as follows:

> exams, 42%
> project, 42%
> homework, problem sets, etc., 10%
> other, 6%

Final Exam: There will be no final exam in this course. In lieu of a final exam, you will have a final design review of your design project, and you will submit a final design project report. That final design project report must be submitted in 541a ENS during the final exam period reserved for a final exam in this course.

Cheating:

Students may work together BEFORE an exam to study for the exam. Students may work together to learn/understand the design tools, but not to work together on their individual design assignments. Students must work together within their design project group to complete the term project. All other work of the course must be your own work.

That is, any other collaboration, unless specifically instructed otherwise, constitutes academic dishonestly and will be directed to the Dean of Students for Disciplinary Action. If you are not clear as to what is permissible and what is not, please ask. Failure to ask ahead of time, and later invoking the statement, "I thought it was ok to do" does not exhonorate you.

If you need help, you are welcome to see the Instructor or one of the TAs. Receiving help from any source other than the Instructor, TA, or someone designated by the Instructor or TA is absolutely not permitted.

If you have any question about the above paragraphs, please ask the instructor or TA before the fact. If you cheat, you violate the soul of the University, which I take very seriously, and will not compromise.

Course evaluation: The MEC Common Evaluation form will be used to evaluate the instructor in this course.

Additional details:

I am asked to remind you to consult the University policy on the deadlines for adding/dropping courses. If you need help with this, please check with me or one of the TAs.

Allegations of Scholastic Dishonesty will be dealt with according to the procedures outlined in Appendix C, Chapter 11, of the General Information Bulletin, http://www.utexas.edu/student/registrar/catalogs/.

The University of Texas at Austin provides, upon request, appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4241 TDD, or the College of Engineering Director of Students with Disabilities, 471-4321.

Finally, for those of you who decide to continue in this course, Good Luck. I hope you find the experience an important part of your computer engineering education. I also hope you have a good time doing it.