Department of Electrical and Computer Engineering
The University of Texas at Austin

ECE 382N, Spring 2006
Y. N. Patt, Instructor
Daniel Lynch, Chang Joo Lee, TAs
Compile-time Course Outline
January 18, 2006
Revised

January 18: **First class meeting**. Introduction to the course, administrative details. Focus of the course. Architecture and Microarchitecture: Sciences of Tradeoffs.

January 19, 20: Extra discussion sessions, for those who feel they need it.
January 23: Problem Set 1a due at the start of class.

January 23: Basic concepts in architecture and microarchitecture. Critical path, Bread and Butter Design, Partitioning, Timing, Pipelining. Data Path, state machine, microsequencer, microinstruction definition, and microcode. Microprogramming (horizontal, vertical, two-level, dynamic microprogramming, bit steering). Extension to pipelining and pipelined control. Effective use of short pipelines, with some digressions into more effective use of long pipelines without blocking. The structure of a modern pipeline. Functions at each stage.

January 24: **Discussion Section**. Introduction to the CAD tools we will be using in the course. Review of the use of these tools on the logic design of a simple ALU.

January 25: Basic concepts in architecture and microarchitecture, continued. The two most important bottlenecks: memory latency, conditional branches.

January 26, 27: Extra discussion sessions, for those who feel they need it.
January 30: Problem Set 1b due at the start of class.

January 30: The x86 ISA, and some implementation issues.
January 31: **Discussion Section**. CAD tools, continued.
February 1: Pipelining in the year 2006.

February 6: Branch Prediction.
February 7: Discussion section
February 8: Branch Prediction, continued.

February 13: No class. (HPCA).
February 14: Optional discussion section (HPCA).
February 15: Run-time optimization: The Trace Cache.

February 20: Problem Set 2 due at the start of class.

February 20: Discussion section.
February 21: Compile time optimization: The Block-structured ISA.
February 22: Simultaneous Multithreading and SSMT.

February 27: Discussion section.
February 28: Run-time optimization: Data Flow; HPS.
March 1: Pentium Pro and Pentium 4 implementations.

March 6: Problem Set 4 due at the start of class.

March 6: Measurement methodology and abuses.
March 7: Discussion section.
March 8: RISC, a Retrospective.

March 13 through 17: Spring break, no class.

March 20,21,22: Individual group meetings to define individual implementations.

March 23, 24: First Design Review in 541a ENS, by appointment.
[Problem Set 5 is to be handed in at that time.]

March 27: Finish Pentium 4, Pentium M, Niagra, etc. The RISC phenomenon.
March 28: Discussion section.
March 29: Written exam, in class. Room to be posted.

April 3: Measurement methodology and abuses
April 4: Current hot topics: Intro to Runahead Execution, Wish Branches, and L2 cache structures to improve on memory latency.
April 5: Discussion section, as needed.

April 10: Guest lectures by Onur Mutlu on Runahead Execution and Hyesoon Kim on Wish Branches.
Note: lecture will be in ETC 5.148.
April 11: Guest lecture by Moinuddin Qureshi on new L2 cache structures.
Note: Lecture will be in ETC 5.148.
April 12: Cache Coherence

April 17: Future processors, part 1 (starting with the Naysayers)
April 18: Discussion section, as needed.
April 19: Discussion section, as needed.

April 24: Discussion section, as needed.
April 25: Discusssion section, as needed.
April 26: Future processors, part 2 (what will the microprocessor look like in 2016)

Oral exams (Exam 2) will be given in 541a ENS on April 27,28.

May 1: Guest lecture by Ron Kalla of IBM. (Ron Kalla has been a key microarchitect in the recent IBM Power series of microprocessors.)
May 2: Discusssion section, as needed.
May 3: Last class meeting. Review of the course.

Final project design reviews in 541a, May 4,5 by appointment.

May 12: Final project report due in 541a, 10pm.

Note: there will be no final exam in this course.