EE460N Exam 1 Review

Buzzwords(selected)

Endianness
Addressability
Overflow
predicated execution
RISC vs CISC

instruction supply
data path
data supply

Major Topics

LC-3b:

1. Implementing a new instruction
2. Micro-sequencer (how do IR[11], BEN, R signals work?)
3. State Diagram(What needs to happen to each instruction?)
4. Datapath
5. How does CC work? How can CC be set?
6. How does memory operation work?

Pipelining

What is pipelining?

Difference between throughput and latency

What can pipelining get us? At what cost?

What does a pipelined processor look like? (F,D,E,Mem,WB)

Are there other ways to have a pipelined processor? (multiple functional units)

Branch Prediction

Why do we need branch prediction?

2-bit saturating counter

When would branch prediction be not necessary?

What is misprediction penalty? What can affect it?

Out of Order Execution

What problem does out of order execution solve?

What are some of the new structures introduced with out of order execution?

What problem does out of order execution introduce?

How does Tomasulo’s algorithm solve those problems?

What is the one problem that Tomasulo’s algorithm does not solve?

Scoreboard

What does scoreboard do?

What information need to be included in the scoreboard?

Where is scoreboard usually?

Reservation Station

What does RS do?

What information does the RS need to hold?

Should I have one RS for the entire processor? Or have a one RS for each functional unit?

Register Renaming

What does RR do?

What problem does RR solve?

How were those problems dealt with in a in order processor?

Separation between PR and AR

What does a tag represent?

Data flow graphs

(destination does not matter as long as later instructions can find it)

ROB

What does ROB do?

What problem does ROB solve?

Difference between completing an instruction and retiring an instruction

Register File

What needs to be in the architectural register file?

What needs to be in the physical register file?

Architectural RF

Valid	Tag	Value
...	...	...

Physical RF

Valid	Value
...	...

Putting Everything Together

In a out of order processor, what is done in order? What is done out of order?

What happens in Fetch?

What happens in Decode?

How are instructions scheduled?

What happens when instruction completes?

Front End (everything before reservation station)

Fetch and Decode are done in program order.

Fetch the instruction as you would in a regular in order processor

Read the operand(either value or tag), based on what?

Grab an available tag, and do what?

Put itself into the RS and the ROB

Architectural RF

Valid	Tag	Value
...	...	...

Physical RF

Valid	Value
...	...

Execution

When all the operands of the instruction is ready, AND when the functional unit is ready, the instruction will be issued.

What happens when two instruction is ready in the same cycle and the processor only supports to issue one instruction each cycle?

If the instruction has data dependency(what kind?), how would it know the data is ready?

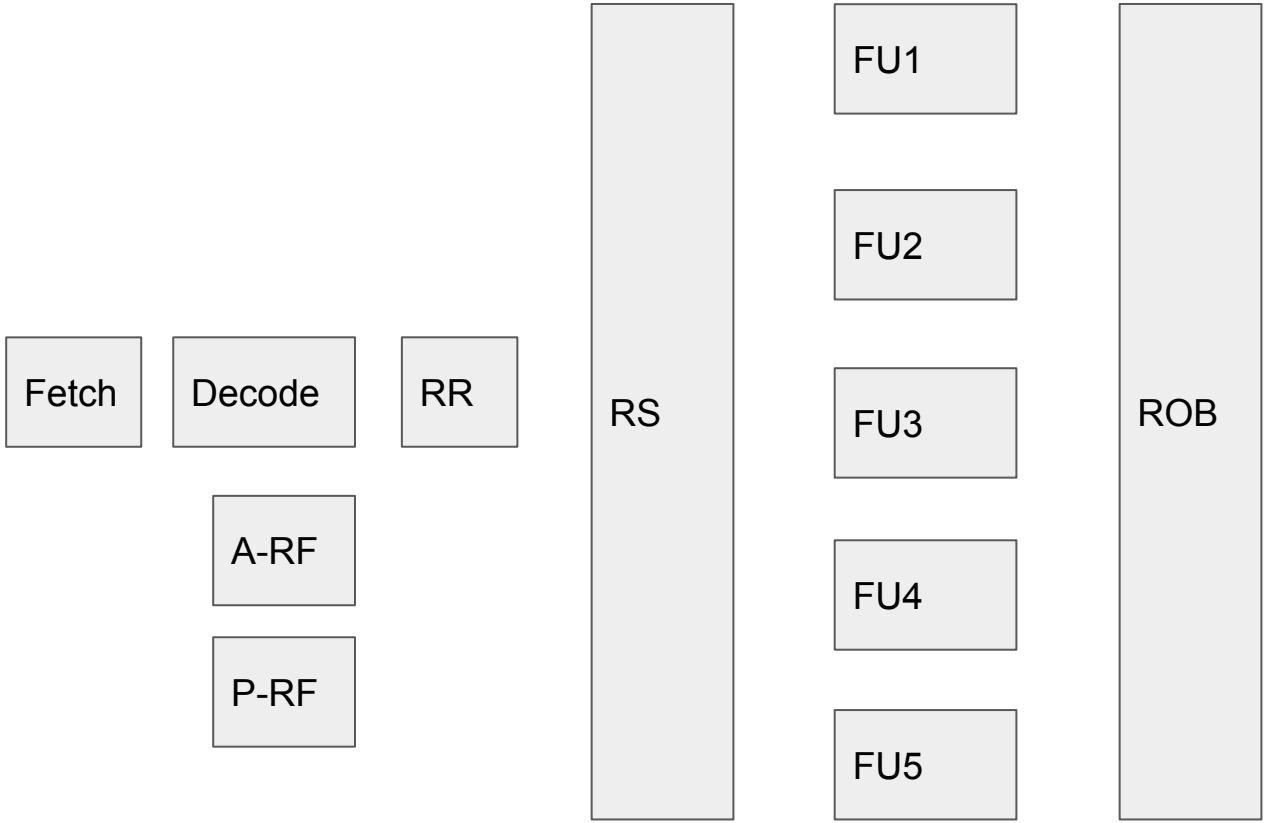
Completion/Retirement

When an instruction completes, broadcast the result to the RS so that all other instructions depended on this can grab the value.

At the same time, write the result back to physical register.

When the instruction at the top of the ROB completes, it can retire. Then the next instruction becomes the top of the ROB

When an instruction retires, it updates the architectural register.


Fetch
Decode
RR
A-RF
P-RF
RS
FU1
FU2
FU3
FU4
FU5
ROB