### Short Retrospective on RISC

# Open Microcode



- Compiler Generates Lowest Level of Interpretation
  - No Microcode
  - Single Cycle Execution
- Complex Compiler vs. Complex Hardware
- Issues:
  - Bandwidth, Compiler Complexity, On Chip Tailoring
  - Wasted Cycles

## What is it?

- Originally : Open Microcode
  - John Cocke (1970's)
- 1980: Simple Set of Simple Instructions
  - Sequin, Patterson (1980)
- 1989: Short, Tight Pipelines
  - John Hennessy
- 1994: VLIW
  - Wall Street Journal

## **Characteristics**

- Fixed Length, Uniform Decode Instructions
- No Microcode
- Load/Store
- Larger Register Set
- Delayed Branch
- Register Windows

# What is it (Non-Technical)

- Everything Since 1983
- "Good"
  - Motorola 68010 Article
  - Microcoded RISC Article
  - MicroVAX 2
  - VAX 9000 Literature
- SPARC System
  - The "RISC" Core

## Why Did It Happen

#### Masterful Marketing

- Published Berkeley Benchmarks
- RISC Chip in Weeks, VAX in Years
- Simple is Beatiful
- 4-on-floor vs. Automatic
- Time-to-Market Curve
  - VAX 8600 Was Very Late
  - Track Technology Curve
- Why Was it Taken Seriously
  - HP Bet the Family Store

## Comments on the Hype

- Simple is Beautiful
  - Complex Instructions Provide Opportunity for Speed-Up
    - 1<sup>st</sup> add Fl.Pt.
    - Graphics
    - *MMX*
  - Compilers Never Use It
    - Some BAD Implementations
    - One Compiler or All Compilers
- Published Berkeley Benchmarks
- Why did H-P jump in ?

# The Players

#### • The University Experiments

- RISC (Berkeley, 1980, Patterson, Emphasis on "Simple")
- MIPS (Stanford, 1981, Hennessy, Emphasis on Compiler)

#### Commercial Products

- HP-PA (The IBM Team, Emphasis on Compiler)
- SPARC (Berkeley RISC)
- MIPS (Simple)
- AMD 29000

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- Motorola 88000
- IBM RISC System 6000 (Return to Past)