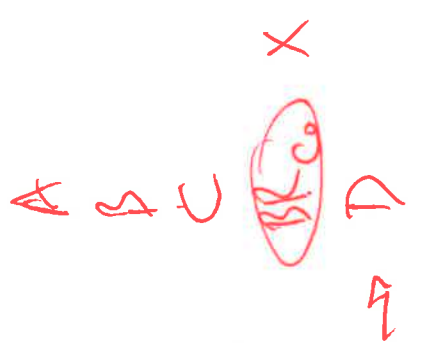
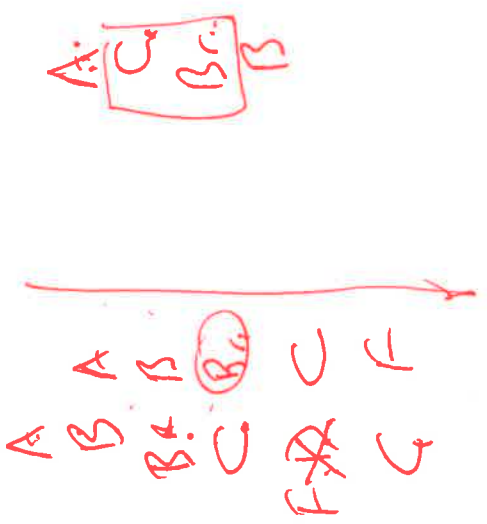


Mechanisms: Run-time and Compile-time

Mechanisms

- ***Conditional Branches***
- ***Trace Cache***
- ***Block-Structured ISA***
- ***Wish branches***

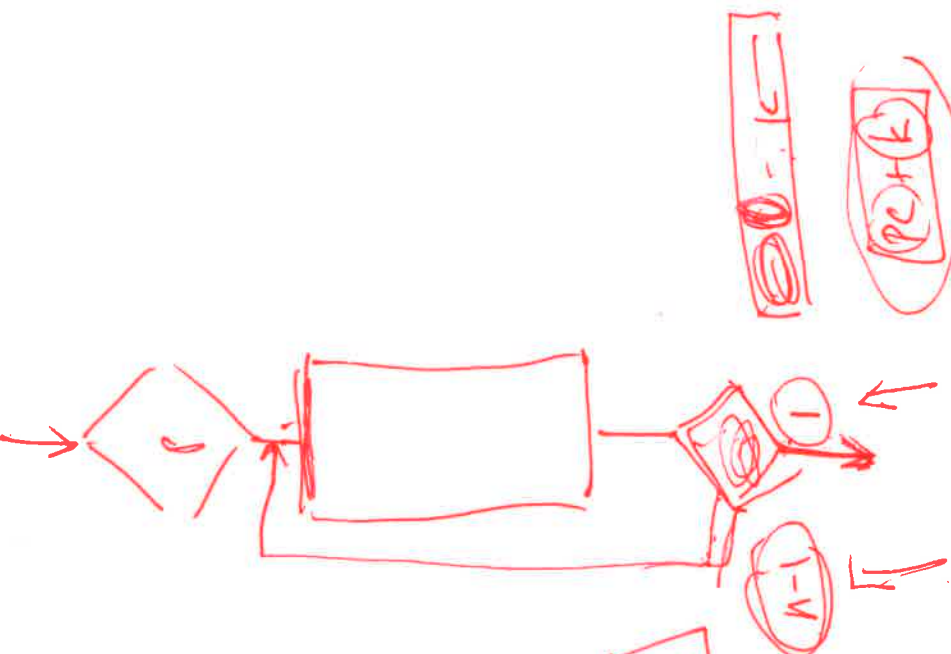


BFN

$$2+3 \rightarrow 5$$

$$2+7 \rightarrow 9$$

$$2+8 \rightarrow 10$$



JIM SMITH
1881 ADST
TSCA 1981

976

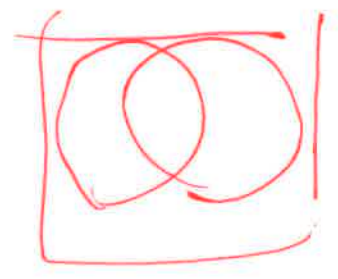
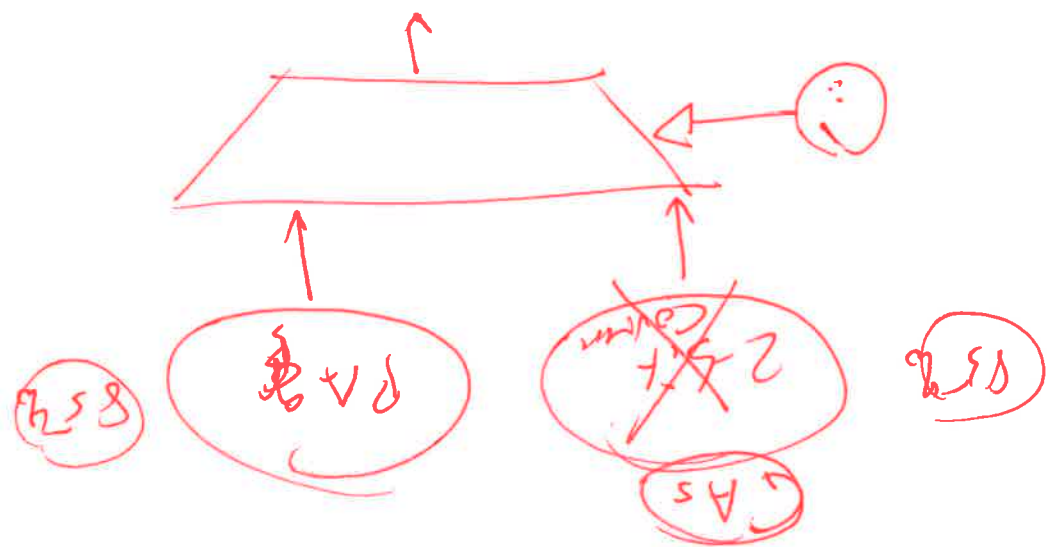
13

986

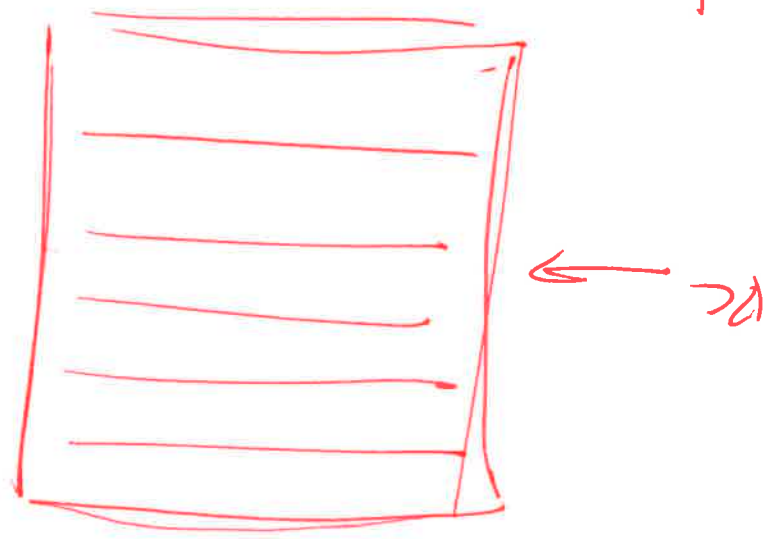
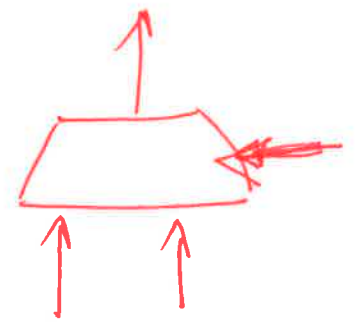
22

996

$$\frac{306}{206}$$



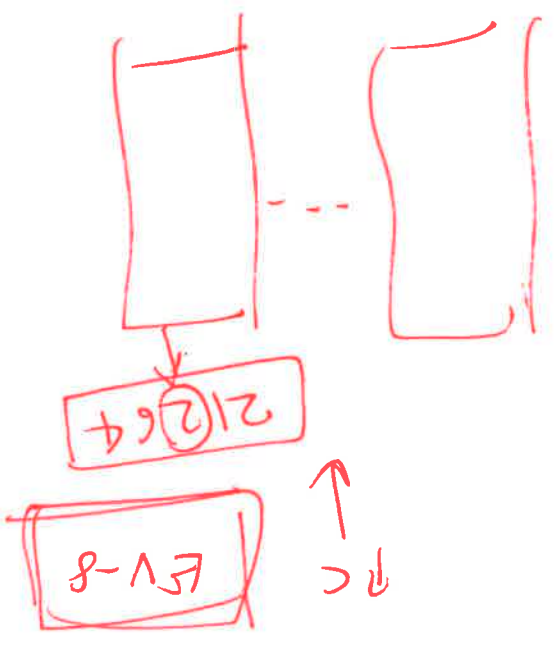
SAS
9



GAS

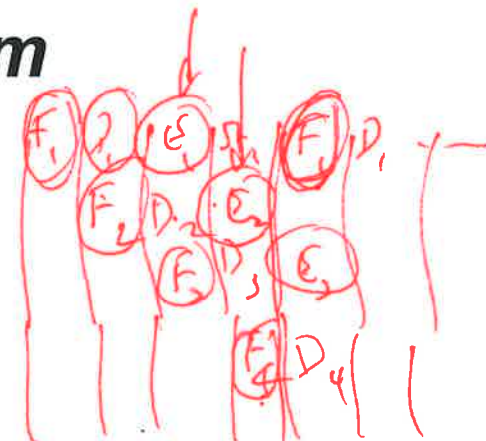
PAR

PAR



The Conditional Branch Problem

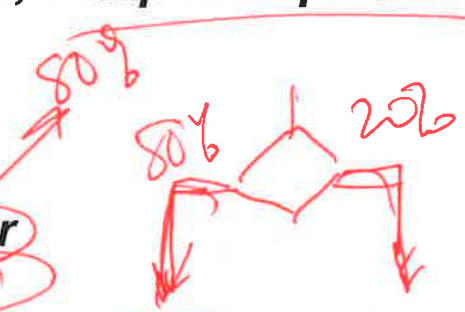
- **Why? Because there are pipelines. (Note: HEP)**
- **Mechanisms to solve it**
 - Delayed branch
 - Take both paths
 - Eliminate branches (predication, compound predicates)
- **Branch Prediction**
 - Static: Always taken, BTFN
 - Early dynamic: LT, 2 bit counter
 - 2 level → gshare, agree, hybrid
 - Indirect jumps
 - Perceptron
 - Expose branch prediction hardware to the software
 - Wish branches



Burton
Smith
1978

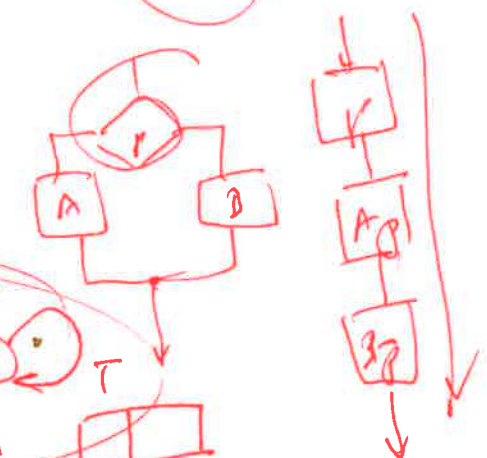
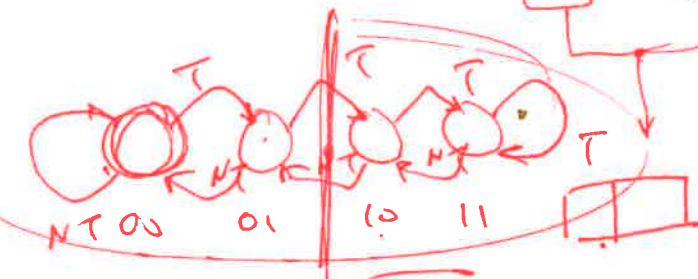
A. DOLLAS

SIMULTANEOUS
Multiple
Threads



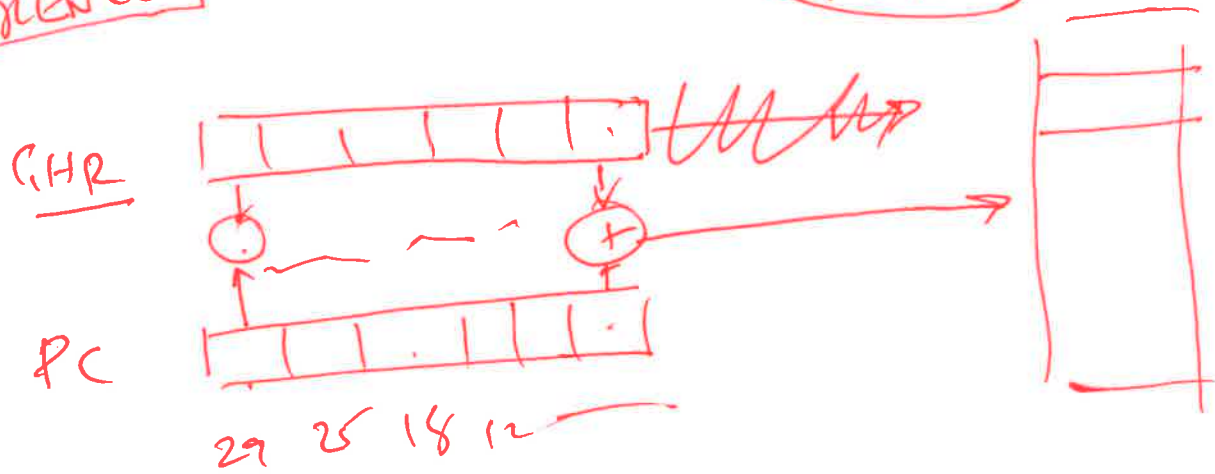
TAGE AND/OR SCHEDULE

70%

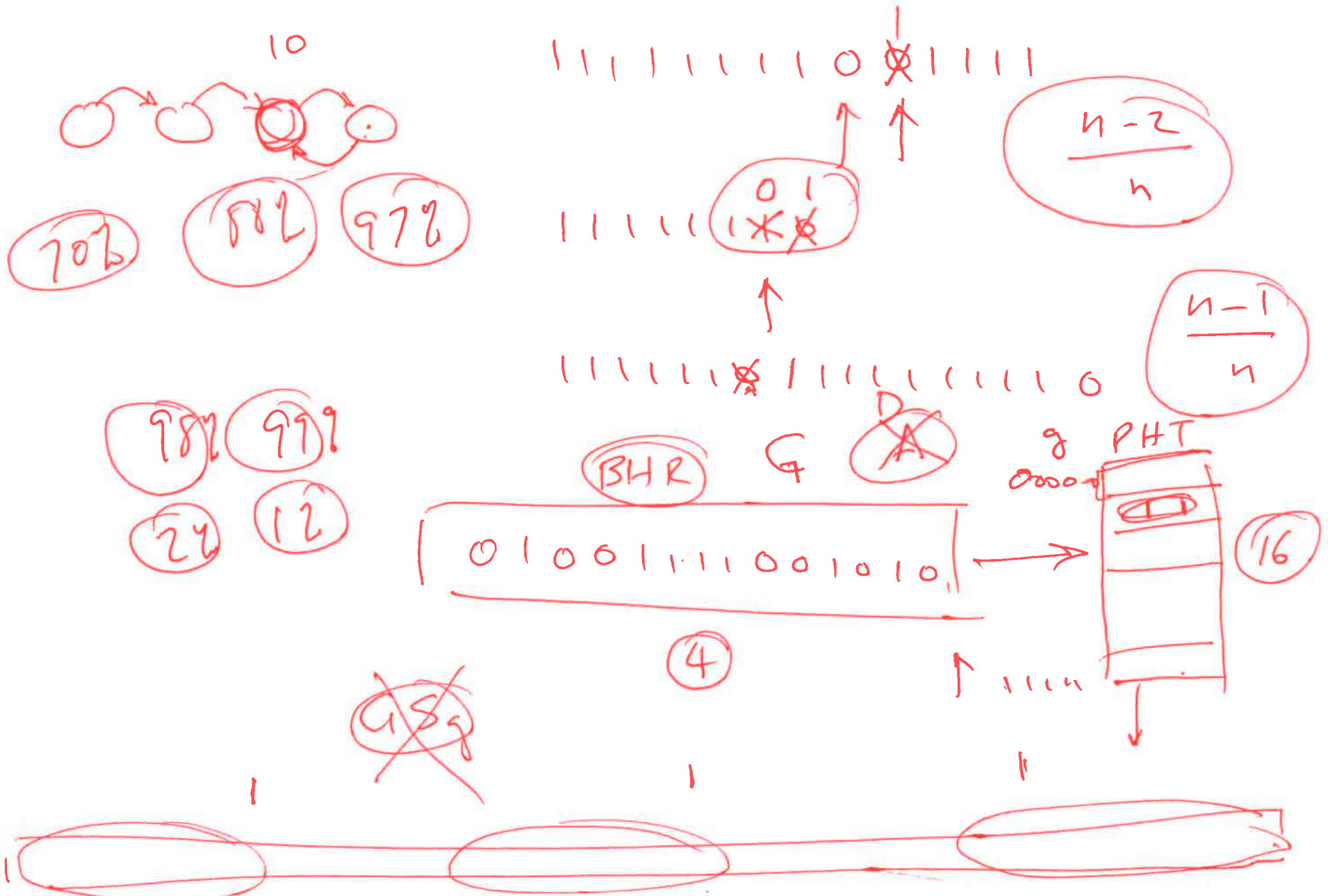


INTERFERENCE

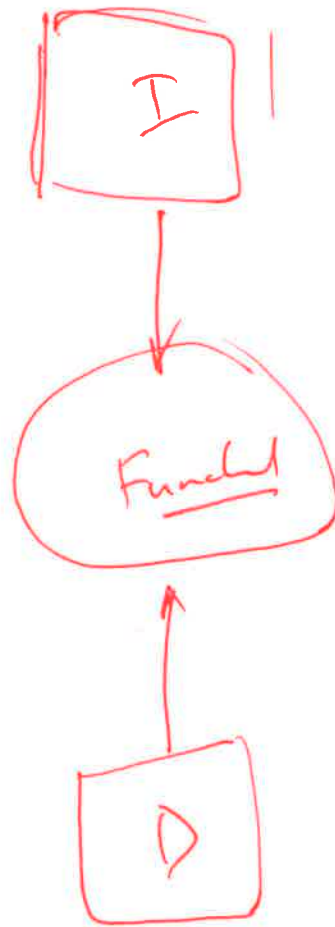
Scott McFarling (John Hennessy)
1993



CSHARB

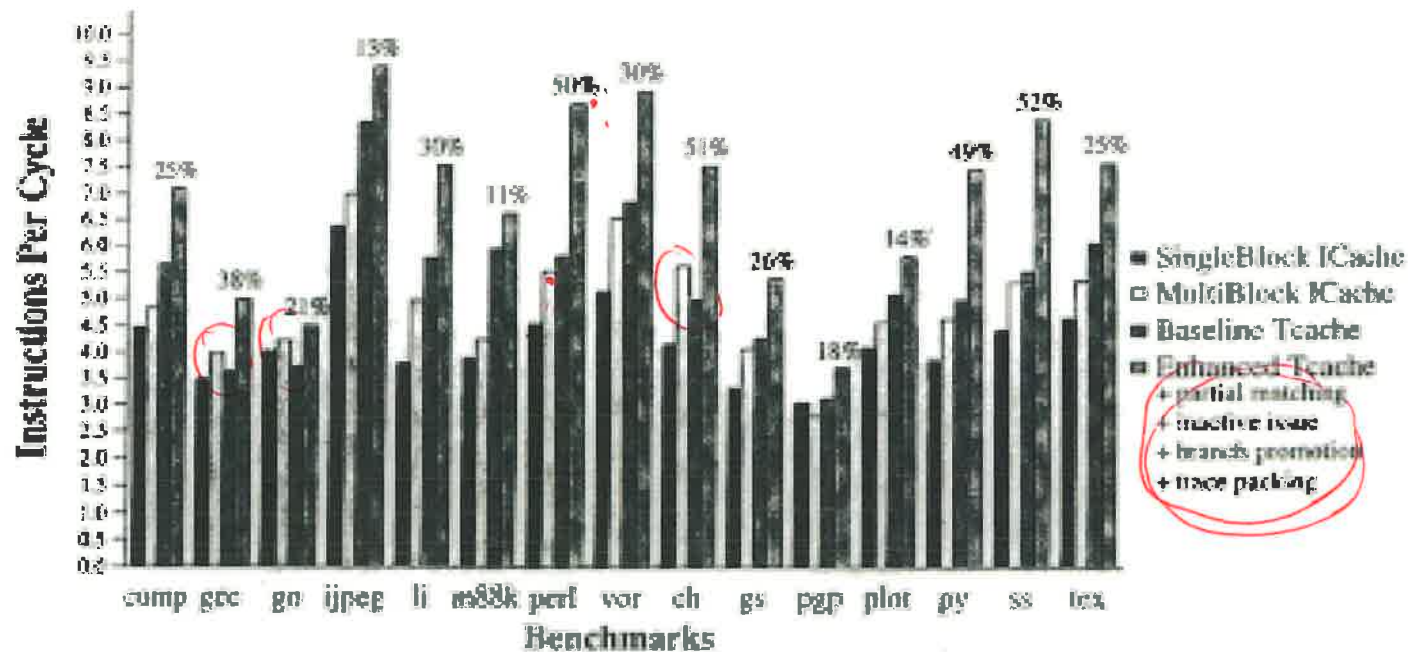


KIMMING SO → ASPLoS 1992 OCT, 1992
 YNP → MICRO 1991 NOV, 1991



Prefetching
100% BP accuracy
No Packet breaks

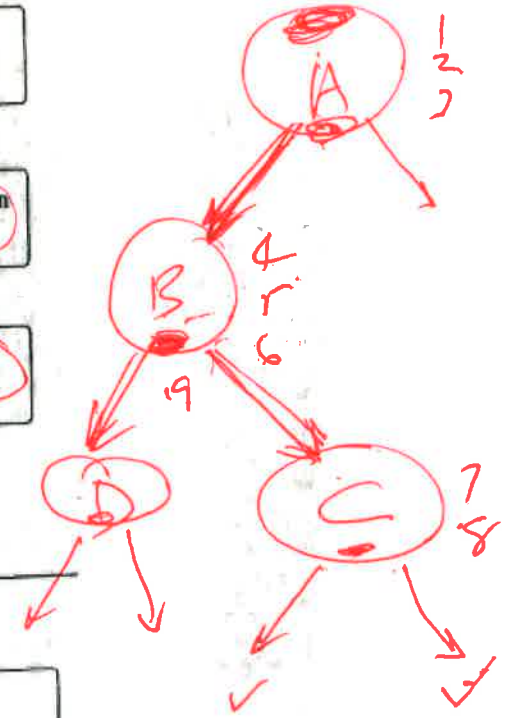
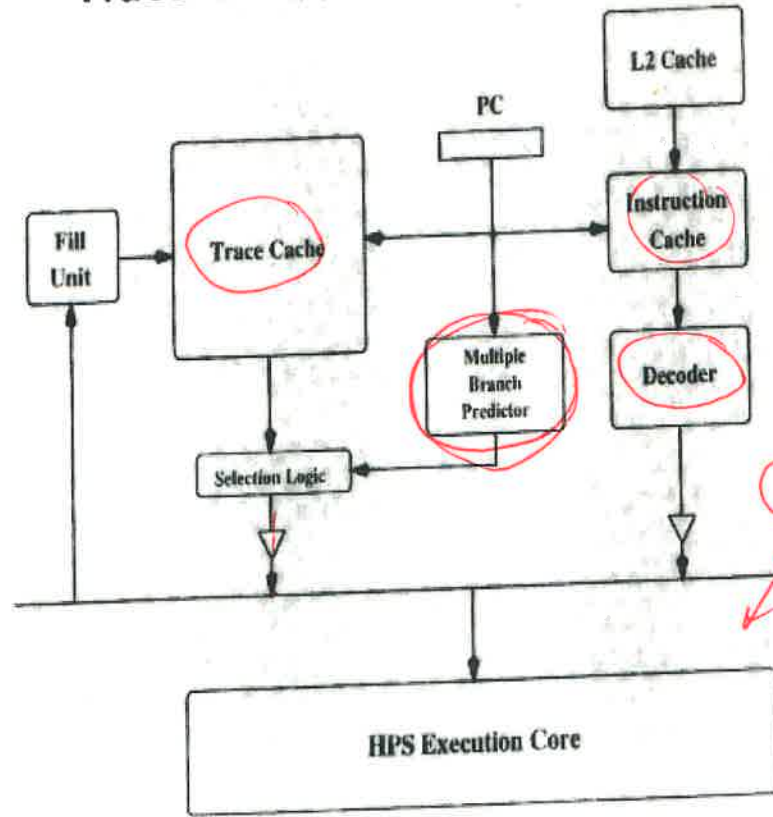
Overall Performance (aggressive core)



9
9
9

Trace Cache Fetch Mechanism

Jim Smith
Eric Rotenberg



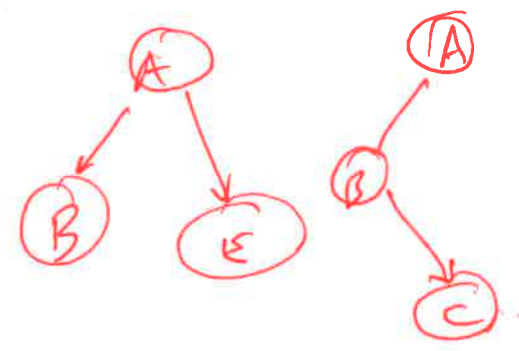
1989 | Uri Weiser
Alex Peleg | 1989

Trace Cache Issues

- Storage partitioning
 - Set Associativity
- 4-way Set Assoc. Cache

- Path Associativity
- Block Collection (retire vs. Issue)
- Fill Unit Latency

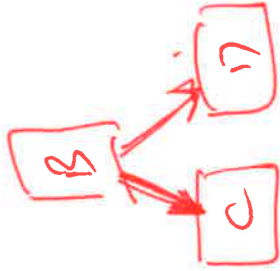
- * • Partial Matching
- * • Inactive Issue
- Dual Path Segments
- * • Branch Promotion
- * • Trace Packing



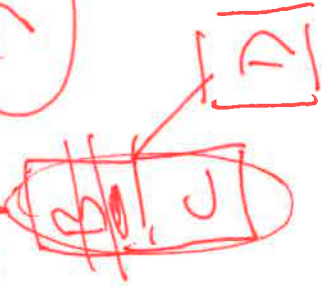
Supra

Supra block
ISCA (1989)

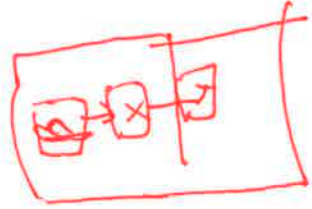
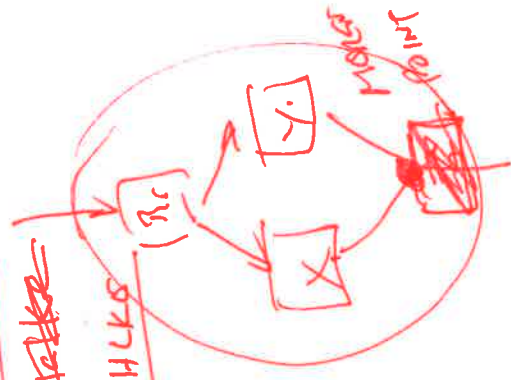
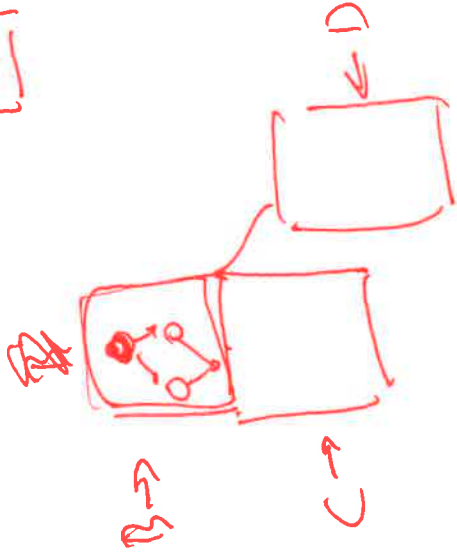
Pole Change



Supra block



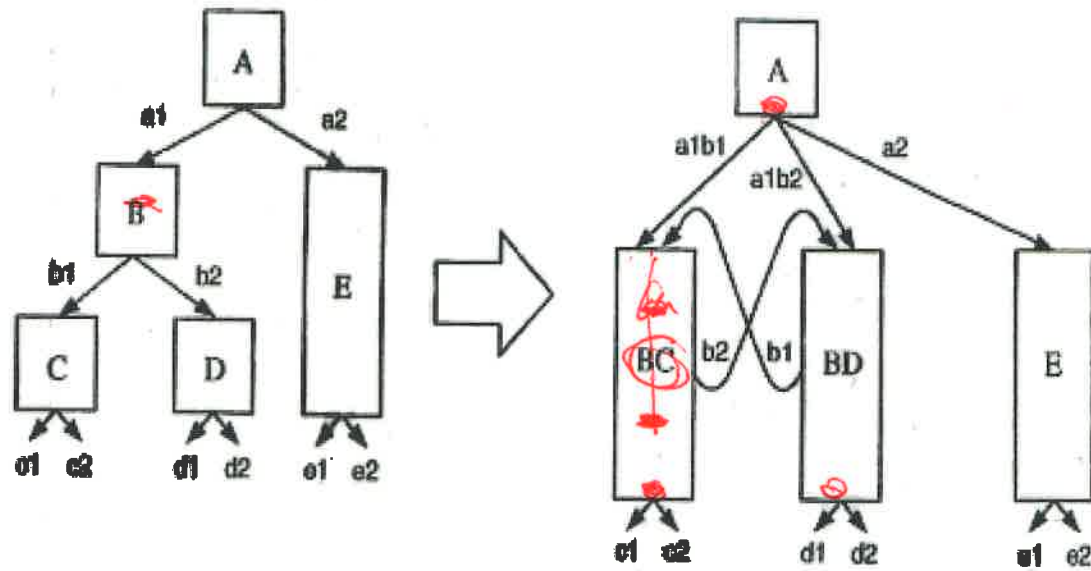
~~Supra~~
Hypra block
Scott ~~MAHUKS~~



HAWMOCKS



Enlarging Basic Blocks



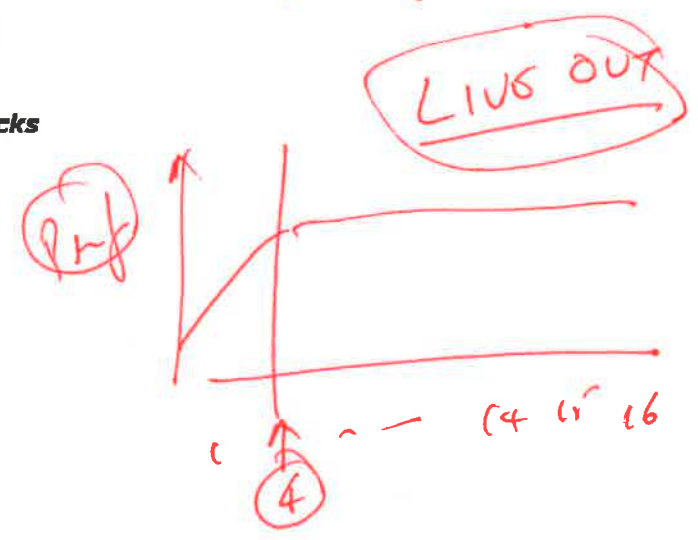
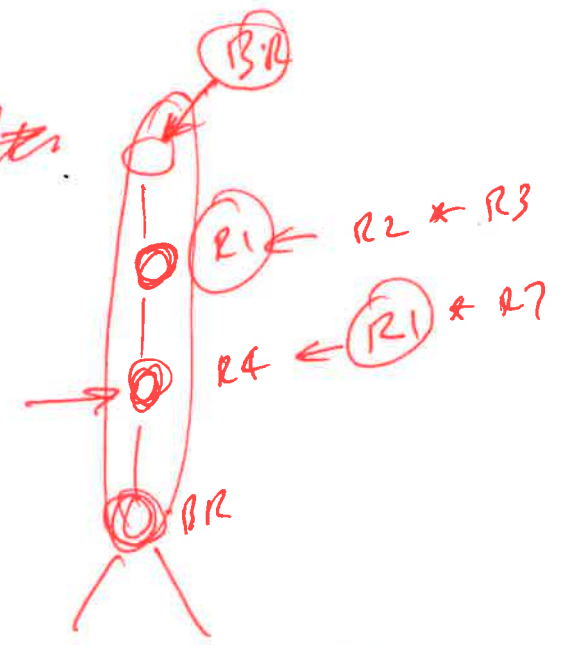
LIVES IN

Block-Structured ISA

* **References:**

- Stephen Melvin (PhD, Berkeley, 1991)
- Eric Hao (PhD, Michigan, 1997)
- ISC paper, Melvin and Patt, 1989
- ISCA paper, Melvin and Patt, 1991
- Micro-29, Hao, Chang, Evers, Patt, 1996

- * **The Atomic Unit of Processing**
- * **Enlarged Blocks**
- * **Savings on Register Pressure**
- * **Faulting Branches, Trapping Branches**
- * **Serial Execution on Exception**
- * **Comparison to Superblocks, Hyperblocks**



Wish Branches

- ***Compile-time and Run-time***
- ***At compile time:***
 - ***Does predication even make sense***
 - ***If no, regular branch and branch prediction***
 - ***If yes, mark wish branch and defer to run-time***
- ***At run time:***
 - ***Prediction accuracy low: predicate***
 - ***Prediction accuracy high: branch predict***