Computer Architecture: Fundamentals, Tradeoffs, Challenges

Chapter 5: The Process

Yale Patt
The University of Texas at Austin

Austin, Texas
Spring, 2023

Outline

- ***The unit of processing as viewed by the O/S***
- ***Process specific state***
  - ***Contents (e.g., PC, PSR)***
  - ***Saving/Restoring state***
- ***Interrupts and Exceptions***
  - ***Similarities***
  - ***Differences***

The Process State

- ***Contains***
  - ***PC, PSR, General Purpose Registers***
  - ***Other ISA specific stuff (e.g., x86 segment regs.)***
  - ***Virtual memory process-specific registers***
- ***Context switch: saves and loads process state***

The Processor Status Register

- ***Minimally:***
  - ***Priority level***
  - ***Privilege level***
  - ***Condition Codes (why?)***
- ***Other examples in some machines***
  - ***Arm: T bit***
  - ***VAX: Compatibility mode bit***
  - ***x86: Auxiliary flag used for BCD arithmetic***
  - ***THUMB: The 8-bit field of the IT instruction***

Priority and Privilege

- ***Priority (sense of urgency)***
  - ***Lowest: user mode***
  - ***Highest: machine check***
  - ***Second highest: power fail***

- ***Privilege (the right to do something)***
  - ***Right to execute certain instructions (e.g., RTI)***
  - ***Right to access privileged memory***

- ***Orthogonal issues (the mail clerk in the basement)***

Interrupts and Exceptions

- **Similarities**
  - Stop the executing process (What to do with it?)
    - Finish or Back up
      - Exceptions: traps vs faults
      - Interrupts: importance of interrupt latency
    - What if you can't do either? (e.g., "Commercial instructions")
  - Put the machine in a consistent state
  - Vector to the starting address of the service routine
  - Upon completion, return to the interrupted process
- **Differences**

Interrupts		Exceptions
External	cause	Internal
As convenient	when	When detected
Almost all	maskable	Almost none
System	context	Process
Depends	priority	Unchanged

Dhanyavaad!