

Table C.1 Data Path Control Signals

Signal Name	Signal Values	
LD.MAR/1:	NO, LOAD	
LD.MDR/1:	NO, LOAD	
LD.IR/1:	NO, LOAD	
LD.BEN/1:	NO, LOAD	
LD.REG/1:	NO, LOAD	
LD.CC/1:	NO, LOAD	
LD.PC/1:	NO, LOAD	
LD.Priv/1:	NO, LOAD	
LD.Priority/1:	NO, LOAD	
LD.SavedSSP/1:	NO, LOAD	
LD.SavedUSP/1:	NO, LOAD	
LD.ACV/1:	NO, LOAD	
LD.Vector/1:	NO, LOAD	
GatePC/1:	NO, YES	
GateMDR/1:	NO, YES	
GateALU/1:	NO, YES	
GateMARMUX/1:	NO, YES	
GateVector/1:	NO, YES	
GatePC-1/1:	NO, YES	
GatePSR/1:	NO, YES	
GateSP/1:	NO, YES	
PCMUX/2:	PC+1 BUS ADDER	;select pc+1 ;select value from bus ;select output of address adder
DRMUX/2:	11,9 R7 SP	;destination IR[11:9] ;destination R7 ;destination R6
SR1MUX/2:	11,9 8,6 SP	;source IR[11:9] ;source IR[8:6] ;source R6
ADDR1MUX/1:	PC, BaseR	
ADDR2MUX/2:	ZERO offset6 PCoffset9 PCoffset11	;select the value zero ;select SEXT[IR[5:0]] ;select SEXT[IR[8:0]] ;select SEXT[IR[10:0]]
SPMUX/2:	SP+1 SP-1 Saved SSP Saved USP	;select stack pointer+1 ;select stack pointer-1 ;select saved Supervisor Stack Pointer ;select saved User Stack Pointer
MARMUX/1:	7,0 ADDER	;select ZEXT[IR[7:0]] ;select output of address adder
TableMUX/1:	x00, x01	
VectorMUX/2:	INTV Priv.exception Opc.exception ACV.exception	
PSRMUX/1:	individual settings, BUS	
ALUK/2:	ADD, AND, NOT, PASSA	
MIO.EN/1:	NO, YES	
R.W/1:	RD, WR	
Set.Priv/1:	0 1	;Supervisor mode ;User mode