Ch. 4

Basic Components Proc. Mem, I/O, Control

Components

Instruction Processing.

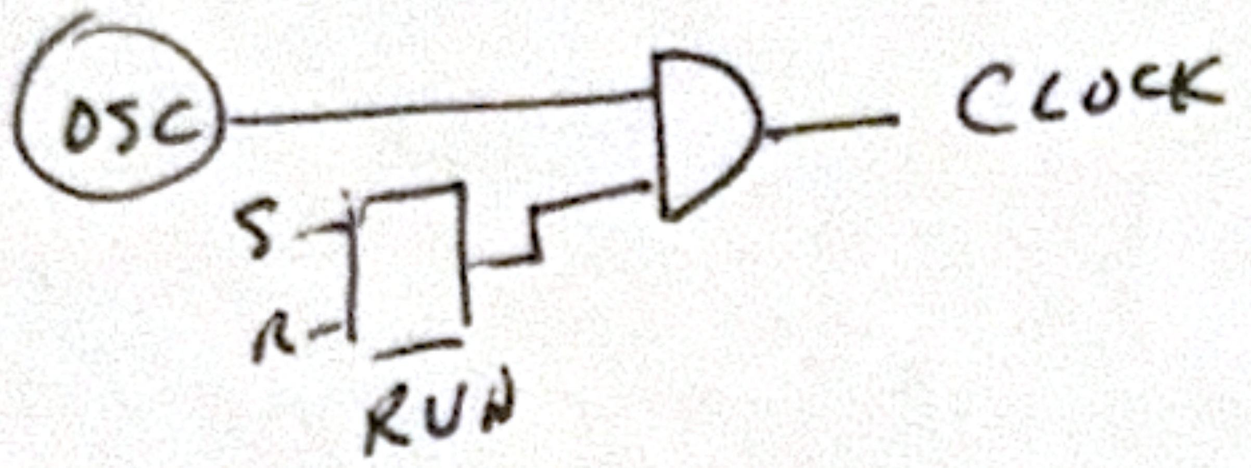
ADD, AND LD
0001, 0101 0010

Instructions F-D-

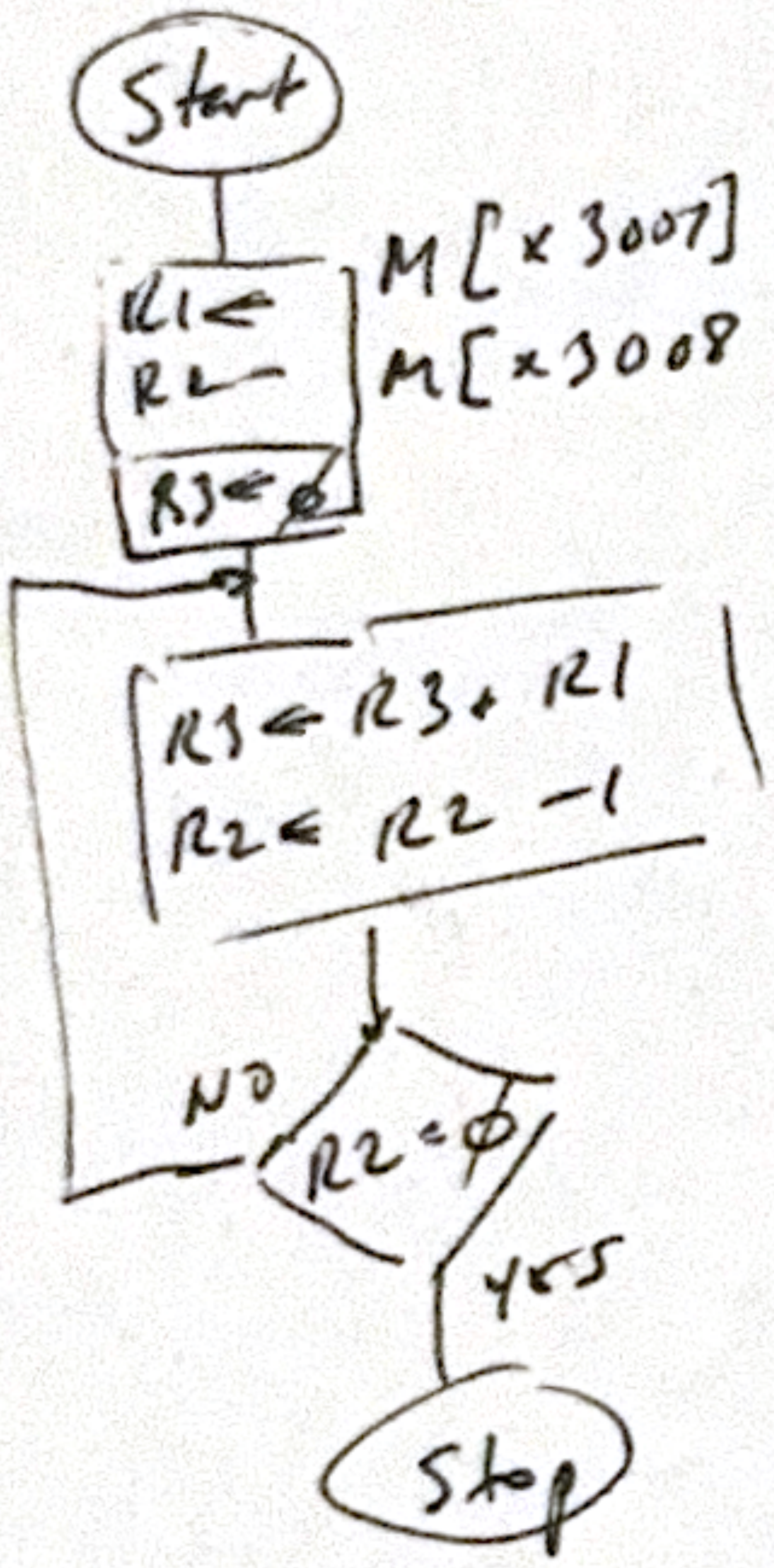
Instruction cycle Fetch, Decode, EA, Data, execute store ~~resul~~

Control – State machine

Halt



MUL



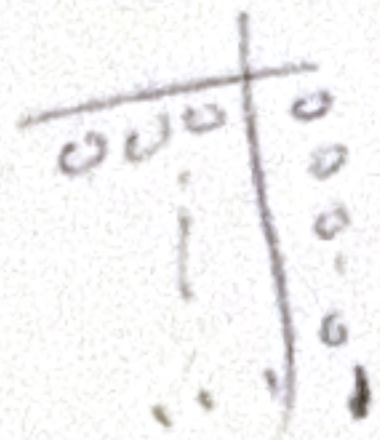
1. Progr…
2. Pr. Ctr…
3. Compr…

Transistor

Inverter

NAND

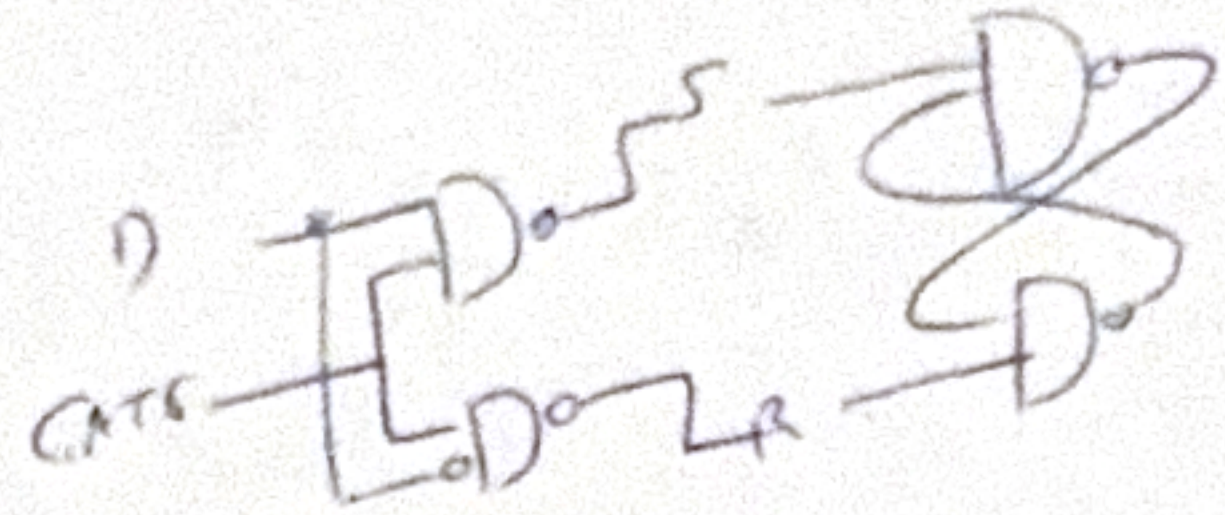
AND ← 3 input gates, logically complete



ADDER / MUX / DECODER

LATCH

GATED



ALARM CLOCK

MEMORY $2^2 \times 3$

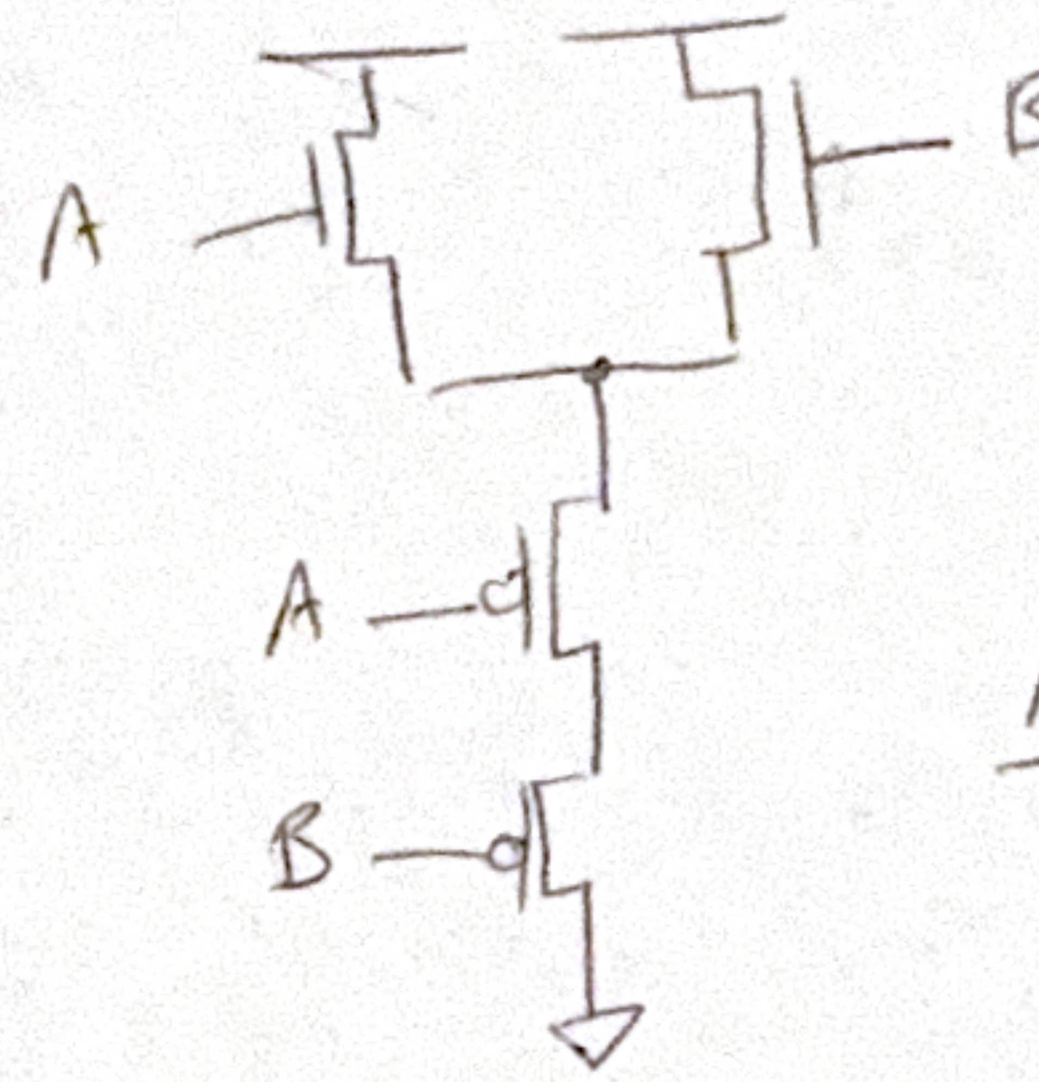
FSM (ASYNCH) — TIC/TAC/TOE, Ballgame, Coke Machine, Lock

The computer: State machine
(Data Path, μseq-control)

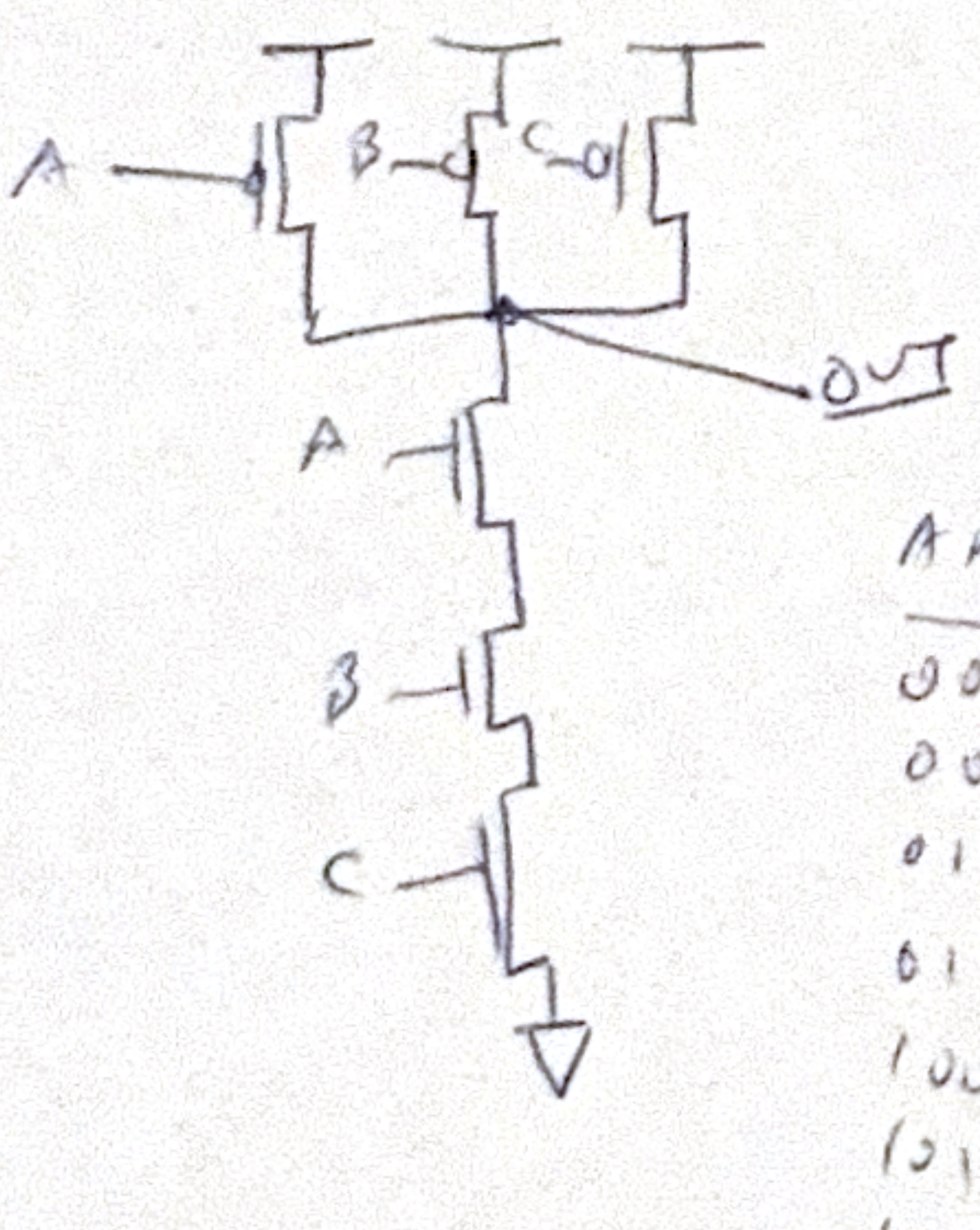
↑

Design Sign

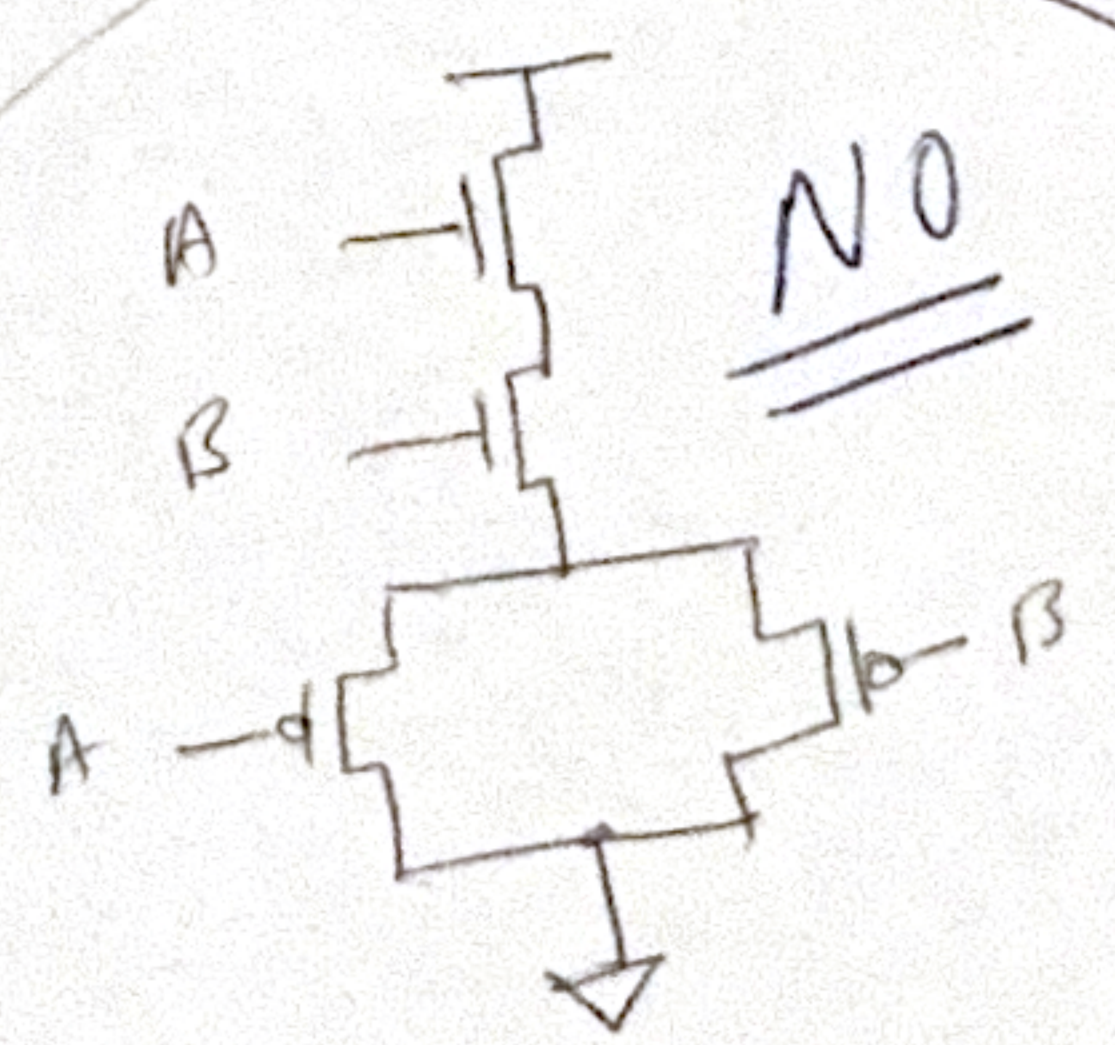
(Register)



A B	Q
0 0	0
0 1	1
1 0	1
1 1	1



A B C	
0 0 0	1
0 0 1	1
0 1 0	1
0 1 1	1
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	0



NO

A B	Q
0 0	0
0 1	0
1 0	0
1 1	1