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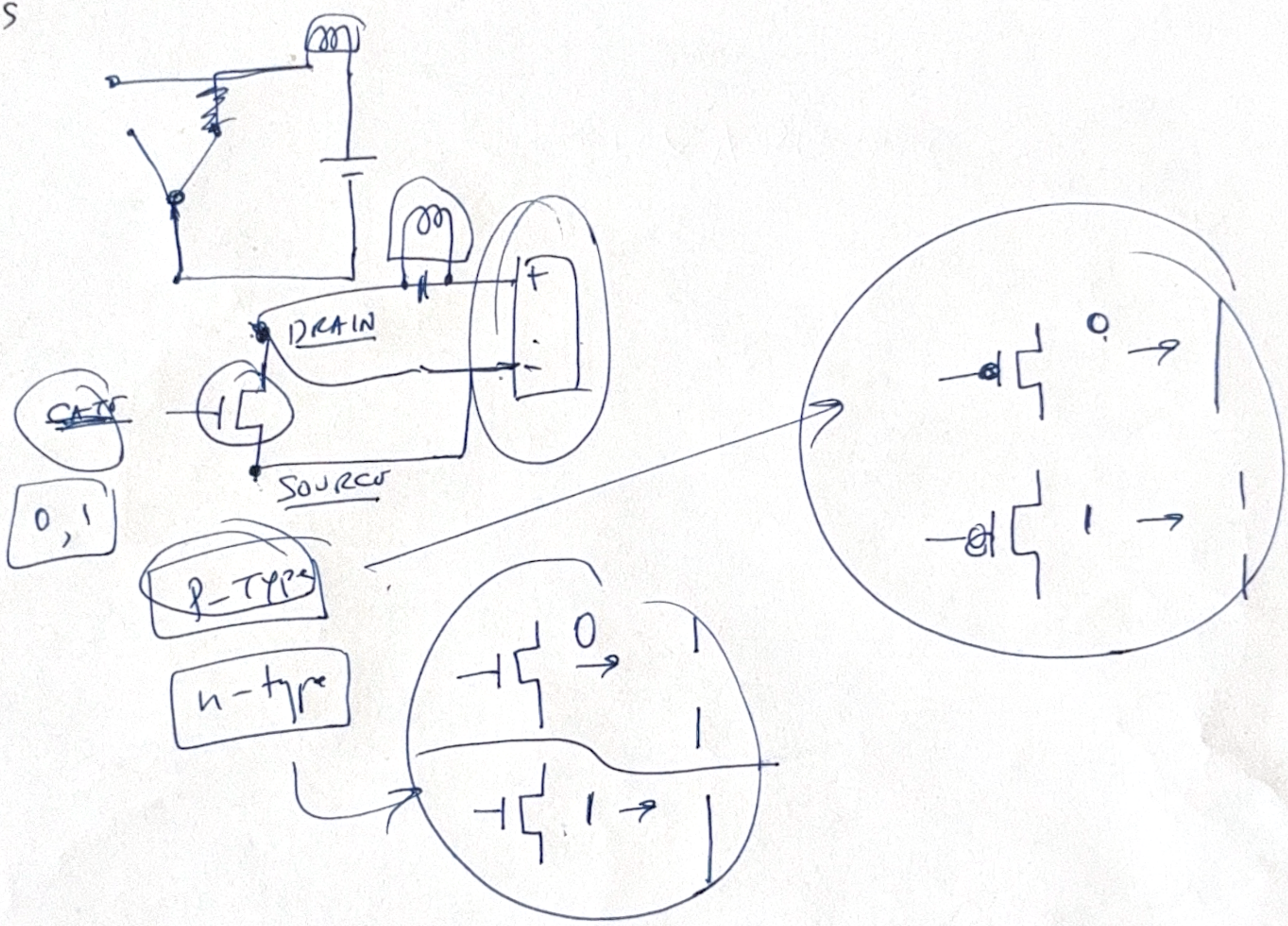
①



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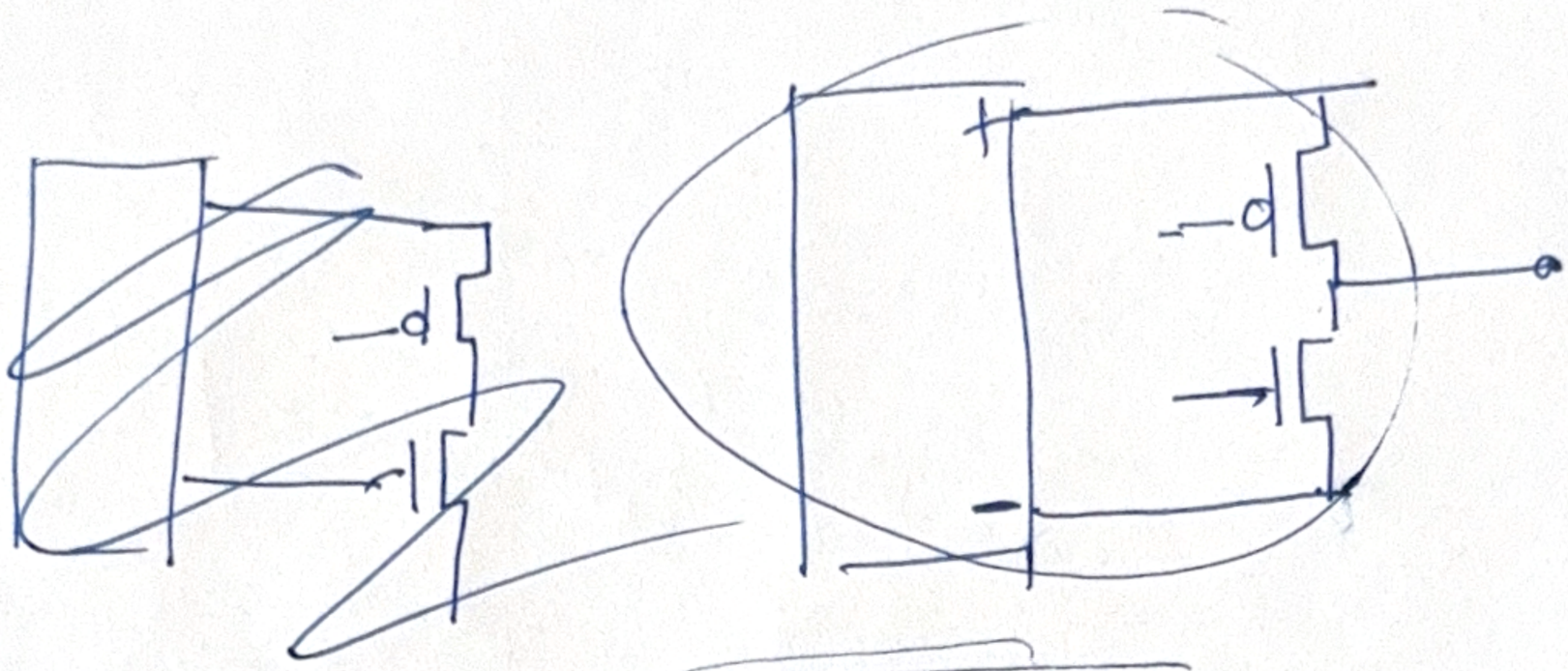
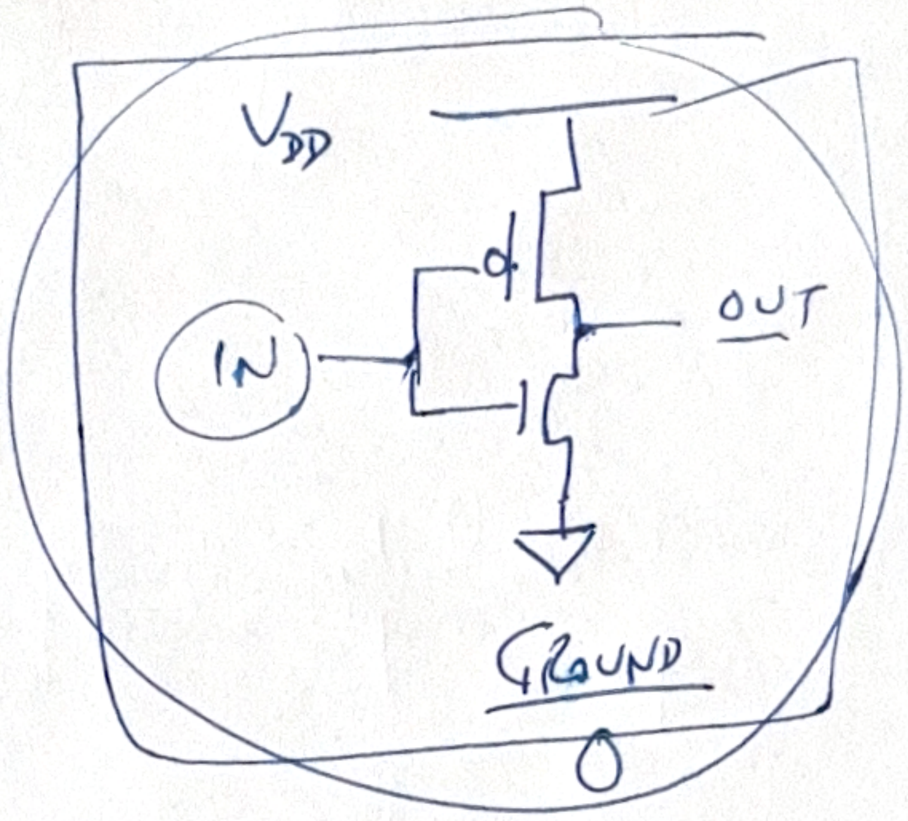
(2)

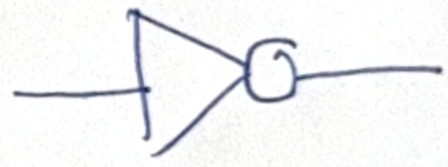




IN	OUT
0	1
1	0

INVERTER

NOT-gate



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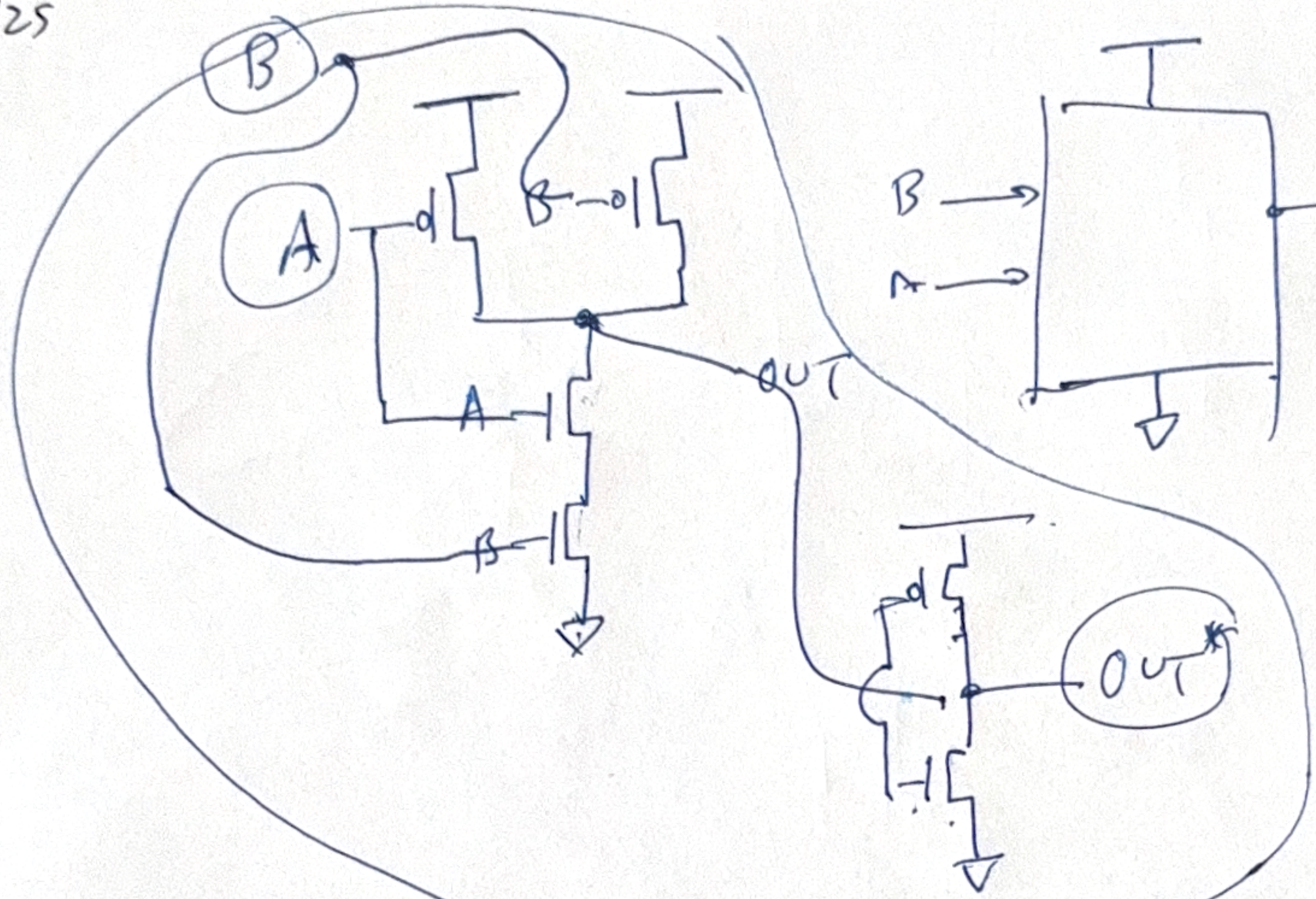
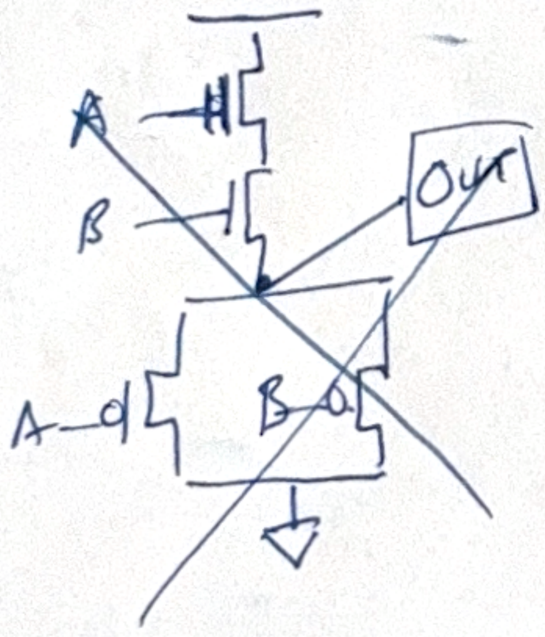
(3)



A	B	OUT	
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

NOT-AND

NAND



AND GATE

A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

TRANSMISSION VOLTAGE

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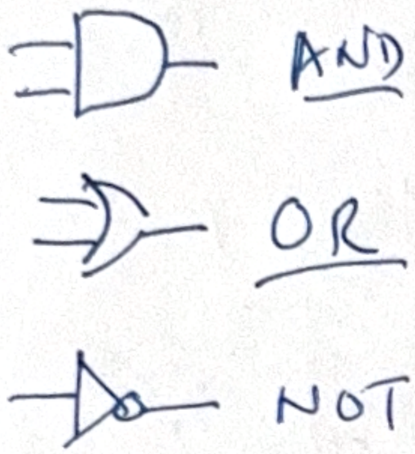
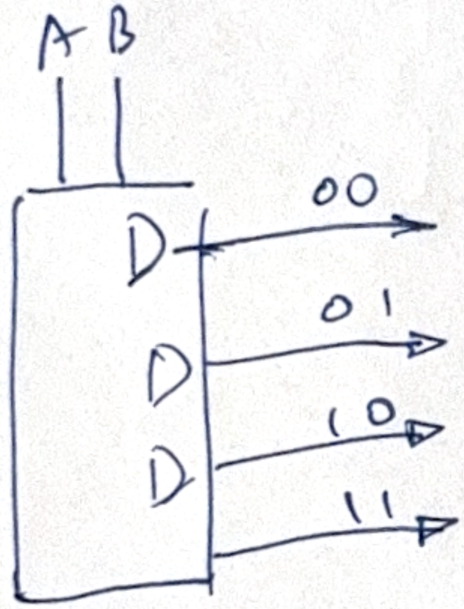
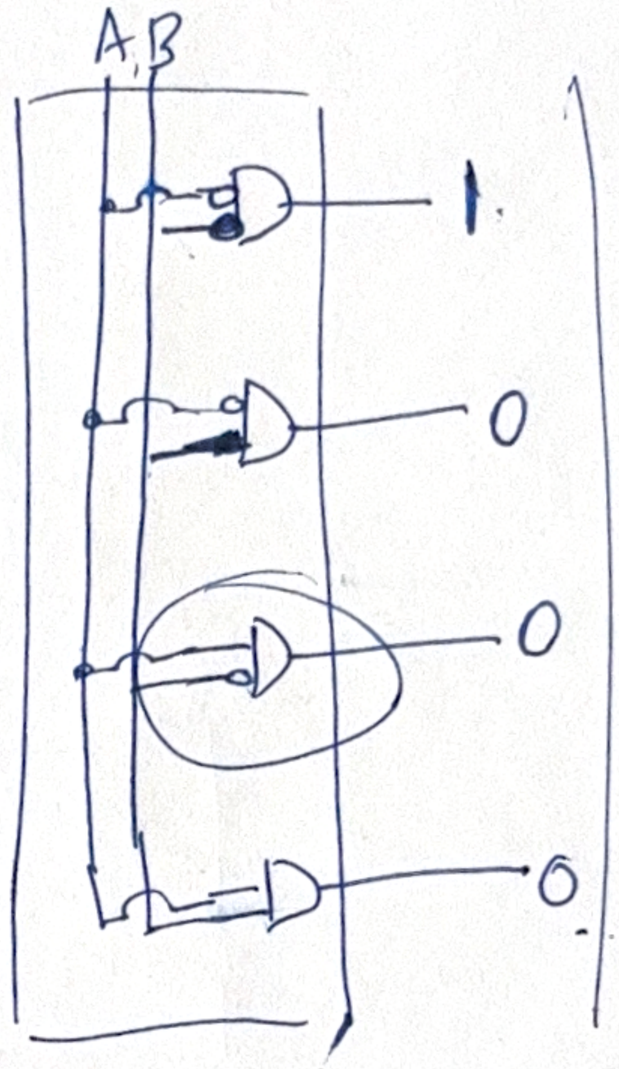
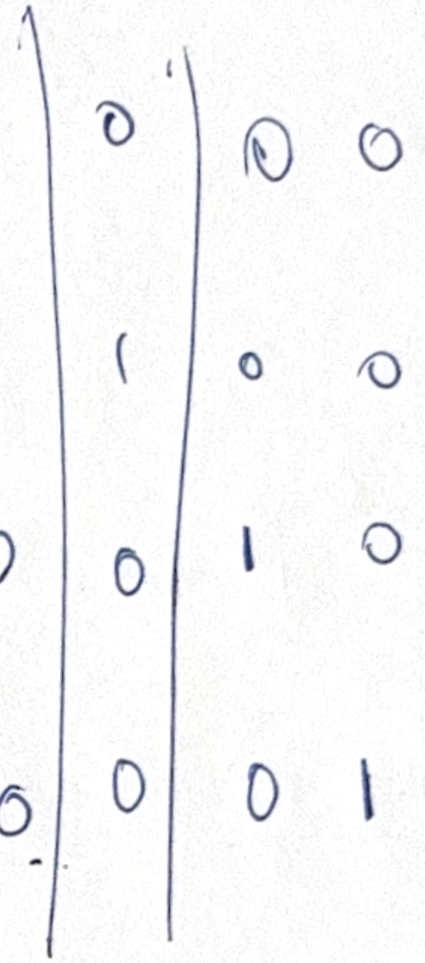
(4)

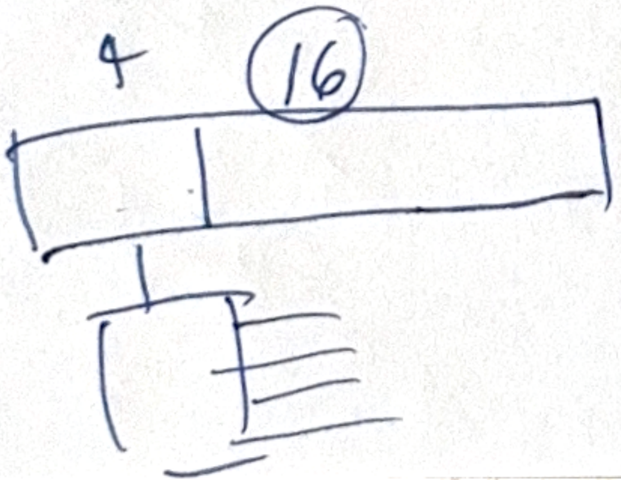








DECODER



01

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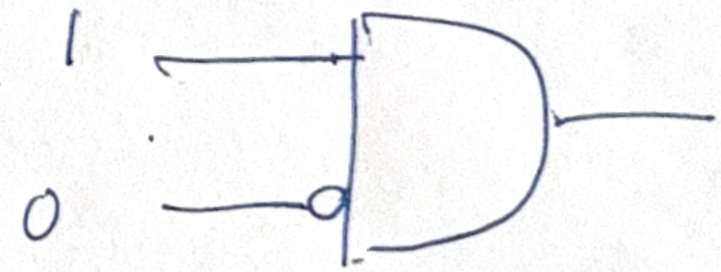

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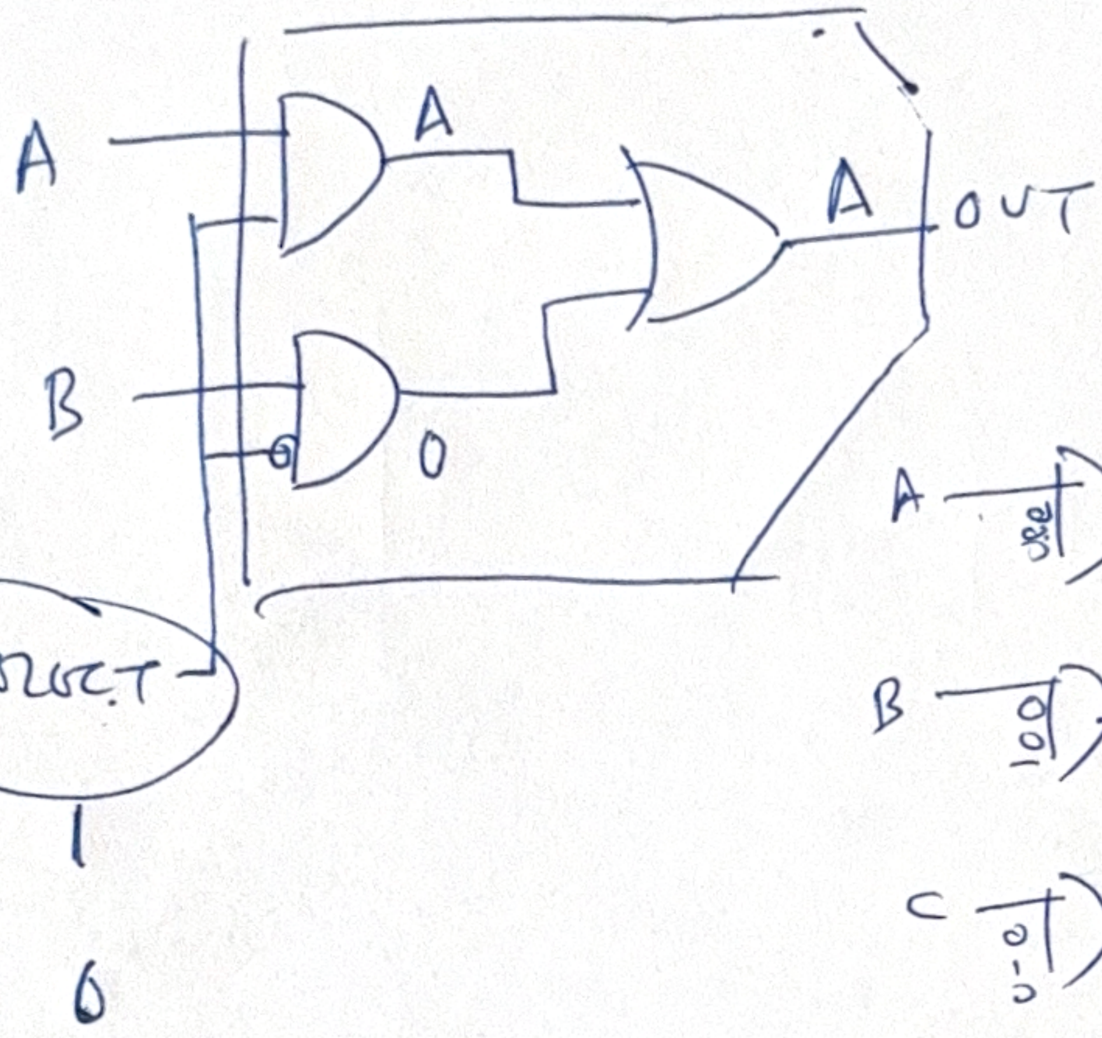
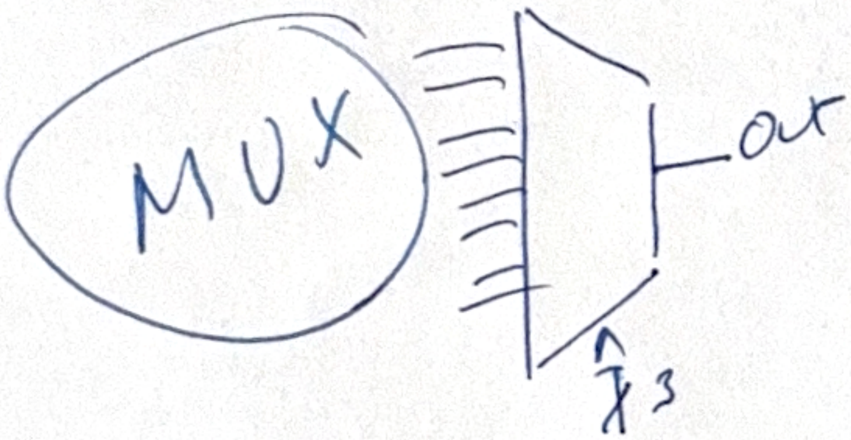
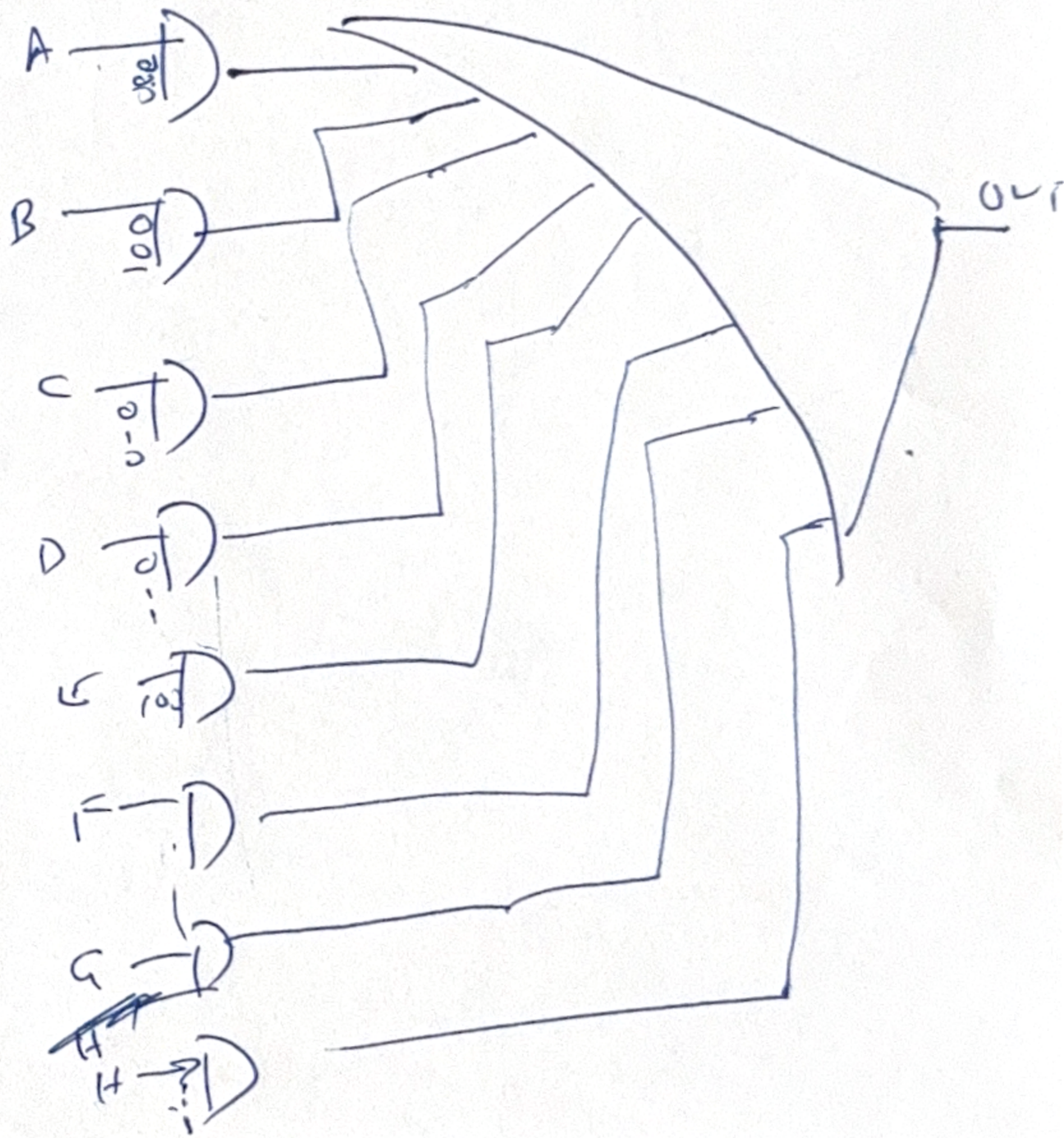
3.





SELECT



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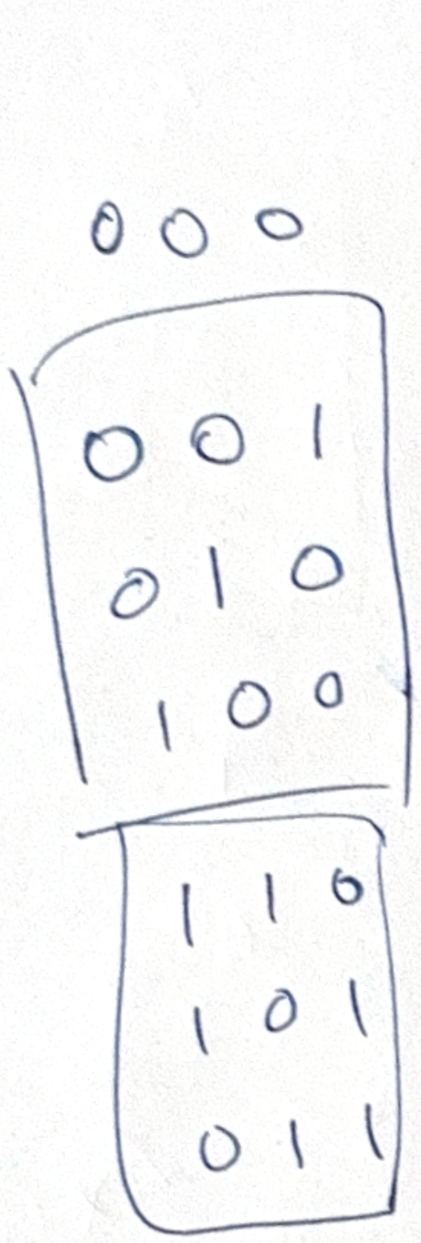
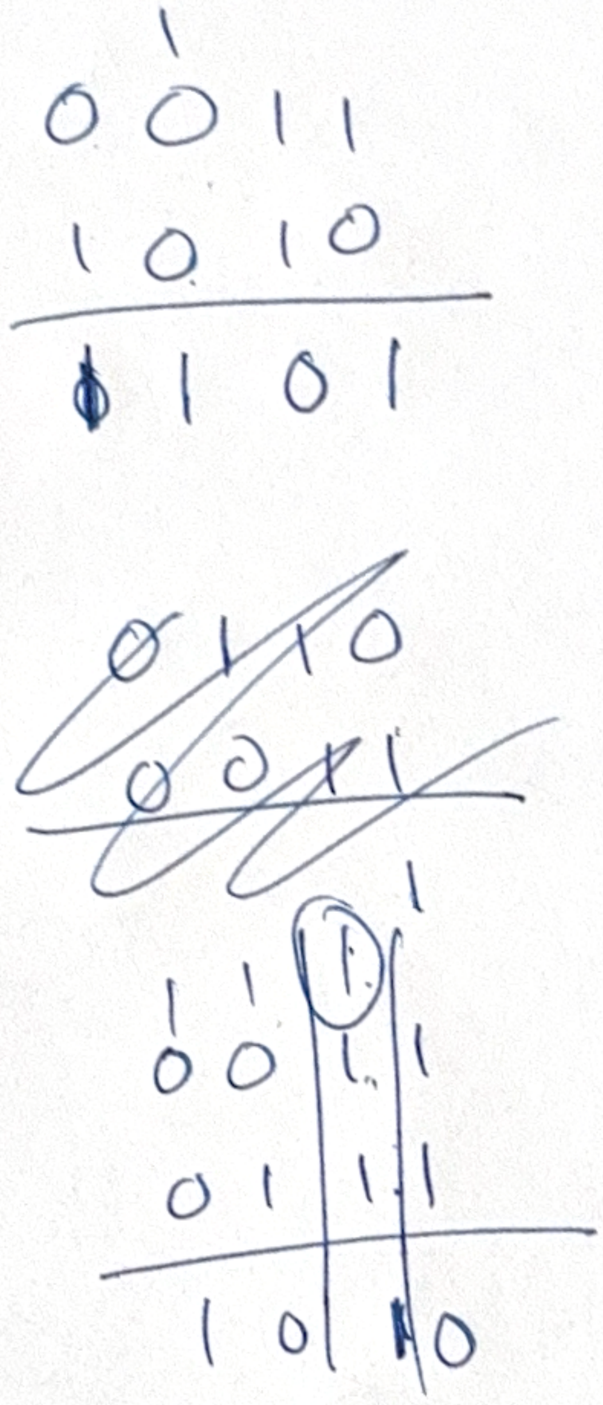
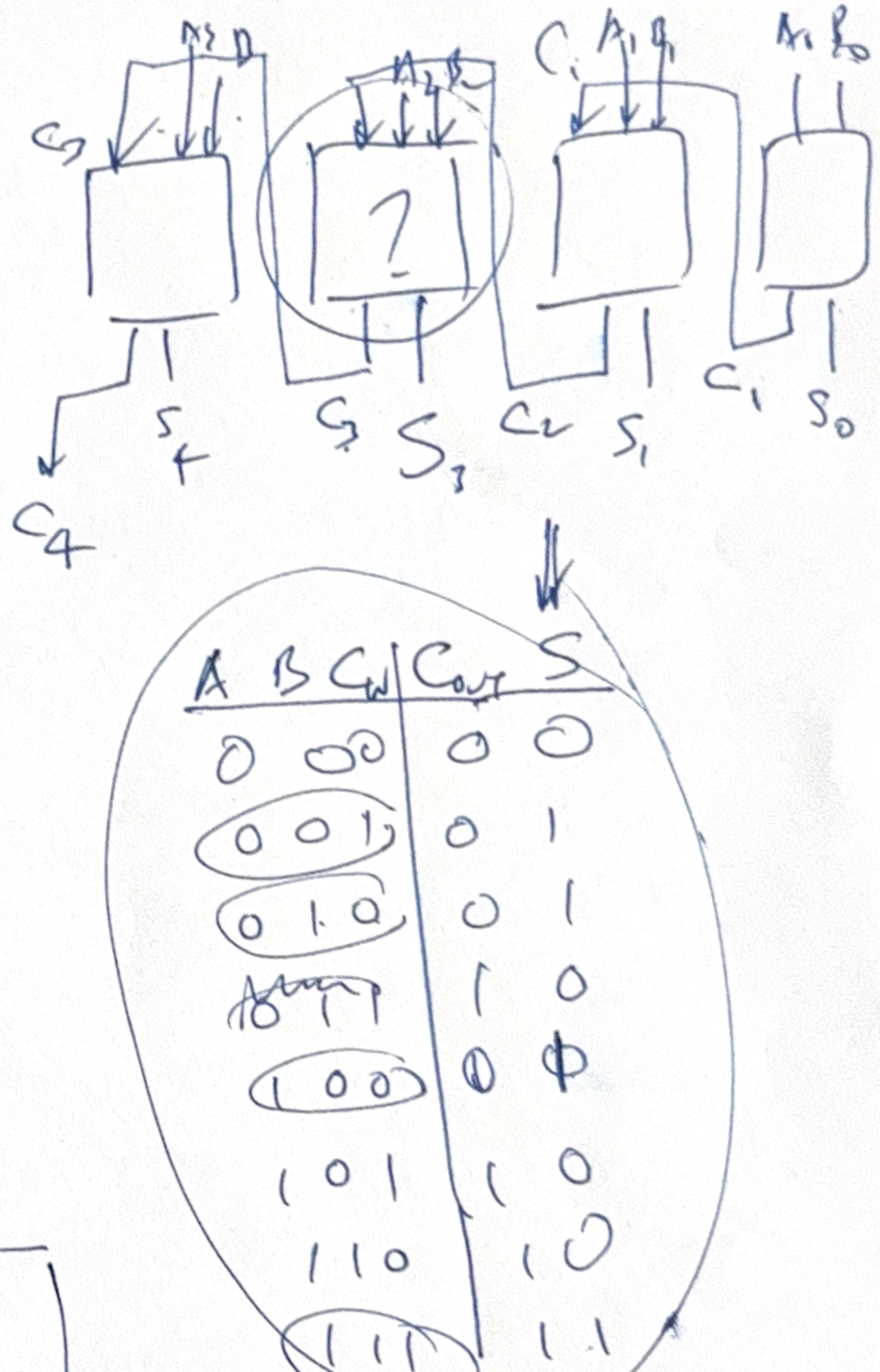
(6)







ONE BIT ADDER

FULL ADDER