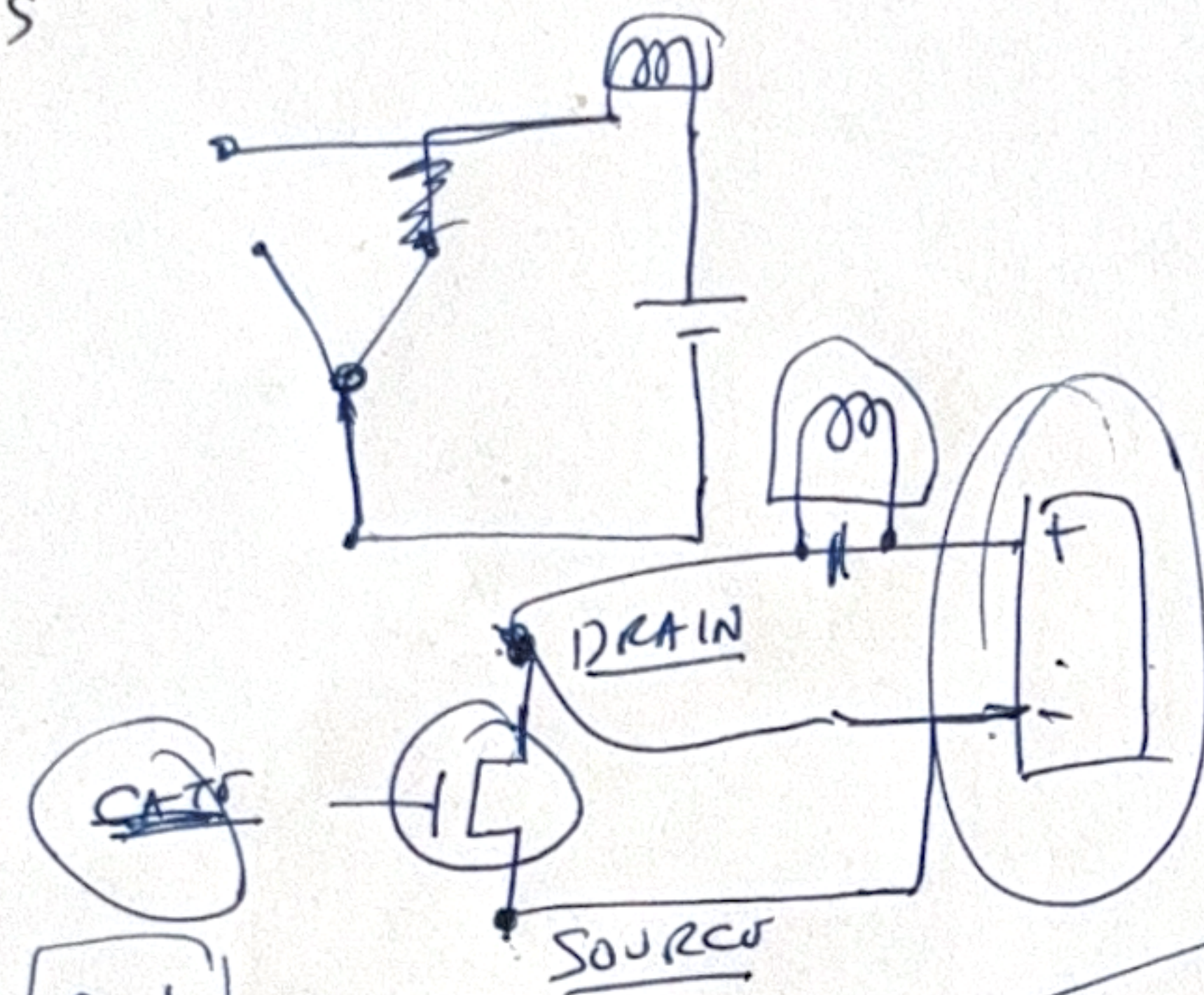


9/8/25

(1)

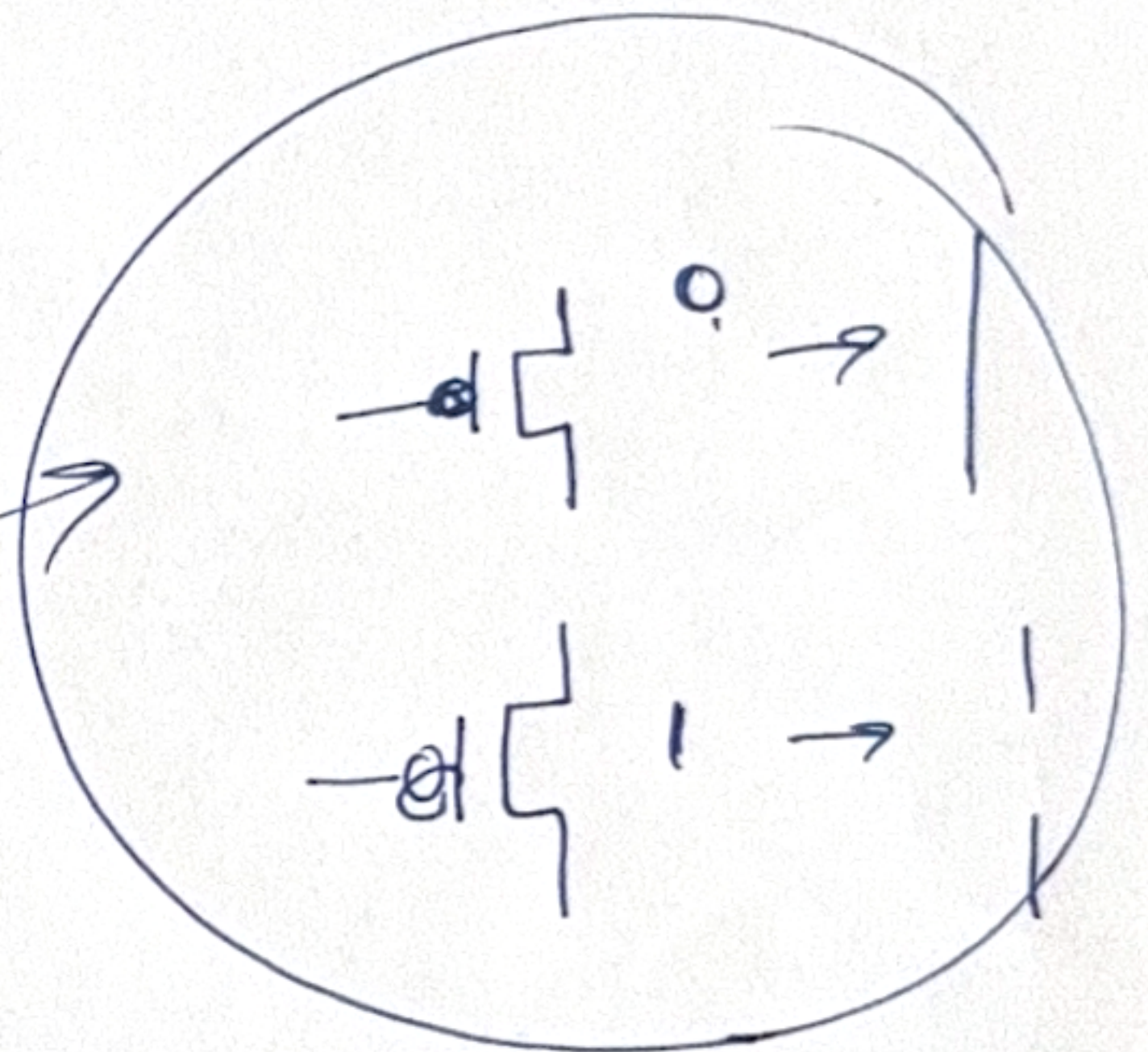
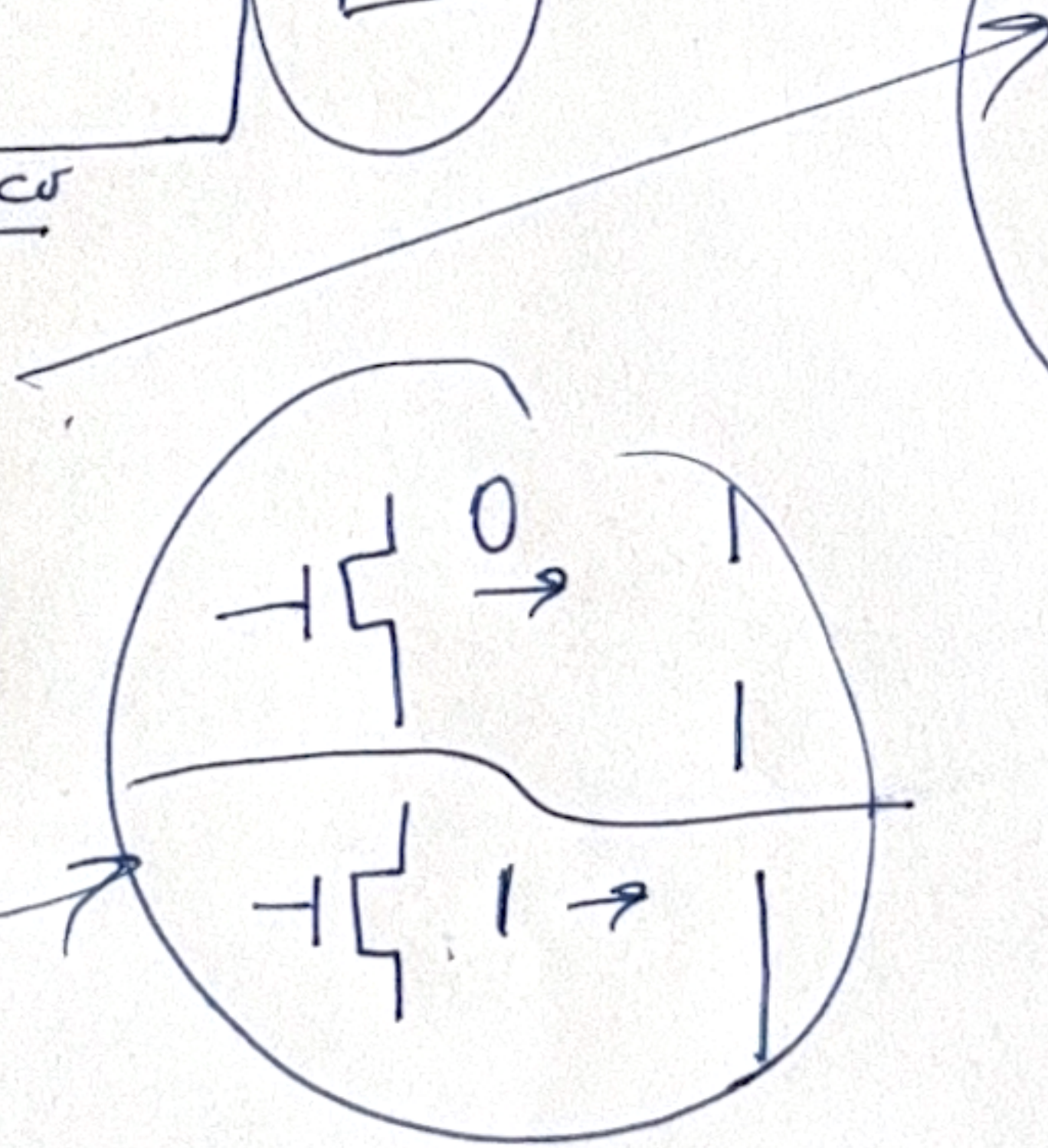


CATS

0, 1

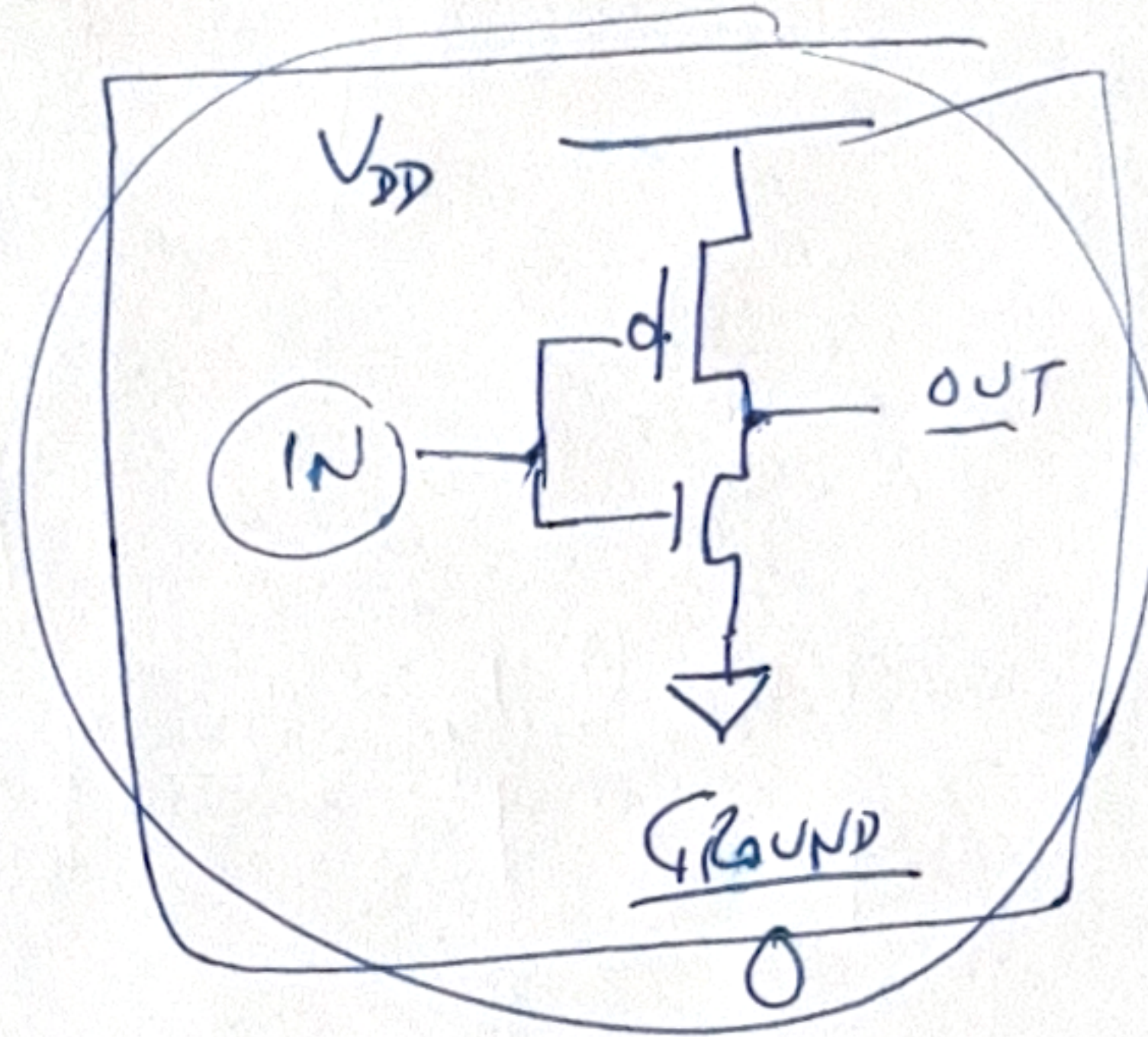
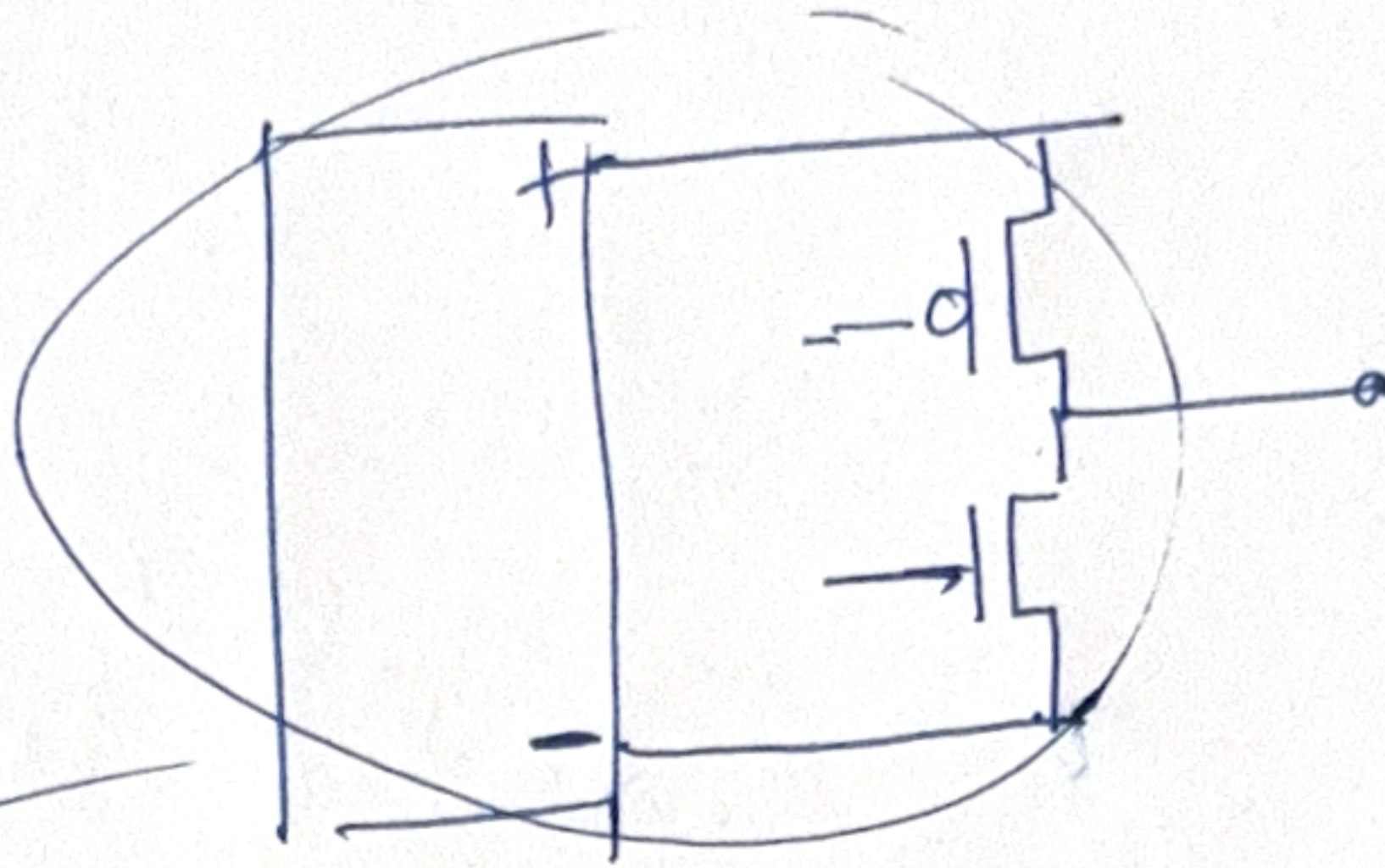
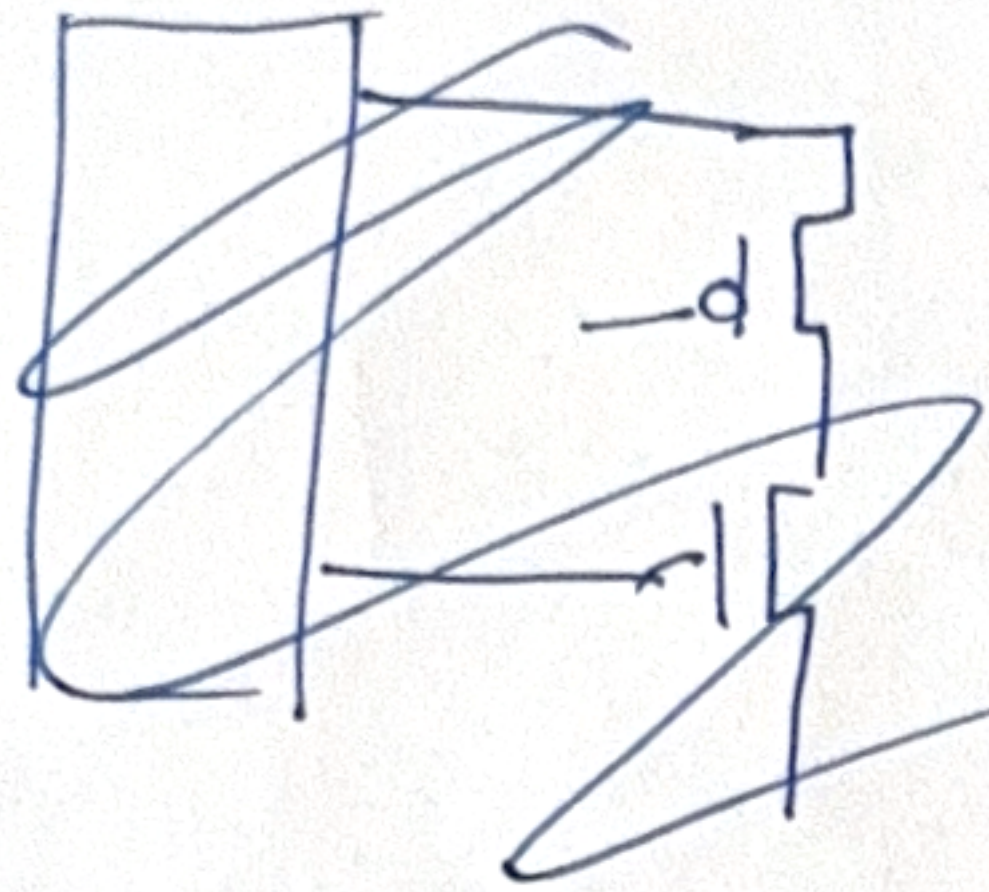
p-type

n-type



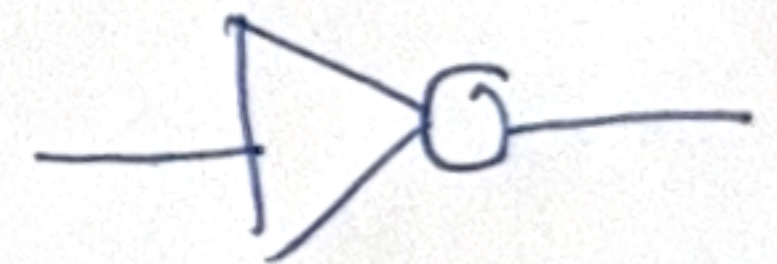
9/8/25

(2)



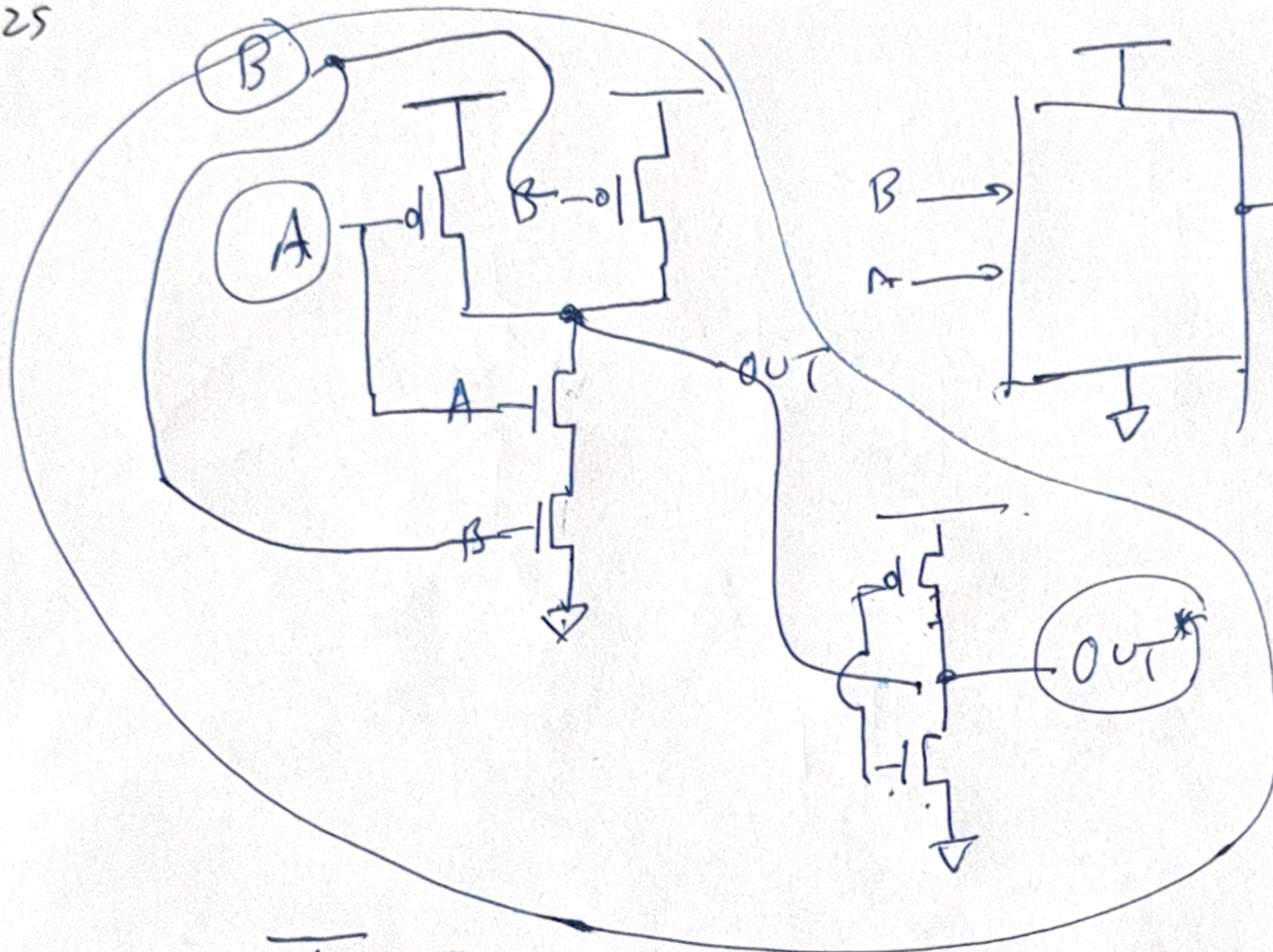
IN	OUT
0	1
1	0

INVERTER
NOT-gate



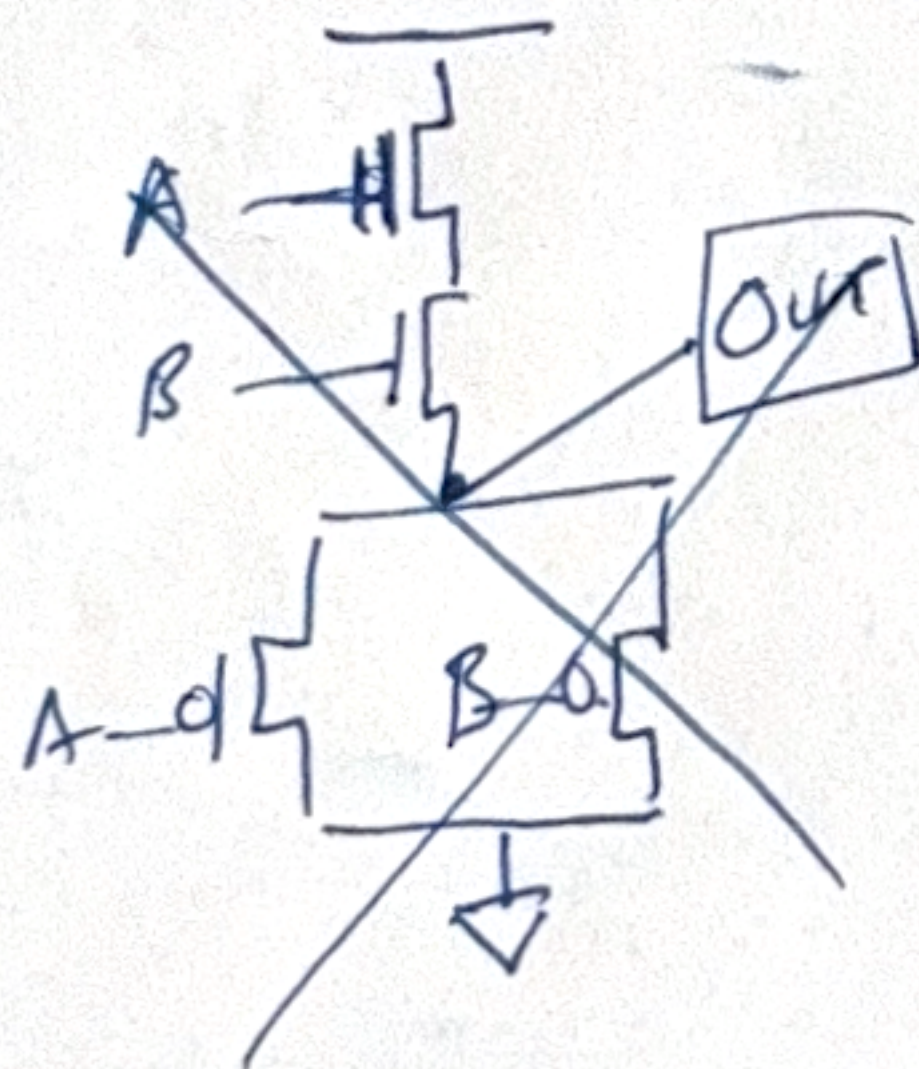
9/8/25

③



A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

NAND-AND
NAND



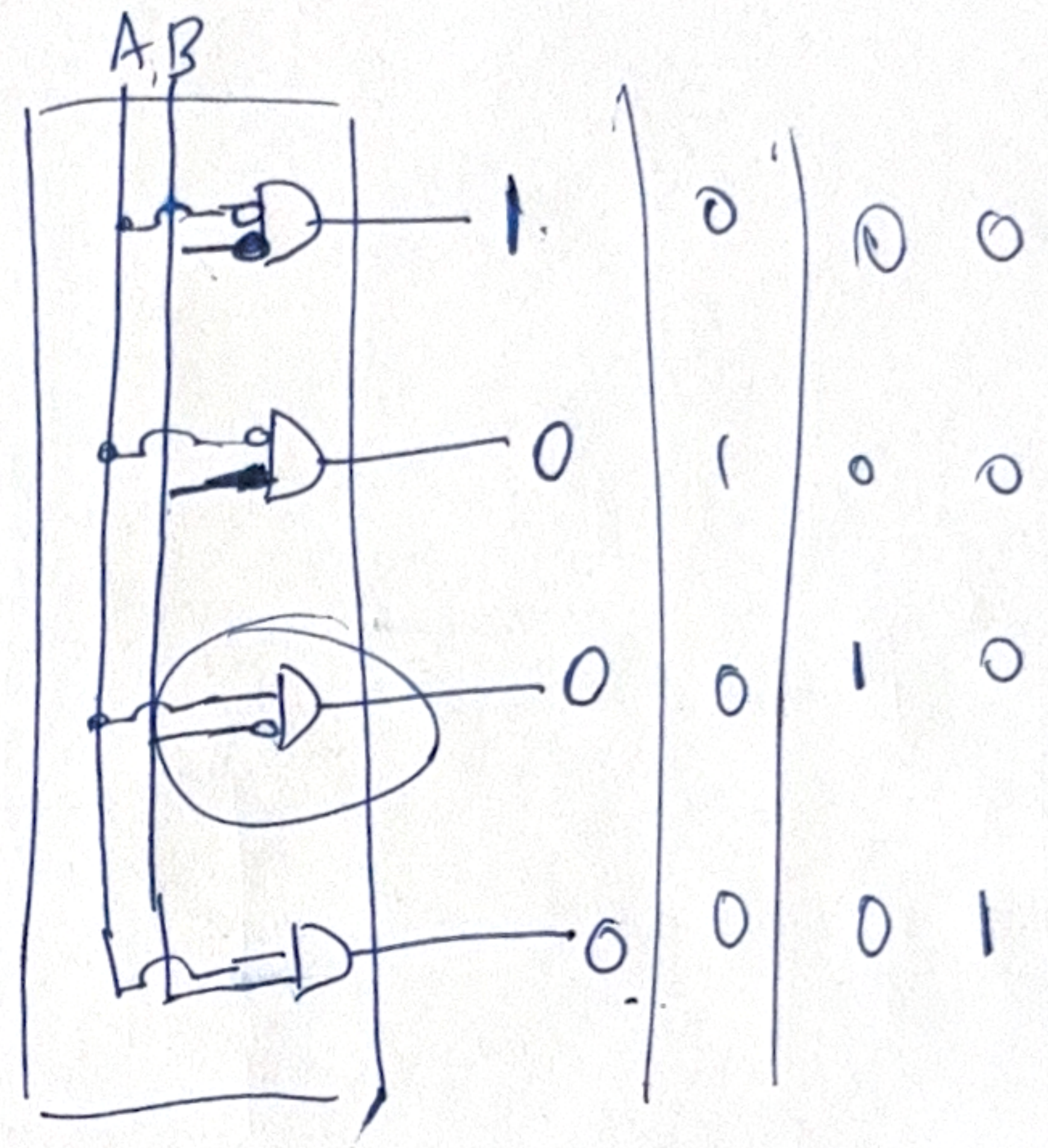
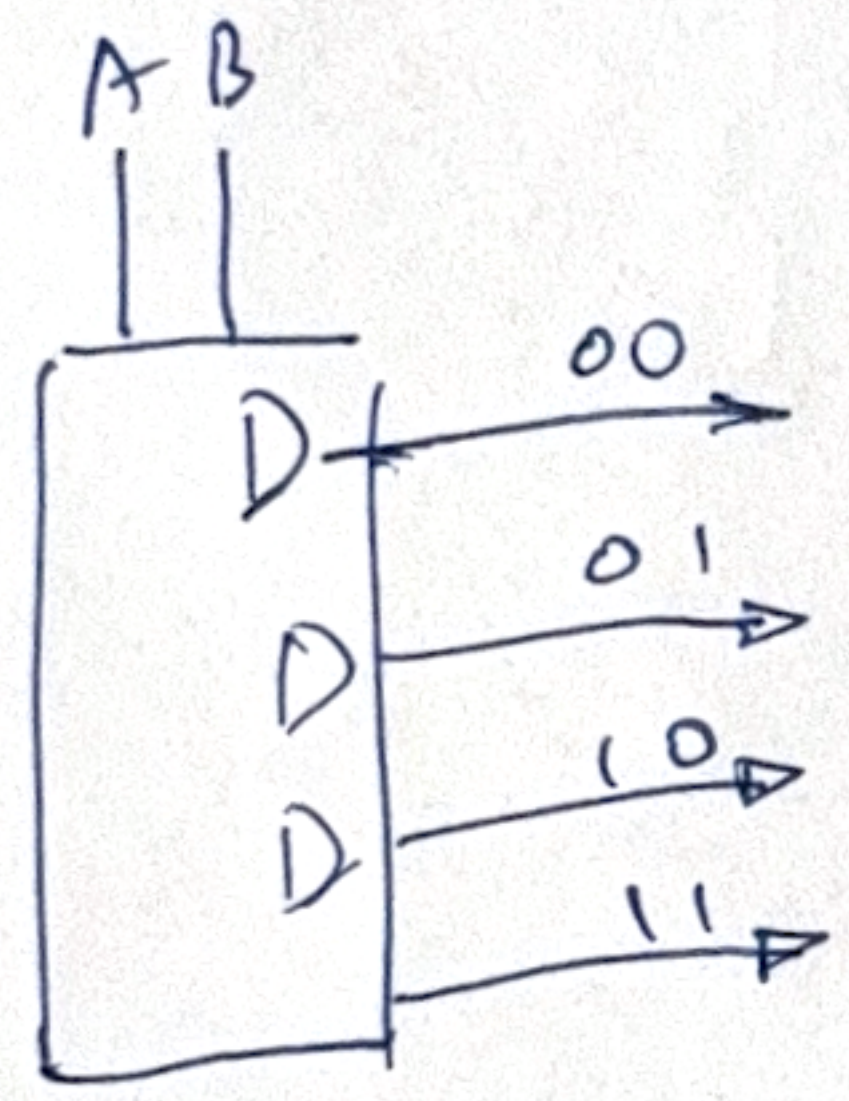
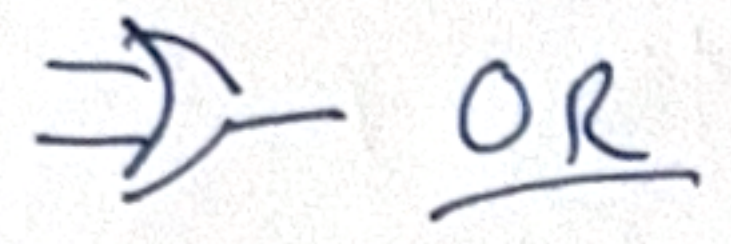
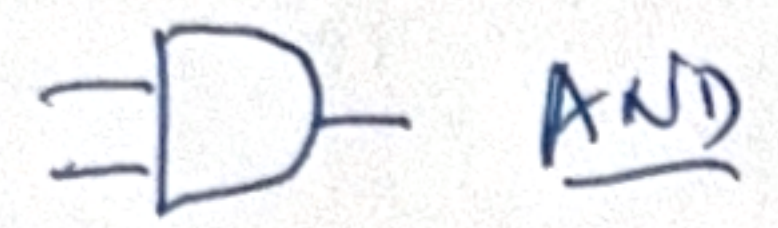
AND GATES

A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

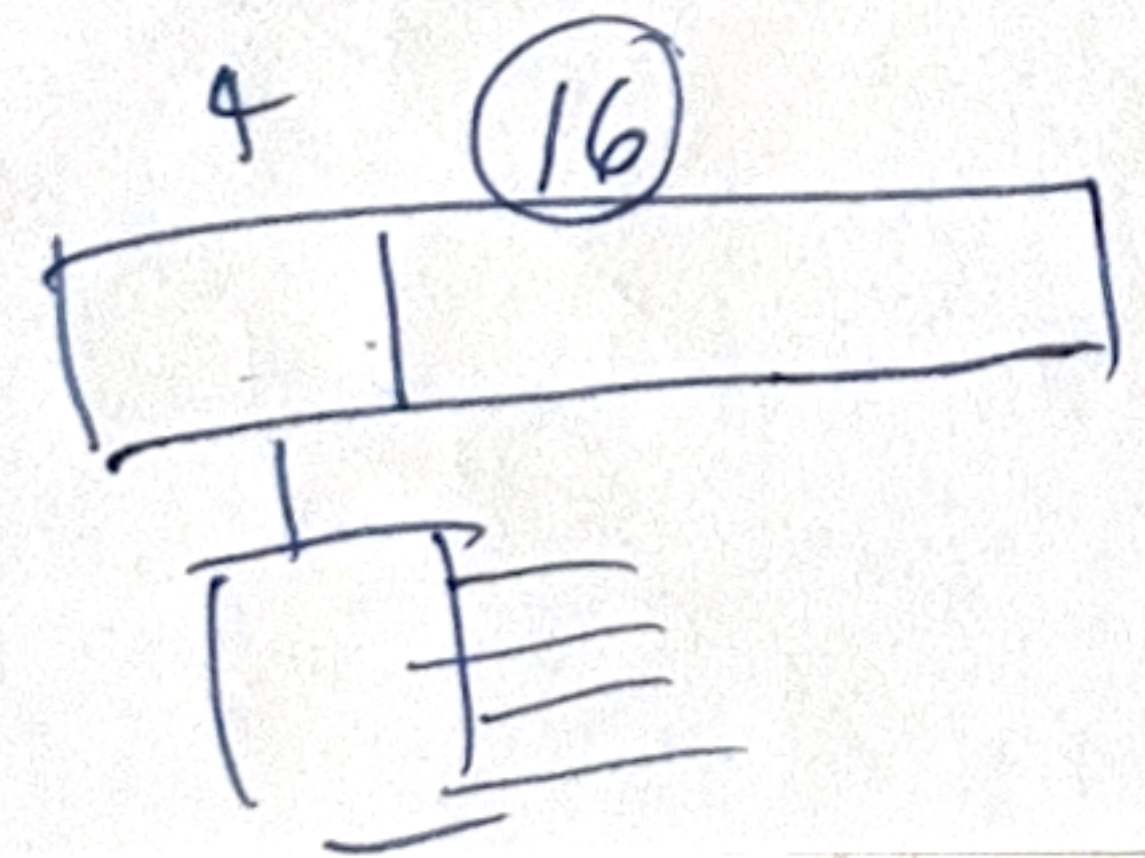
TRANSMISSION
VOLTAGES

9/8/25

(4)



DECODE

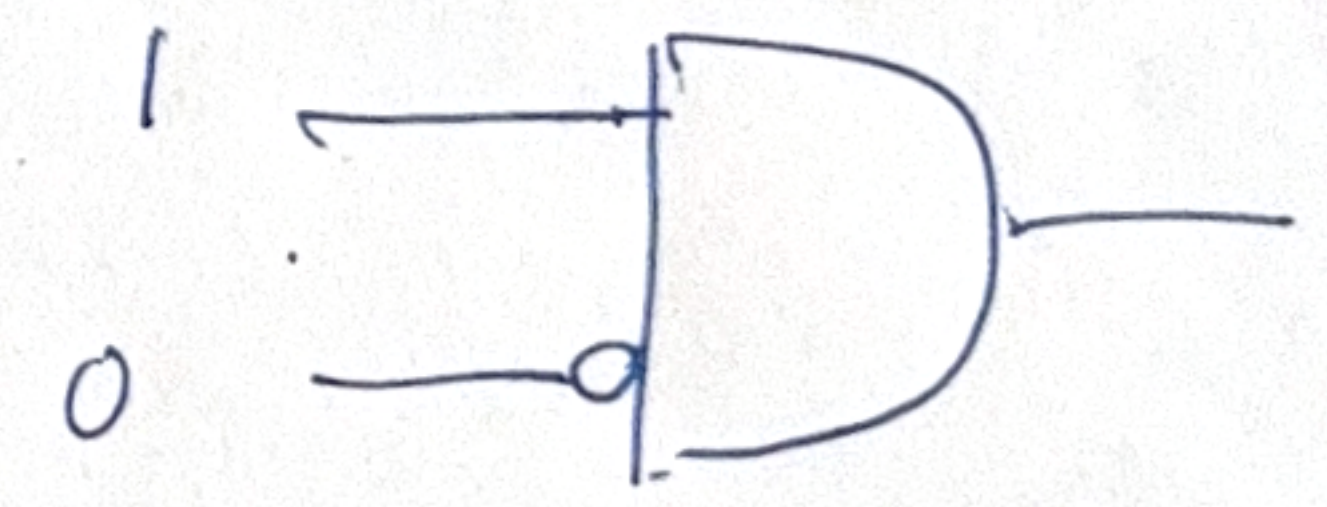


01

10

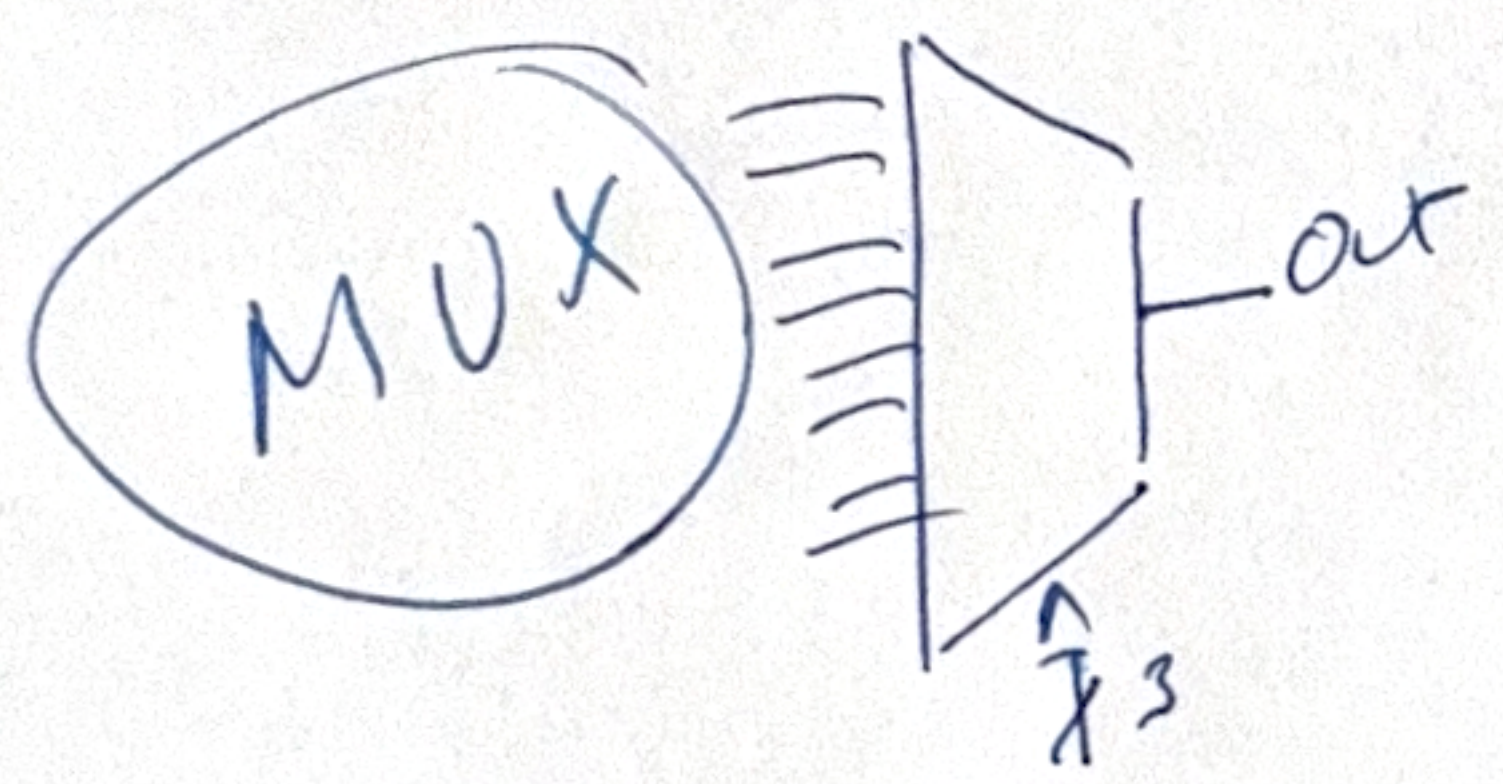
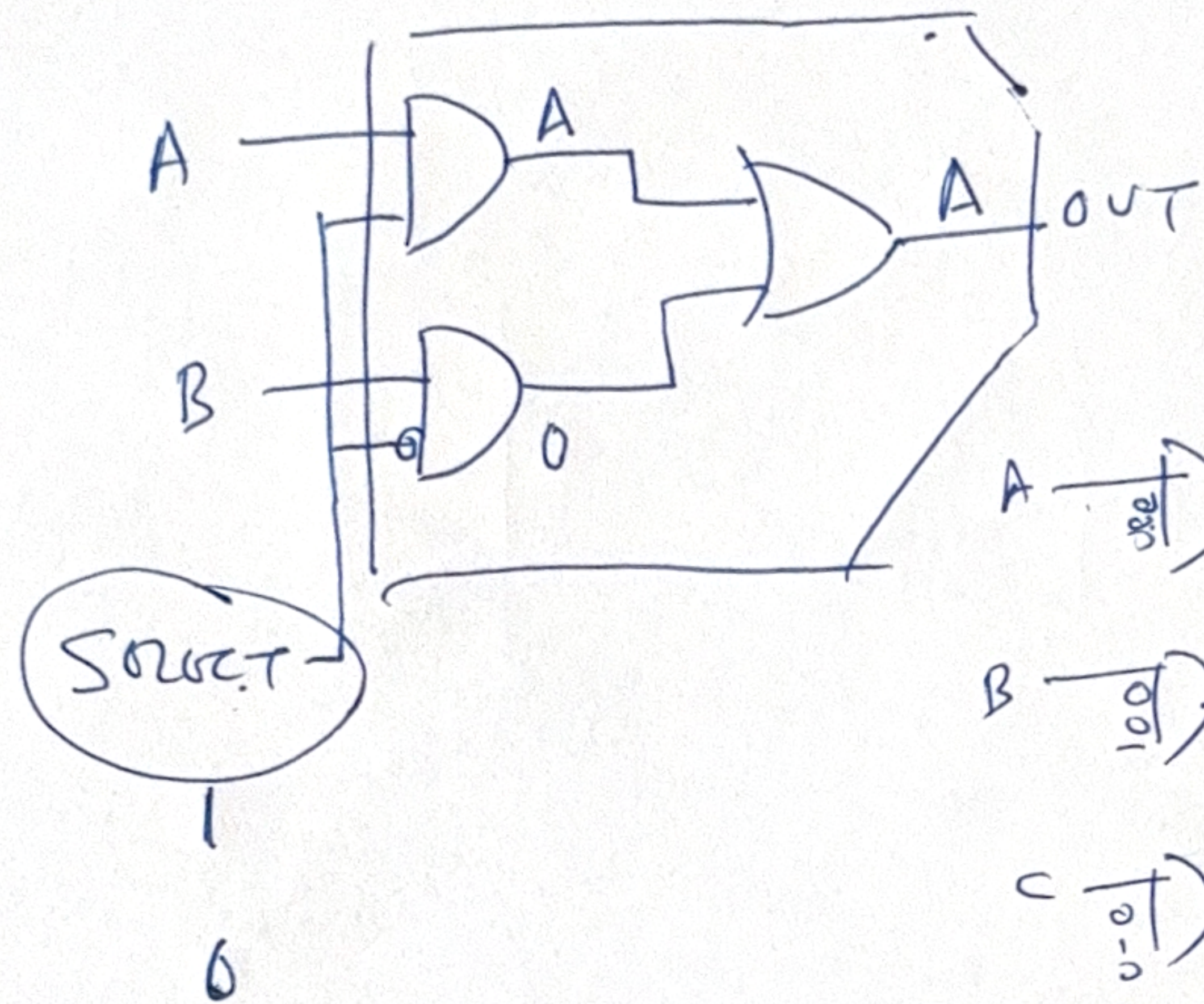
11

0001
1010

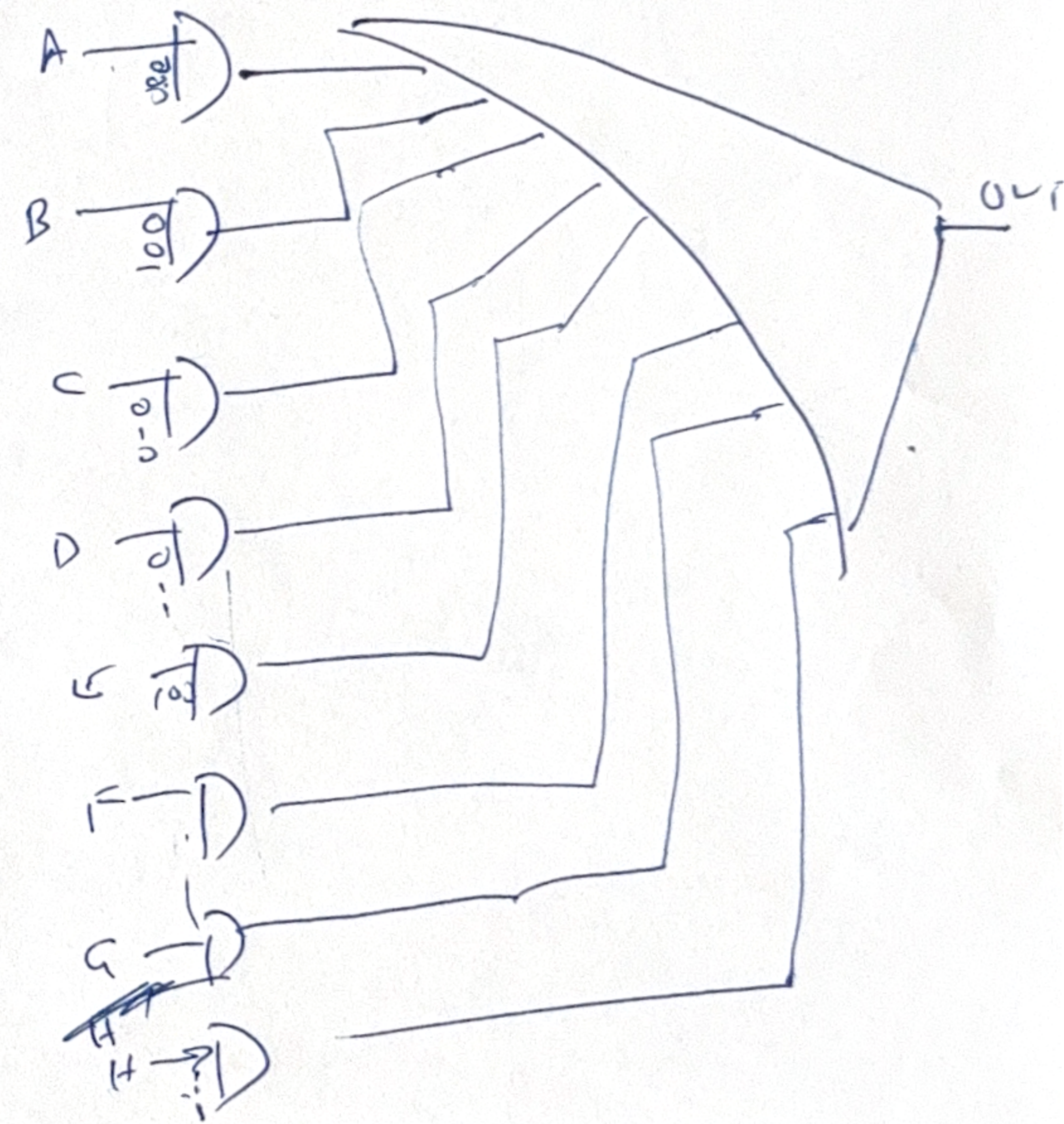


9/8/25
(5)

3/.

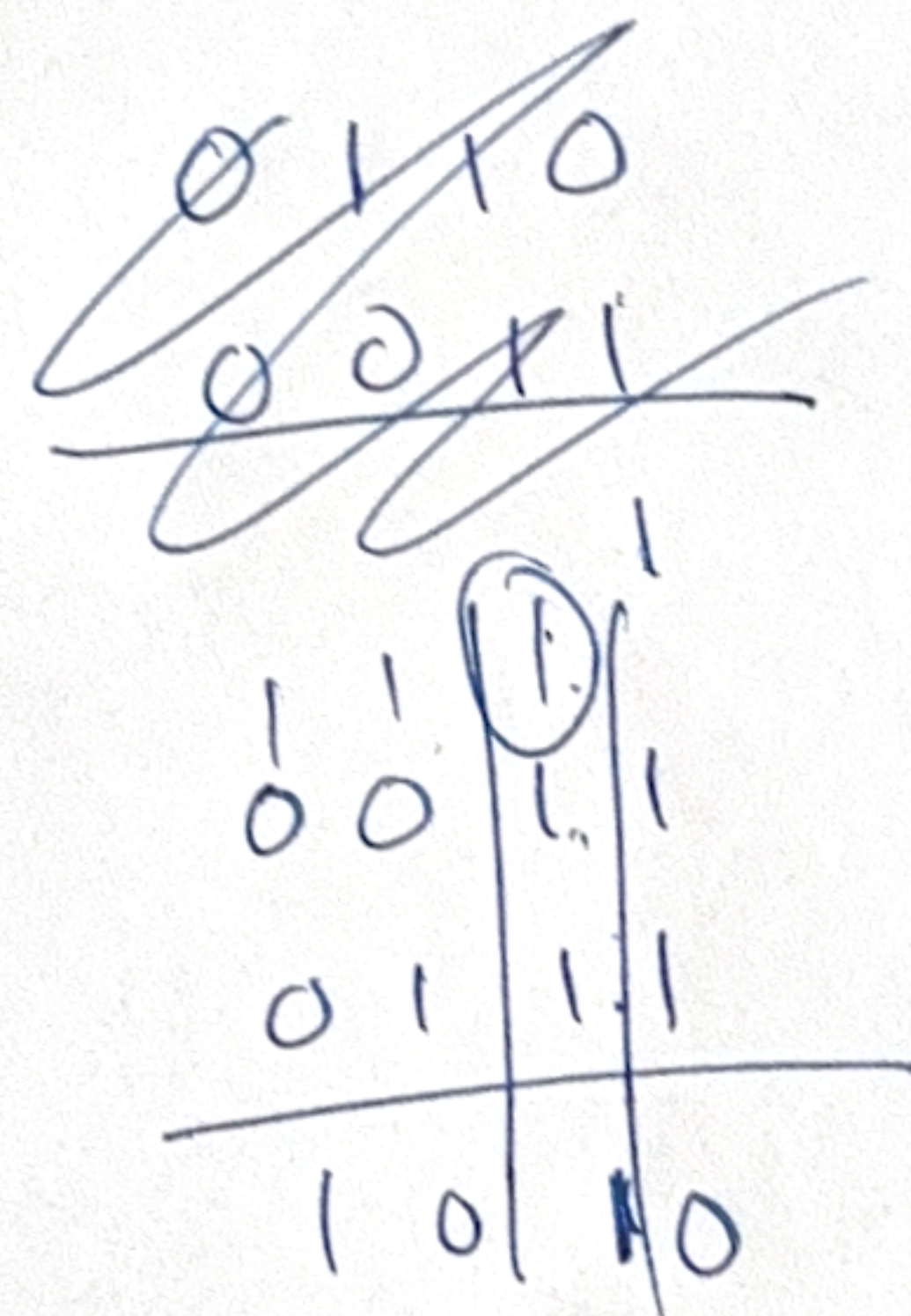
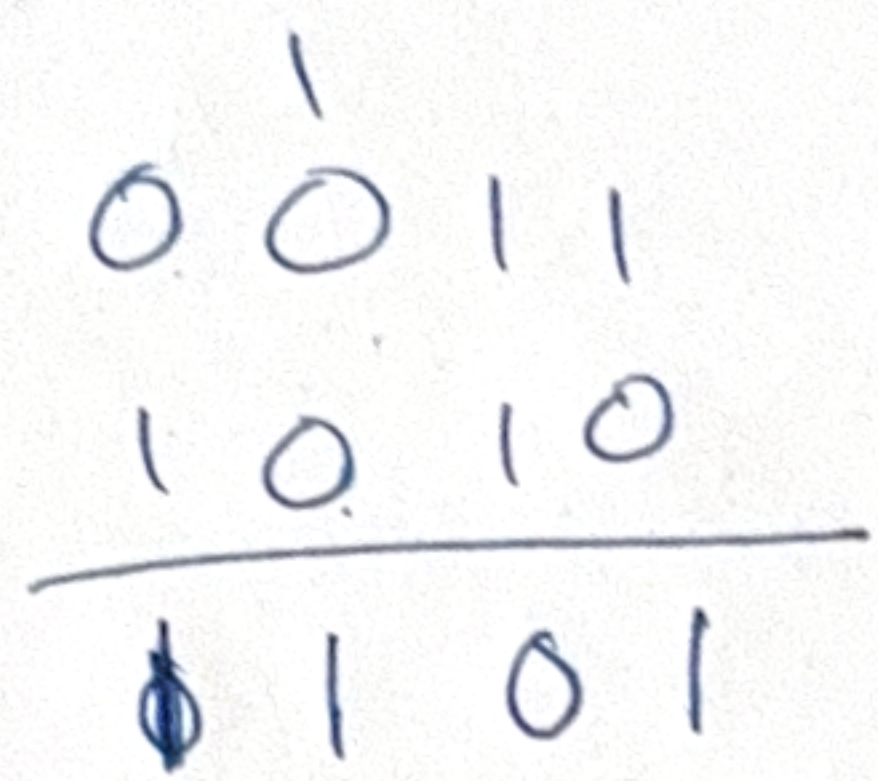
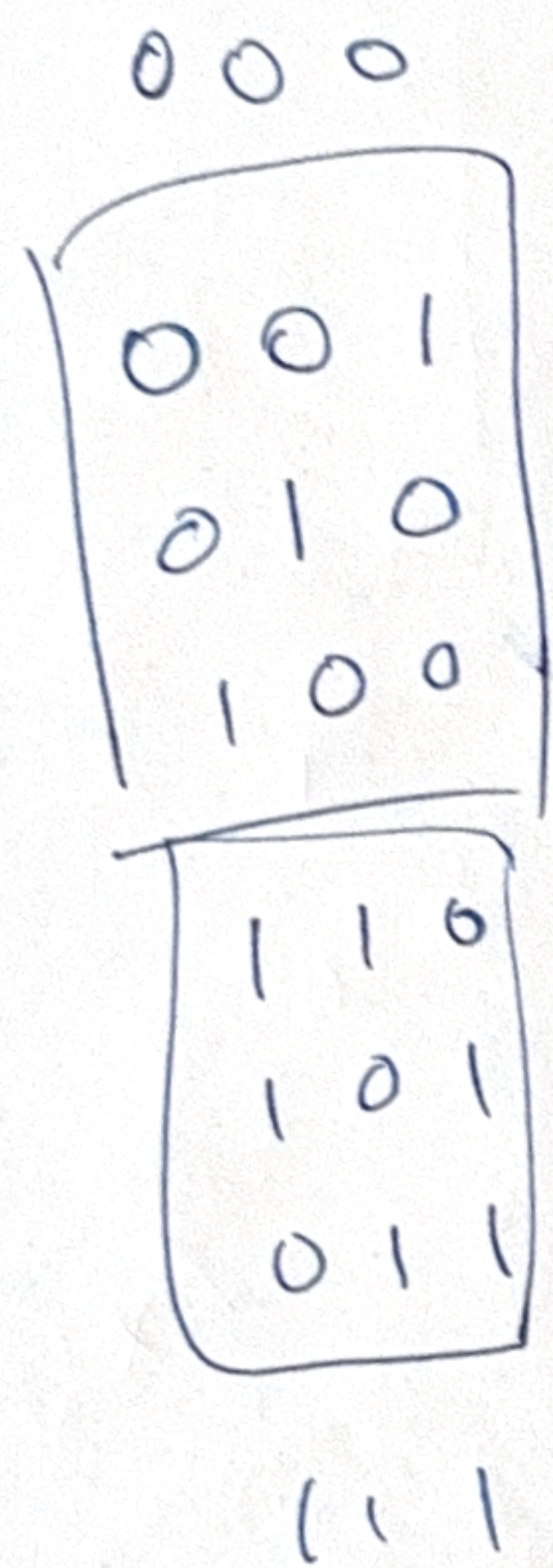


↑↑↑
Source



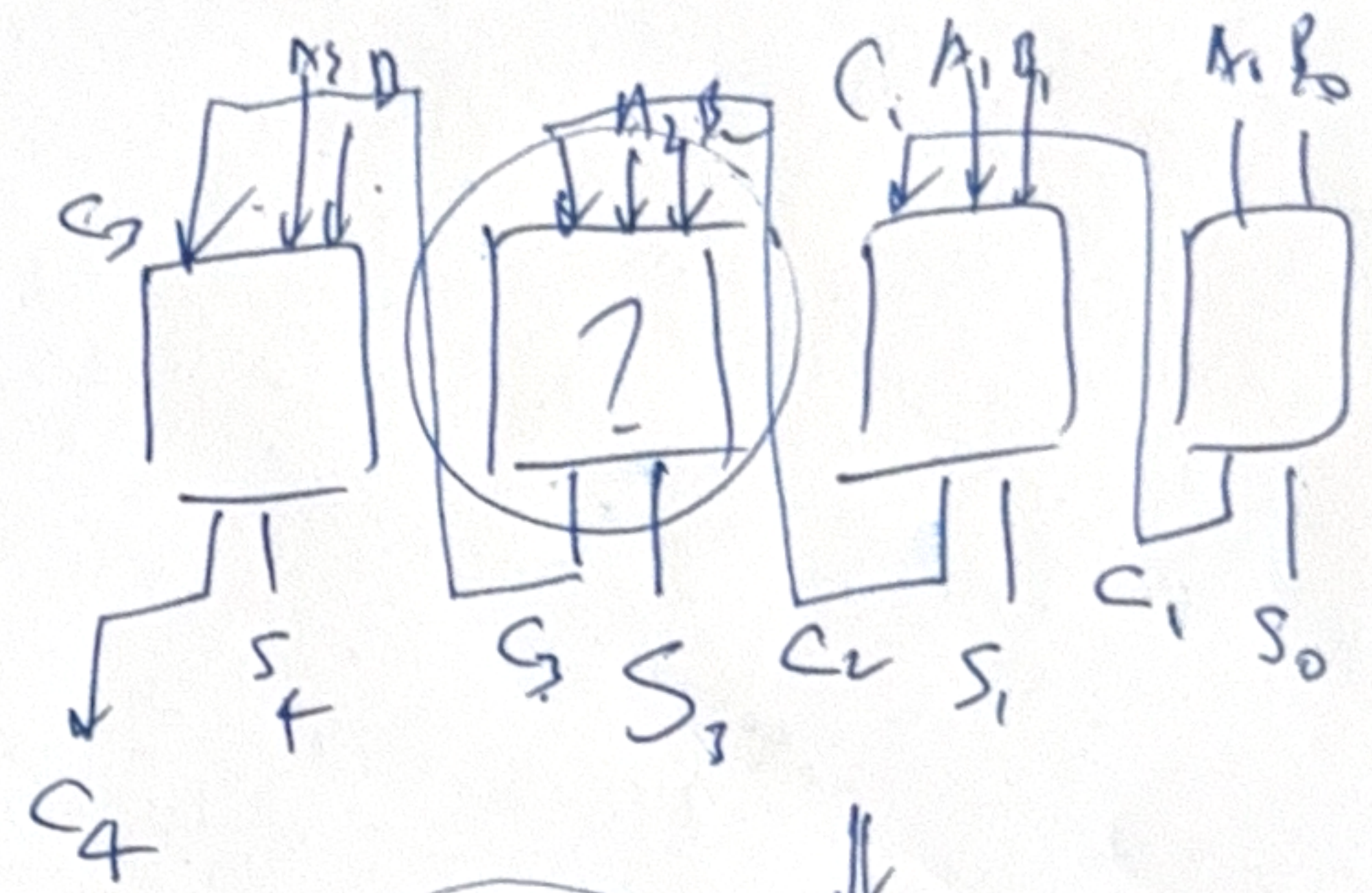
9/8/25

(6)



ONE
BIT
ADDRESS

FULL
ADDRESS



A	B	C _{in}	C _{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1