Labs 1,2,3,4 aLec01 to aLec15

This is a closed book exam, with one 8.5 by 11-inch crib sheet. You have 75 minutes, so please allocate your time accordingly. You may not search the internet or communicate with other people in any way during the quiz. You cannot use a calculator, but will not need one.

We trust you will uphold UT's Honor Code by making sure your answers are your own and you have not consulted with another person.

Fixed-point numbers (decimal/binary, signed/unsigned, 8/16/32 bit)
1) Convert value to integer. E.g., What integer is stored in the computer, when the value 2.1 is stored in 16-bit unsigned binary fixed-point, with a resolution of 2**-10? Answer: I = 2.1*1024, which is about 2150. I will make the math so easy a calculator will not be needed.
2) Convert integer to value. E.g., What is the value of an 8-bit signed decimal fixed-point number (resolution is 0.1) if the integer stored in memory is –123? Answer: –123*0.1 equals –12.3.
3) Basic concepts of range, resolution and rounding.
4) Given the range and resolution, choose the format

Programming (C on the Arm Cortex M) Techniques
1) How to check for overflow when performing integer calculations in C. Answer: promote to higher precision and check intermediate results.
2) Stack picture: function call, function parameters, locals, and interrupt service stack frame
3) Memory allocation: global, local, constants, and reset/interrupt vectors
4) Modularity linking call graph to `#include 'file.h'`, private versus public
5) `const volatile static`
6) Data flow graph
7) Debugging: dumps, monitors, scans, breaks, filter, profiling
8) Putting prototypes to public functions in the `'file.h'`, implementations in the `'file.c'`

I/O concepts (on the TM4C123): focus on concepts and don't memorize details
1) Direction register. Friendly means setting only the bits that are needed, leaving the rest unchanged.
2) Concept of bit-specific access to GPIO ports. Not details, but the concepts of friendly and critical sections
2) Masking input bits to check for individual signals, making individual output bits high, low, or toggle.
3) Using SysTick to measure elapsed time, and to create a time delay
4) Periodic timer interrupts: rate, and vector (jitter)

Detailed I/O programming (on the TM4C123)
1) FIFO implementation
2) Periodic timer interrupts using Timer0A and/or SysTick
3) Debugging dumps, profiles
4) Mailbox and semaphore
5) Edge-triggered interrupt on Port A or B

Interfacing
1) Switches with debouncing and LEDs
2) MOSFET interface (G D S understanding), using diode or capacitor to remove back EMF;
3) Speaker (where software creates a squarewave)
4) Simple circuit model for N-channel MOSFET transistors in on/off applications

IoT

IP addresses, DNS (what, why), UDP (what, why), TCP (what, why), sockets (types, what, why), Steps involved in client-server paradigm.

Definitions (match definition with the following terms)
Real-time, friendly, latency, ROM, RAM, computer, CPU, Harvard architecture, von Neumann architecture processor, registers, bus, embedded computer, microprocessor, microcomputer, microcontroller, I_{OL}, I_{OH}, I_{IL}, I_{IH},

V_{OL}, V_{OH}, V_{IH}, V_{IL}, capacitive loading, nonvolatile, open collector, open drain, tristate, memory-mapped I/O, dynamic efficiency, static efficiency, functional debugging, performance debugging, non-intrusiveness, profile, desk check, instrument, stabilize, scan, break, thread, busy wait, CPU bound, I/O bound, atomic, critical section, reentrant, interrupt vector, interrupt acknowledge, interrupt arm, interrupt enable, interrupt priority, board support package, functional abstraction, complexity abstraction, cohesion, coupling, latency, power budget, probability mass function, Central Limit Theorem

Variables

RAM versus ROM
Public scope versus private scope
Temporary versus permanent allocation
Precision

Know voltage current power in R, L or C. Time constant, step response (RC RL LC circuits)

Definitions

Fall 2011 Quiz 1, debugging profile
Fall 2011 Quiz 1, semaphore application
Fall 2012 Quiz 1, Questions 1-2, What is LR, stabilize, profile, intrusive?
Fall 2012 Quiz 1, Question 3, Is the FIFO reentrant?
Fall 2012 Quiz 1, Question 5, Scope of a variable
Fall 2012 Quiz 1, Question 6, Voltage and current across a capacitor
Fall 2015 Quiz 1, Question 1, Probability Mass Function, Central Limit Theorem
Fall 2017 Quiz 1, Question 7, UDP vs TCP
Fall 2016 Quiz 1, Question 1, Central Limit Theorem
Fall 2016 Quiz 1, Question 1, `const`, `static`
Fall 2016 Quiz 1, Question 1, Connection socket
Spring 2017 Quiz 1, Question 5, `const`, `volatile`, `static`
Spring 2018 Quiz 1, Question 8, use of FIFO for interfacing I/O bound versus CPU bound
Spring 2021 Quiz 1, Question 12, definitions
Spring 2021 Quiz 1, Question 13, real time

Interrupts

Fall 2012 Quiz 1, Question 7, Write code to measure time jitter using SysTick
Fall 2014 Quiz 1, Question 1, debugging, FIFOs and CPU bound
Fall 2014 Quiz 1, Question 2, Critical section
Fall 2014 Quiz 1, Question 4, Edge-triggered interrupts
Fall 2015 Quiz 1, Question 2, Critical section
Fall 2015 Quiz 1, Question 5, SysTick interrupts, debounce switches
Fall 2016 Quiz 1, Question 2, Critical section
Fall 2016 Quiz 1, Question 6, Edge-triggered interrupts
Fall 2016 Quiz 1, Question 7, debugging interrupts
Fall 2016 Quiz 1, Question 8, SysTick interrupts
Spring 2017 Quiz 1, Question 1, Critical section (new architecture)
Spring 2017 Quiz 1, Question 6, interrupts and stack
Spring 2017 Quiz 1, Question 8, periodic interrupt
Spring 2018 Quiz 1, Question 1, Critical section
Spring 2018 Quiz 1, Question 7, interrupts and the I bit
Spring 2018 Quiz 1, Question 10, SysTick interrupts, debounce switches
Fall 2019 Quiz 1, Question 5 producer/consumer, FIFO size PMF
Fall 2019 Quiz 1, Question 6 Critical section
Fall 2019 Quiz 1, Question 8 Interrupt jitter
Fall 2019 Quiz 1, Question 11 Firm real time
Fall 2019 Quiz 1, Question 12 Edge-triggered interrupts

Spring 2021 Quiz1, Question 1 Periodic Timer interrupt
Spring 2021 Quiz1, Question 2 Edge-triggered interrupt
Spring 2021 Quiz 1, Question 7, producer/consumer, FIFO size PMF
Spring 2021 Quiz 1, Question 8, Critical section
Spring 2022 Quiz 2, Question 4, Periodic Timer interrupt
Spring 2022 Quiz 2, Question 5, DAC SNR using a spectrum analyzer
Spring 2022 Quiz 1, Question 7, Periodic Timer interrupt

Fixed-Point

Fall 2011 Quiz 1, Question 6, Fixed-point math, implemented in C
Fall 2012 Quiz 1, Question 4, binary fixed point
Fall 2015 Quiz 1, Question 8, fixed point divide
Fall 2016 Quiz 1, Question 5, decimal fixed point
Spring 2017 Quiz 1, Question 4, decimal fixed point
Spring 2018 Quiz 1, Question 4, binary fixed point
Fall 2019 Quiz 1, Question 9 fixed-point design
Spring 2021 Quiz 1, Question 10, binary fixed point

Hardware interfacing (replace BJT/2N2222 interfacing with MOSFET e.g., IRLD120)

Fall 2011 Quiz 1, Question 3, Xbee interface (V_{OL}, V_{IL}, V_{OH}, V_{IH})
Fall 2011 Quiz 1, Question 7, LED interface (100 mA).
Fall 2012 Quiz 1, Question 6, V and I for ideal capacitor
Fall 2014 Quiz 1, Question 3, V_{OL}, V_{IL}, V_{OH}, V_{IH} interfacing
Fall 2014 Quiz 1, Question 5, V and I for ideal capacitor
Fall 2014 Quiz 1, Question 7, BJT (treat it like a speaker)
Fall 2015 Quiz 1, Question 3, V_{OL}, V_{IL}, V_{OH}, V_{IH} interfacing
Fall 2015 Quiz 1, Question 5, BJT interface of a speaker
Fall 2016 Quiz 1, Question 3, V_{OL}, V_{IL}, V_{OH}, V_{IH} interfacing
Fall 2016 Quiz 1, Question 4, V and I for ideal capacitor
Fall 2016 Quiz 1, Question 9, BJT interface of a 50-mA LED
Spring 2017 Quiz 1, Question 2, V_{OL}, V_{IL}, V_{OH}, V_{IH} interfacing
Spring 2017 Quiz 1, Question 3, Ideal capacitor
Spring 2017 Quiz 1, Question 9, SSR (LED) interface
Spring 2018 Quiz 1, Question 2, V_{OL}, V_{IL}, V_{OH}, V_{IH} interfacing
Spring 2018 Quiz 1, Question 3, Ideal capacitor and inductor
Spring 2018 Quiz 1, Question 9, BJT interface of a speaker
Fall 2019 Quiz 1, Question 3, Differential equation showing V and I for ideal capacitor
Fall 2019 Quiz 1, Question 4, Power line noise
Fall 2019 Quiz 1, Question 7, BJT interface of a speaker
Fall 2019 Quiz 1, Question 10, V_{OL}, V_{IL}, V_{OH}, V_{IH} interfacing
Spring 2021 Quiz1, Question 5 Complex impedance of capacitor
Spring 2021 Quiz 1, Question 6, Power line noise
Spring 2021 Quiz 1, Question 9, Speaker interface
Spring 2021 Quiz 1, Question 11, V_{OL}, V_{IL}, V_{OH}, V_{IH} interfacing
Spring 2022 Quiz 2, Question 2, RC time constant
Spring 2022 Quiz 2, Question 3, measure current
Spring 2022 Quiz 1, Question 6, Speaker interface, power

Internet of Things

Spring 2017 Quiz 1, Question 7, UDP
Spring 2018 Quiz 1, Question 5, IP address in big endian
Spring 2018 Quiz 1, Question 6, server code (not tested Fall 2018, but think of a similar)
Fall 2019 Quiz 1, Question 1, sockets

Fall 2019 Quiz 1, Question 2, virtual pins
Spring 2021 Quiz1, Question 3 Blynk topology
Spring 2021 Quiz1, Question 4 Blynk security
Spring 2022 Quiz 1, Question 1, TCP socket

You may use the I/O definitions from either header file tm4c123gh6pm.h in your answers without showing the define statements. E.g., these apply to all software

```
#include "tm4c123gh6pm.h"
```

These tables will be supplied (along the exam will use NPN and not PNP transistors)

Parameter	PN2222 (I_C=150mA) PN2907 (I_C=150mA)	2N2222 (I_C=500mA) 2N2907 (I_C=500mA)	TIP120 (I_C=3A) TIP125 (I_C=3A)
h_{fe}	100	40	1000
V_{BEsat}	0.6	2	2.5 V
V_{CE} at saturation	0.3	1	2 V

These parameters will be included for the TM4C12xx microcontroller (no 12mA mode will be used)

I_{OL} = 8mA, I_{OH} = 8mA, I_{IL} = 2µA, I_{IH} = 2µA,
V_{OL} = 0.4V, V_{OH} = 2.4V, V_{IL} = 1.3V, V_{IH} = 2.0 V

Address	31-24	23-17	16	15-3	2	1	0	Name
$E000E010	0	0	COUNT	0	CLK_SRC	INTEN	ENABLE	NVIC_ST_CTRL_R
$E000E014	0	24-bit RELOAD value						NVIC_ST_RELOAD_R
$E000E018	0	24-bit CURRENT value of SysTick counter						NVIC_ST_CURRENT_R

Address	31-29	28-24	23-21	20-8	7-5	4-0	Name
$E000ED20	TICK	0	PENDSV	0	DEBUG	0	NVIC_SYS_PRI3_R

	31–3	2–0	Name
$4003.0000		**GPTMCFG**	TIMER0_CFG_R

	31–4	3	2	1-0	
$4003.0004		**TAAMS**	**TACMR**	**TAMR**	TIMER0_TAMR_R

	14	13	11-10	8	6	5	3-2	0	
$4003.000C	TBPWML	TBOTE	TBEVENT	TBEN	TAPWML	TAOTE	**TAEVENT**	**TAEN**	TIMER0_CTL_R

	31-11	10	9	8	7-4	2	1	0	
$4003.0018		CBEIM	CBMIM	TBTOIM		**CAEIM**	CAMIM	TATOIM	TIMER0_IMR_R
$4003.001C		CBERIS	CBMRIS	TBTORIS		**CAERIS**	CAMRIS	TATORIS	TIMER0_RIS_R
$4003.0020		CBEMIS	CBMMIS	TBTOMIS		CAEMIS	CAMMIS	TATOMIS	TIMER0_MIS_R
$4003.0020		CBECINT	CBMCINT	TBTOCINT		**CAECINT**	CAMCINT	TATOCINT	TIMER0_ICR_R

	31–16	15–0	
$4003.0028	TAILRH	**TAILRL**	TIMER0_TAILR_R
$4003.0030	TAMRH	TAMRL	_TAMATCHR_R

	31–8	7-0	
$4003.0038		TAPSR	TIMER0_TAPR_R
$4003.0040		TAPSMR	TIMER0_TAPMR_R

	31–16	15-0	
$4003.0048	TARH	**TARL**	TIMER0_TAR_R

7	6	5	4	3	2	1	0	Name

DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA	GPIO_PORTB_DATA_R
DIR	DIR	DIR	DIR	DIR	DIR	DIR	DIR	GPIO_PORTB_DIR_R
IS	IS	IS	IS	IS	IS	IS	IS	GPIO_PORTB_IS_R
IBE	IBE	IBE	IBE	IBE	IBE	IBE	IBE	GPIO_PORTB_IBE_R
IEV	IEV	IEV	IEV	IEV	IEV	IEV	IEV	GPIO_PORTB_IEV_R
IME	IME	IME	IME	IME	IME	IME	IME	GPIO_PORTB_IM_R
RIS	RIS	RIS	RIS	RIS	RIS	RIS	RIS	GPIO_PORTB_RIS_R
MIS	MIS	MIS	MIS	MIS	MIS	MIS	MIS	GPIO_PORTB_MIS_R
ICR	ICR	ICR	ICR	ICR	ICR	ICR	ICR	GPIO_PORTB_ICR_R
SEL	SEL	SEL	SEL	SEL	SEL	SEL	SEL	GPIO_PORTB_AFSEL_R
DRV2	DRV2	DRV2	DRV2	DRV2	DRV2	DRV2	DRV2	GPIO_PORTB_DR2R_R
DRV4	DRV4	DRV4	DRV4	DRV4	DRV4	DRV4	DRV4	GPIO_PORTB_DR4R_R
DRV8	DRV8	DRV8	DRV8	DRV8	DRV8	DRV8	DRV8	GPIO_PORTB_DR8R_R
ODE	ODE	ODE	ODE	ODE	ODE	ODE	ODE	GPIO_PORTB_ODR_R
PUE	PUE	PUE	PUE	PUE	PUE	PUE	PUE	GPIO_PORTB_PUR_R
PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	GPIO_PORTB_PDR_R
SLR	SLR	SLR	SLR	SLR	SLR	SLR	SLR	GPIO_PORTB_SLR_R
DEN	DEN	DEN	DEN	DEN	DEN	DEN	DEN	GPIO_PORTB_DEN_R
CR	CR	CR	CR	CR	CR	CR	CR	GPIO_PORTB_CR_R
AMSEL	AMSEL	AMSEL	AMSEL	AMSEL	AMSEL	AMSEL	AMSEL	GPIO_PORTB_AMSEL_R

Address	31 – 29	23 – 21	15 – 13	7 – 5	Name
0xE000E400	GPIO Port D	GPIO Port C	GPIO Port B	GPIO Port A	NVIC_PRI0_R
0xE000E404	SSI0, Rx Tx	UART1, Rx Tx	UART0, Rx Tx	GPIO Port E	NVIC_PRI1_R
0xE000E408	PWM Gen 1	PWM Gen 0	PWM Fault	I2C0	NVIC_PRI2_R
0xE000E40C	ADC Seq 1	ADC Seq 0	Quad Encoder	PWM Gen 2	NVIC_PRI3_R
0xE000E410	Timer 0A	Watchdog	ADC Seq 3	ADC Seq 2	NVIC_PRI4_R
0xE000E414	Timer 2A	Timer 1B	Timer 1A	Timer 0B	NVIC_PRI5_R
0xE000E418	Comp 2	Comp 1	Comp 0	Timer 2B	NVIC_PRI6_R
0xE000ED20	SysTick	PendSV	--	Debug	NVIC_SYS_PRI3_R

Address	31	30	29-7	6	5	4	3	2	1	0	Name
0xE000E100	G	F	…	UART1	UART0	E	D	C	B	A	NVIC_EN0_R
0xE000E104			…						UART2	H	NVIC_EN1_R