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December 11, 2003, 9 am to 12 noon

This is an open book, open notes exam. You must put answers on this first piece of paper; please don't turn in any extra sheets.

(10) Question 1. Design an analog circuit with the following specifications

(5) Question 2. Which is the cheapest ROM part (select A,B,C,D,E,F)

(15) Question 3. Consider this op amp circuit.

Part a) What is its input impedance?

Part b) What is its output impedance?

Part c) What is its frequency response?

(5) Question 4. What is the value of the number?

(5) Question 5. Just name the 6812 signal pin.

(5) Question 6. At what rate should you run your PID controller?

(5) Question 7. Which measurement? Answer A,B,C,D,E

(5) Question 8. Which is the **data flow graph**? Answer A,B,C,D

(5) Question 9. The 6812 is running in expanded mode with 4 megabytes of extended program page ROM. Fill in the two boxes in the following software that reads physical location \$17506.

```
PPAGE =  ;
data = * ((char *) (  )) ;
```

(5) Question 10. The 6812 is running in expanded mode with 1 megabyte of extended data page RAM. Fill in the two boxes in the following software that reads physical location \$17506.

```
DPAGE =  ;
data = * ((char *) (  )) ;
```

(15) Question 11. A fuzzy logic controller

Part a) Give the four constants to be stored in the ROM-based structure.

Part b) Calculate the value of the input membership set if the crisp input were to be \$A0.

Part c) Describe the state of the plant if the crisp input were to be \$A0.

(5) Question 12. What is the pulse-width measurement resolution for the program? Give units.

(5) Question 13. What is the frequency measurement resolution for the program? Give units.

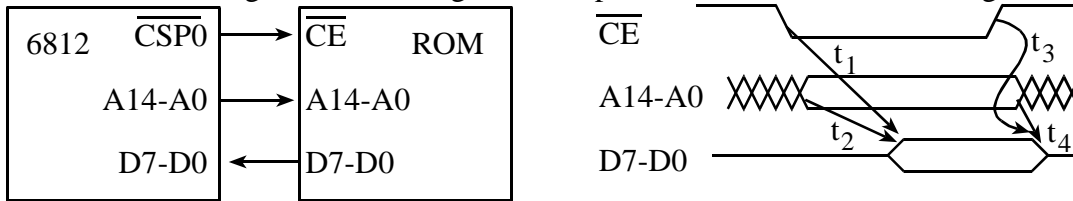
(10) Question 14. Just fill in the best term from the word bank.

- Part a) .
- Part b) .
- Part c) .
- Part d) .
- Part e) .

(10) Question 1. Design an analog circuit with the following specifications
 two single-ended inputs (not differential)
 any input impedance is OK
 transfer function $V_{out} = 5 \cdot V_1 - 3 \cdot V_2 + 5$

You are limited to one OP07 op amp and one reference chip (you choose it). Give chip numbers but not pin numbers. Specify all resistor values. You will use +12 and -12V analog supply voltages.

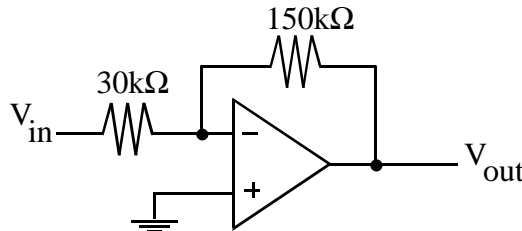
(5) Question 2. Consider a 6812/ROM interface that runs without cycle stretching. The MC68HC812A4 is running at 8 MHz using CSP0 chip select. Assume the following hardware.



Which is the cheapest ROM part that can run without cycle stretching? All times are in ns.

version	cost	t ₁	t ₂	t ₃	t ₄
A	\$6	20	30	5	5
B	\$5	30	30	10	5
C	\$4	30	40	10	10
D	\$3	50	50	10	10
E	\$2	70	70	10	10
F	\$1	100	100	10	10

(15) Question 3. Consider this op amp circuit built with an OP07 op amp. The OP07 input impedance is 20 MΩ, its open loop output impedance is 60 Ω, its open loop gain is 200000, and its bandwidth at 1 Hz is 400 kHz.



- Part a) What is the input impedance of this entire circuit?
- Part b) What is its output impedance of this entire circuit?
- Part c) What is its frequency response of this entire circuit?

(5) Question 4. A signed 16-bit binary fixed point number system has a Δ resolution of 1/32. What is the corresponding value of the number if the integer part stored in memory is 2000?

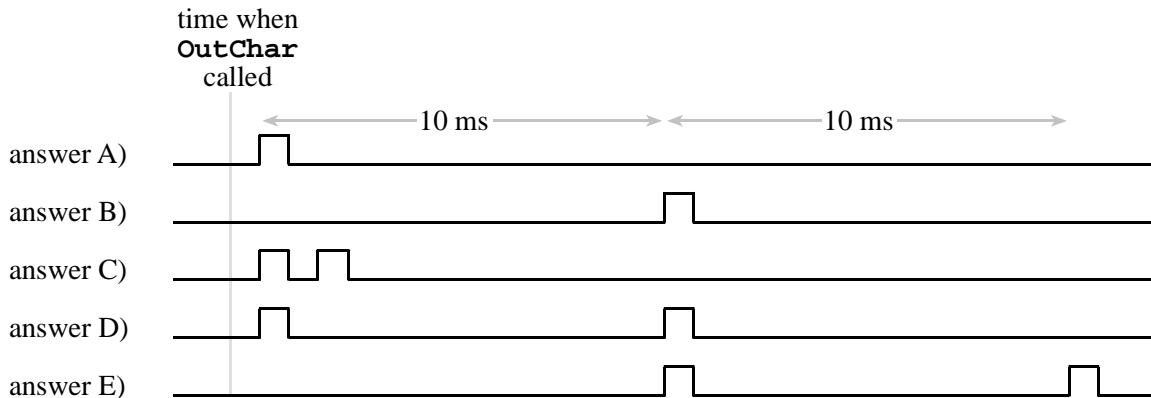
(5) Question 5. Assume there is a 16-bit wide RAM interfaced to the 6812 using two 8-bit RAM chips. If there is an 8-bit write to the 16-bit RAM, only one of the two 8-bit RAM chips should be activated. What 6812 signal is used to differentiate between an 8-bit write and a 16-bit write to the same address? Just name the 6812 signal pin.

(5) **Question 6.** You will be controlling the speed of a DC motor using a 6812-based PID controller. The motor has time constant of 1 second, which means it takes 1 second to reach 0.707 of the final speed after the input is changed. At what rate should you run your PID controller?

(5) **Question 7.** Consider the SCI system shown below, with just TDRE interrupts (no RDRF):

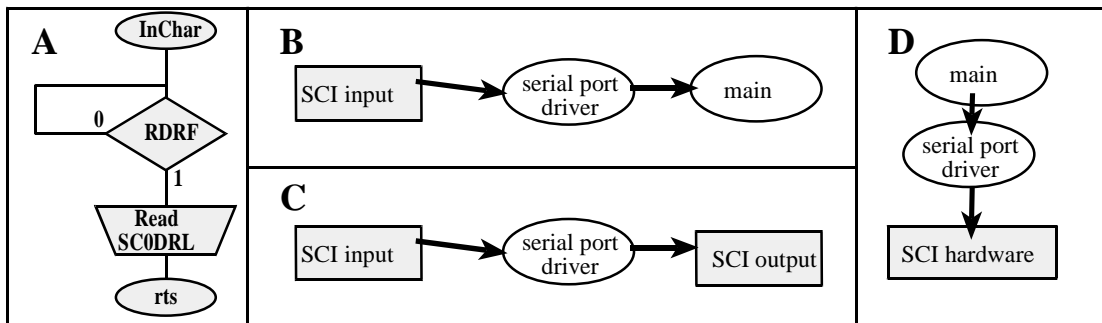
```
void SCI_OutChar(char data){
    while (TxFifo_Put(data) == 0){}; // spin if TxFifo is full
    SC0CR2 = 0x8C; // arm TDRE (no RIE)
}
#pragma interrupt_handler SciHandler
void SciHandler(void){ char data; char status;
    PORTA |= 0x01; // debugging profile
    status = SC0SR1; // first part of clear TDRE
    if(TxFifo_Get(&data))
        SC0DRL = data; // clears TDRE
    else
        SC0CR2 = 0x0c; // disarm TDRE
    PORTA &= ~0x01;
}
```

Assume the baud rate is 1000 bits/sec, and PORTA bit 0 is an output connected to the logic analyzer. Also assume the SCI hardware is initially idle. Which of the following measurements do you expect to observe on PA0?



(5) **Question 8.** Which answer is the **data flow graph** for the following program? The **main** program calls **SCI_InChar**. No other SCI functions occur.

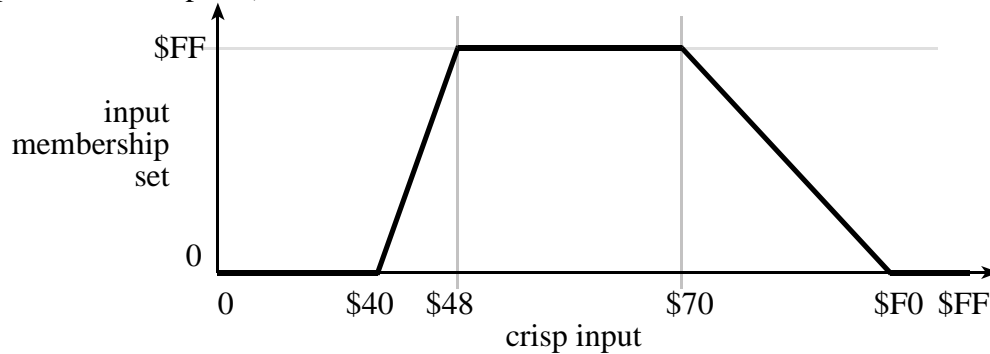
```
char SCI_InChar(void){
    while((SC0SR1 & RDRF) == 0){};
    return(SC0DRL);
}
```



(5) **Question 9.** See answer sheet.

(5) **Question 10.** See answer sheet.

(15) **Question 11.** A fuzzy logic controller needs to execute the following fuzzification step (crisp input to input membership set.)



Part a) What four constants should be stored in the ROM-based structure to allow the controller to execute this function with the `mem` instruction? I.e., how is this fuzzification function represented?

Part b) Calculate the value of the input membership set if the crisp input were to be \$A0.

Part c) Assuming the input membership means *Hot* (i.e., temperature too high), describe the state of the plant if the crisp input were to be \$A0.

(5) **Question 12.** What is the pulse-width measurement resolution for the following program? The signal is connected to both PT0 and PT1.

```
unsigned short PulseWidth;
/**interrupt on PT0, signal rising edge
// no interrupt on PT1, signal falling edge
#pragma interrupt_handler TC0handler
void TC0handler(void){
    TFLG1 = 0x01; // acknowledge interrupt
    PulseWidth = TC1-TC0; // time from falling to rising edge
}
void main(void){
    TIOS = 0; // all input capture
    DDRT = 0; // make all pins of Port T input
    TSCR = 0x80; // enable TCNT
    TMSK1 = 0x01; // arm IC0
    TMSK2 = 0x34; // set TCNT period
    TCTL4 = 0x09; // PT0 rise, PT1 fall
    asm(" cli"); // enable interrupts
    while(1){}
}
```

(5) **Question 13.** What is the frequency measurement resolution for the following program? The signal is connected to PT1. OC5 is used to create a periodic interrupt.

```
unsigned short Freq;
unsigned short Count; // Number of rising edges
#pragma interrupt_handler TC1handler()
void TC1handler(void){
    Count++; // number of rising edges
    TFLG1=0x02;} // ack, clear C1F
#pragma interrupt_handler TC5handler()
void TC5handler(void){
    TFLG1= 0x20; // Acknowledge
    TC5 = TC5+10000;
    Freq = Count;
    Count = 0; } // Setup for next
```

```

void ritual(void) {
asm(" sei");      // make atomic
  TIOS|=0x20;     // enable OC5
  TSCR=0x80;     // enable
  TMSK2=0x31;    // TCNT period
  TMSK1|=0x22;   // Arm OC5 and IC1
  TC5=TCNT+100;
  TCTL4 = (TCTL4&0xF3)|0x04; /* C1F set on rising edges */
  Count = 0;     // Set up for first
  TFLG1=0x22;   // clear OC5F
asm(" cli"); }

```

(10) Question 14. Select the best term that describes each definition.

Part a) A technique to periodically increase the priority of low-priority threads so that low priority threads occasionally get run. The increase is temporary.

Part b) The condition where low priority threads never get run.

Part c) The condition where thread 1 is waiting for a resource held by thread 2, and thread 2 is waiting for a resource held by thread 1.

Part d) The condition where a thread is prevented from running because it needs something that is unavailable.

Part e) The condition where once a thread blocks, there are a finite number of threads that will be allowed to proceed before this thread is allowed to proceed.

word bank

active	nonreentrant
aging	preemptive scheduler
blocked	producer-consumer
bounded buffer	reentrant
bounded waiting	rendezvous
critical section	round robin scheduler
deadlock	sleeping
killed	spin lock
maximum latency	starvation