

# 74HC244

## Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver

### High-Performance Silicon-Gate CMOS

The 74HC244 is identical in pinout to the LS244. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverting outputs and two active-low output enables.

The HC244 is similar in function to the HC240A.

#### Features

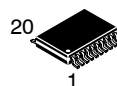
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 136 FETs or 34 Equivalent Gates
- This is a Pb-Free Device



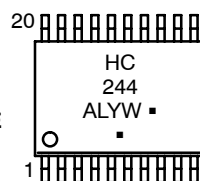
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#### MARKING DIAGRAM



**TSSOP-20  
DT SUFFIX  
CASE 948E**



HC244 = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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## PIN ASSIGNMENT

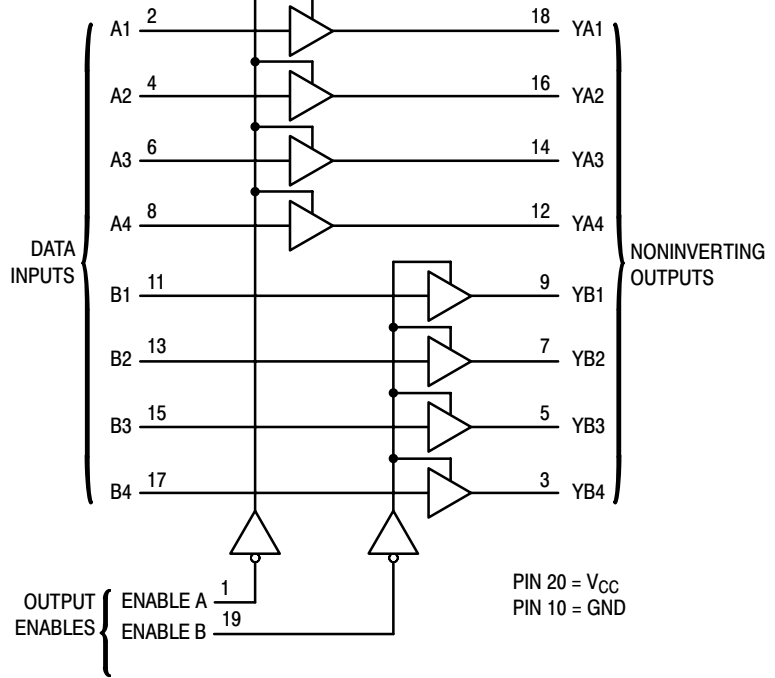
|          |    |    |                 |
|----------|----|----|-----------------|
| ENABLE A | 1  | 20 | V <sub>CC</sub> |
| A1       | 2  | 19 | ENABLE B        |
| YB4      | 3  | 18 | YA1             |
| A2       | 4  | 17 | B4              |
| YB3      | 5  | 16 | YA2             |
| A3       | 6  | 15 | B3              |
| YB2      | 7  | 14 | YA3             |
| A4       | 8  | 13 | B2              |
| YB1      | 9  | 12 | YA4             |
| GND      | 10 | 11 | B1              |

## FUNCTION TABLE

| Inputs                |      | Outputs |
|-----------------------|------|---------|
| Enable A,<br>Enable B | A, B | YA, YB  |
| L                     | L    | L       |
| L                     | H    | H       |
| H                     | X    | Z       |

Z = high impedance

## LOGIC DIAGRAM



## ORDERING INFORMATION

| Device       | Package   | Shipping†        |
|--------------|-----------|------------------|
| 74HC244DTR2G | TSSOP-20* | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

## MAXIMUM RATINGS

| Symbol           | Parameter   | Value                          | Unit |
|------------------|---|--------------------------------|------|
| V <sub>CC</sub>  | DC Supply Voltage (Referenced to GND)                           | - 0.5 to + 7.0                 | V    |
| V <sub>in</sub>  | DC Input Voltage (Referenced to GND)                            | - 0.5 to V <sub>CC</sub> + 0.5 | V    |
| V <sub>out</sub> | DC Output Voltage (Referenced to GND)                           | - 0.5 to V <sub>CC</sub> + 0.5 | V    |
| I <sub>in</sub>  | DC Input Current, per Pin                                       | ±20                            | mA   |
| I <sub>out</sub> | DC Output Current, per Pin                                      | ±35                            | mA   |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins                 | ±75                            | mA   |
| P <sub>D</sub>   | Power Dissipation in Still Air, TSSOP Package†                  | 450                            | mW   |
| T <sub>stg</sub> | Storage Temperature   | - 65 to + 150                  | °C   |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 Seconds (TSSOP Package) | 260                            | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min         | Max                | Unit |
|-------------------|--|-------------|--------------------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)  | 2.0         | 6.0                | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND)   | 0           | $V_{CC}$           | V    |
| $T_A$             | Operating Temperature, All Package Types   | - 55        | + 125              | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)<br>$V_{CC} = 2.0$ V<br>$V_{CC} = 4.5$ V<br>$V_{CC} = 6.0$ V | 0<br>0<br>0 | 1000<br>500<br>400 | ns   |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol   | Parameter                                      | Test Conditions   | $V_{CC}$<br>(V)          | Guaranteed Limit          |                           |                           | Unit    |
|----------|--|---|--------------------------|---------------------------|---------------------------|---------------------------|---------|
|          |  |   |                          | - 55 to<br>25°C           | ≤ 85°C                    | ≤ 125°C                   |         |
| $V_{IH}$ | Minimum High-Level Input Voltage               | $V_{out} = V_{CC} - 0.1$ V<br>$ I_{out}  \leq 20$ $\mu$ A                                       | 2.0<br>3.0<br>4.5<br>6.0 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | V       |
| $V_{IL}$ | Maximum Low-Level Input Voltage                | $V_{out} = 0.1$ V<br>$ I_{out}  \leq 20$ $\mu$ A  | 2.0<br>3.0<br>4.5<br>6.0 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | V       |
| $V_{OH}$ | Minimum High-Level Output Voltage              | $V_{in} = V_{IH}$<br>$ I_{out}  \leq 20$ $\mu$ A  | 2.0<br>4.5<br>6.0        | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         | V       |
|          |  | $V_{in} = V_{IH}$ $ I_{out}  \leq 2.4$ mA<br>$ I_{out}  \leq 6.0$ mA<br>$ I_{out}  \leq 7.8$ mA | 3.0<br>4.5<br>6.0        | 2.48<br>3.98<br>5.48      | 2.34<br>3.84<br>5.34      | 2.2<br>3.7<br>5.2         |         |
| $V_{OL}$ | Maximum Low-Level Output Voltage               | $V_{in} = V_{IL}$<br>$ I_{out}  \leq 20$ $\mu$ A  | 2.0<br>4.5<br>6.0        | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         | V       |
|          |  | $V_{in} = V_{IL}$ $ I_{out}  \leq 2.4$ mA<br>$ I_{out}  \leq 6.0$ mA<br>$ I_{out}  \leq 7.8$ mA | 3.0<br>4.5<br>6.0        | 0.26<br>0.26<br>0.26      | 0.33<br>0.33<br>0.33      | 0.4<br>0.4<br>0.4         |         |
| $I_{in}$ | Maximum Input Leakage Current                  | $V_{in} = V_{CC}$ or GND  | 6.0                      | ±0.1                      | ±1.0                      | ±1.0                      | $\mu$ A |
| $I_{OZ}$ | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>$V_{in} = V_{IL}$ or $V_{IH}$<br>$V_{out} = V_{CC}$ or GND    | 6.0                      | ±0.5                      | ±5.0                      | ±10                       | $\mu$ A |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND<br>$I_{out} = 0$ $\mu$ A   | 6.0                      | 4.0                       | 40                        | 40                        | $\mu$ A |

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

| Symbol                   | Parameter  | $V_{CC}$<br>(V)          | Guaranteed Limit      |                       |                       | Unit |
|--------------------------|--|--------------------------|-----------------------|-----------------------|-----------------------|------|
|                          |  |                          | – 55 to<br>25°C       | ≤ 85°C                | ≤ 125°C               |      |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Maximum Propagation Delay, A to YA or B to YB<br>(Figures 1 and 3)         | 2.0<br>3.0<br>4.5<br>6.0 | 96<br>50<br>18<br>15  | 115<br>60<br>23<br>20 | 135<br>70<br>27<br>23 | ns   |
| $t_{PLZ}$ ,<br>$t_{PHZ}$ | Maximum Propagation Delay, Output Enable to YA or YB<br>(Figures 2 and 4)  | 2.0<br>3.0<br>4.5<br>6.0 | 110<br>60<br>22<br>19 | 140<br>70<br>28<br>24 | 165<br>80<br>33<br>28 | ns   |
| $t_{PZL}$ ,<br>$t_{PZH}$ | Maximum Propagation Delay, Output Enable to YA or YB<br>(Figures 2 and 4)  | 2.0<br>3.0<br>4.5<br>6.0 | 110<br>60<br>22<br>19 | 140<br>70<br>28<br>24 | 165<br>80<br>33<br>28 | ns   |
| $t_{TLH}$ ,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output<br>(Figures 1 and 3)            | 2.0<br>3.0<br>4.5<br>6.0 | 60<br>23<br>12<br>10  | 75<br>27<br>15<br>13  | 90<br>32<br>18<br>15  | ns   |
| $C_{in}$                 | Maximum Input Capacitance  | –                        | 10                    | 10                    | 10                    | pF   |
| $C_{out}$                | Maximum Three-State Output Capacitance<br>(Output in High-Impedance State) | –                        | 15                    | 15                    | 15                    | pF   |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| $C_{PD}$ | Power Dissipation Capacitance (Per Buffer)* | Typical @ 25°C, $V_{CC} = 5.0$ V | pF |
|----------|---|----------------------------------|----|
|          |   | 34                               |    |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## SWITCHING WAVEFORMS

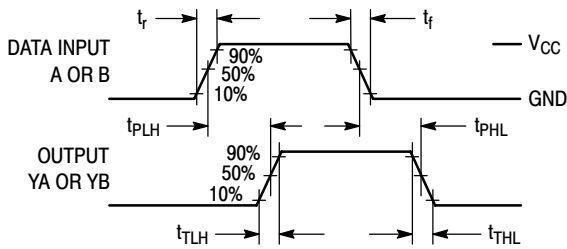


Figure 1.

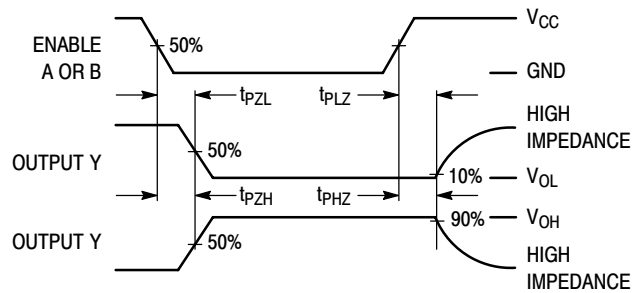



Figure 2.





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